CML Microcircuits
COMMUNICATION SEMICONDUCTORS

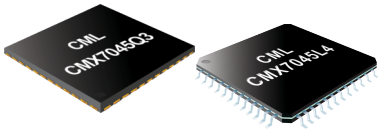
Product Preview

PP7045/1 November 2011

CMX7045

Marine AIS-SART Processor

(Automatic Identification System—Search and Rescue Transmitter)



48-pin VQFN 48-pin LQFP

Market Overview

AIS-SART (Automatic Identification System—Search and Rescue Transmitter) is a self-contained unit used to locate a survival craft, life raft, distressed vessel or person by sending updated position reports using standard AIS position reports.

The specification for the AIS-SART has been developed by the IEC (International Electrical Committee), TC80 AIS Work Group.

The AIS-SART was added to the GMDSS regulations, effective January 2010. The international standard is IEC 61097-14.

AIS-SART derives position and time synchronisation from a built-in GNSS receiver and transmits its position with an update rate of 1 minute. Eight identical position reports are sent each minute to maintain a high probability that at least one of the position reports is sent on the highest point of a wave.

Long battery life is a critical requirement, units must have a long standby battery life and be ready to operate in a distress situation for a long period of time.

AIS-SARTs are typically cylindrical, brightly coloured and can also be incorporated into life jackets.

CMX7045 Brief Description

The CMX7045 is a dedicated processor for marine Automatic Identification System-Search and Rescue Transmitter (AIS-SART) operation, fully meeting the requirements of the IEC 61097-14 international standard.

This highly-integrated and flexible device includes a 9600 baud GMSK modulator for transmission of formatted data. Additional auxiliary functions are also provided to further support the system host, these include: a two-input 10-bit ADC, four 10-bit DACs, two system clock outputs and four GPIOs.

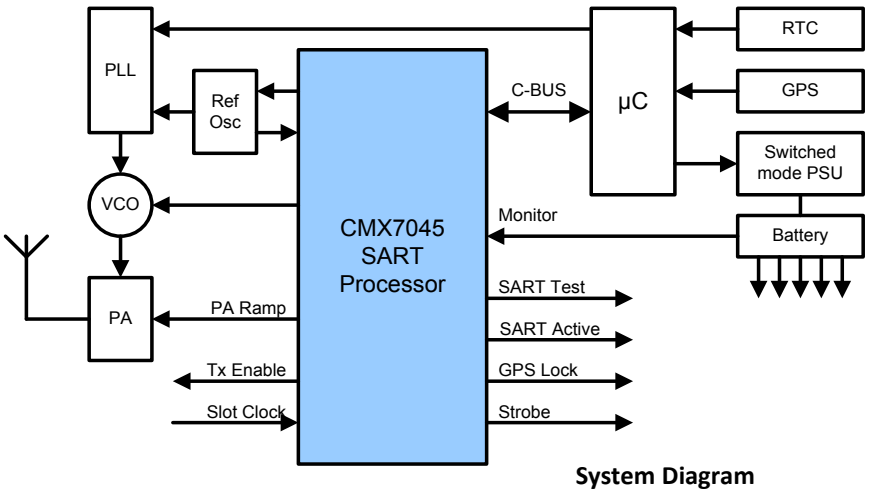
The CMX7045 offers low-power sleep modes to ensure maximum system battery life and is available in a small 48-pin LQFP or VQFN package.

Features

- Tx AIS 9600bps GMSK modulator
- AIS burst frame formatting
  - Bit stuffing
  - NRZI coding
  - Training sequence insertion
  - CRC generation
  - AIS slot Tx buffer
- Flexible Tx interface
- Conforms to IEC 61097-14
- Battery monitor function
- Configured by Function Image™
- Auxiliary functions
  - Two clock generators
  - Two 10-bit ADCs
  - Four 10-bit DACs
- Active integration roadmap
- Low-power 3V-3.6V operation
- Small, low profile 48-pin LQFP and VQFN

Key Benefits

- Equipment – fast time to market
- Off-the-shelf solution
- Reduced development time
- Field proven operation and performance
- Only requires small, low-cost host micro
- High integration solution
- Includes many sub-systems that reduce the overall system size and cost:
  - PA ramp automation
  - ADC for battery monitor
  - Integrated AIS modem with Tx burst frame formatting
- Built on *FirmASIC* ® technology
- Evaluation kit and support available
- Roadmap to high quantity, low cost
- Maximum support

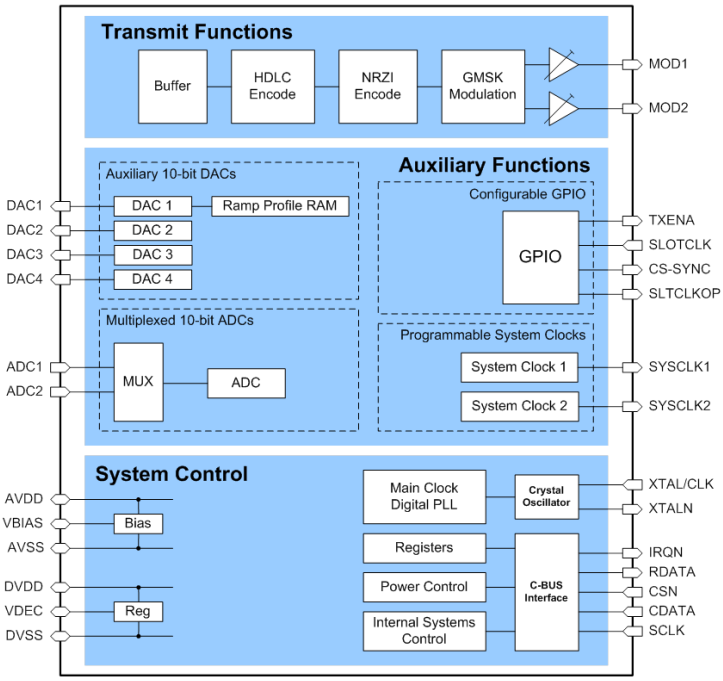


System Diagram

General Description

The AIS system uses two basic channel access mechanisms: Self Organising Time Division Multiple Access (SOTDMA) and Carrier-Sensing Time Division Multiple Access (CSTDMA). The CMX7045 is compatible with both systems and offers additional features which simplify the implementation of an AIS-SART device conforming to international standard IEC 61097-14.

The CMX7045 is built on *FirmASIC* ® technology. The Function Image™ (FI) file, which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software.
The FI data file is no greater than 24kbytes.



Function Block Diagram

Tx Modem Functions

- AIS 25kHz channel
  - (GMSK, 9600bps, 2.4kHz deviation, BT = 0.4)
- AIS Burst mode with full AIS frame formatting (HDLC-type)
  - Bit stuffing
  - NRZI coding
  - Training sequence and start/stop flag insertion
  - CRC generation
- AIS Raw mode (for greater flexibility)
- Supports arbitrary data streams for user-defined protocols
- 160-byte (equivalent to 5 AIS slots) Tx data buffer
- Flexible Tx Interface
- Two-point modulation outputs, with independent gain and polarity controls

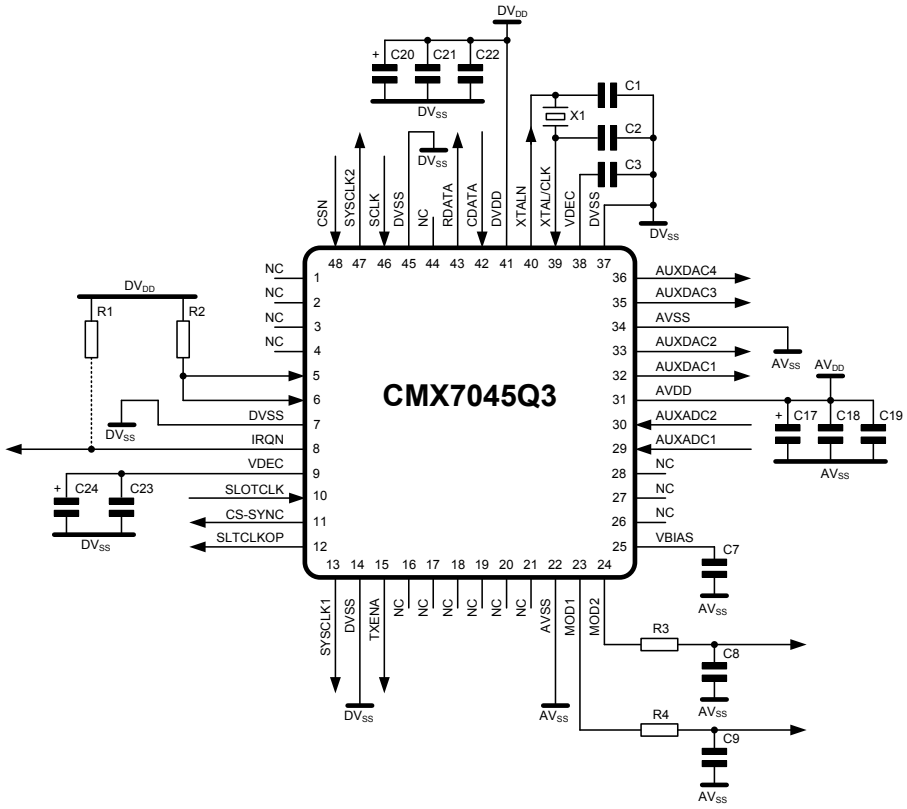
Analogue I/O Functions

- Auxiliary ADC system
  - A two-input 10-bit successive approximation ADC with integrated sample and hold
- Auxiliary DAC system
  - Four general-purpose auxiliary 10-bit DACs
  - Ramping auxiliary DAC (using DAC 1)
    - DAC steps through a user-configured sequence of DAC output values to develop a specific rising/falling DAC output signal. This is useful for ramping an RF PA, and can be configured to operate automatically at the start and end of a burst.

System Functions

- All internal sub-systems are controlled via a single serial host interface to reduce host µC pin count and simplify external host driver complexity
- Transaction oriented command/response logical host interface executes tasks, supporting normal operation, device configuration, and functions to assist manufacturing calibration trimming of external circuits
- Internal system clock derived from reference oscillator and eliminates the need for additional XTAL or baseband clock oscillator
- Auxiliary clock synthesisers generate two clocks for external use to support peripheral devices
- Function Image™ is loaded directly from the host µC via C-BUS
- Integrated 2.5V regulator can develop 2.5V from required 3.3V supply
- Powersave facilities minimise total system power.

Pin-out and External Components

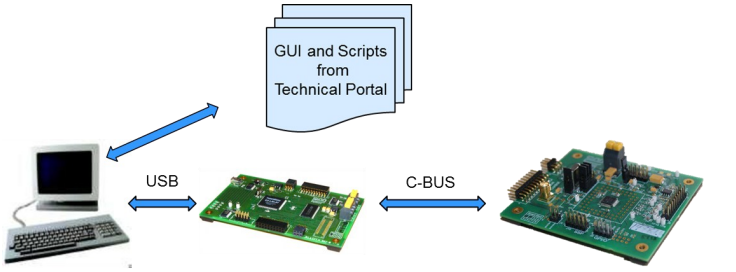


Components	
R1	100k
R2	220k
R3	100k
R4	100k
C1	18pF
C2	18pF
C3	10nF
C7	100nF
C8	100pF
C9	100pF
C17	10µF
C18	10nF
C19	10nF
C20	10µF
C21	10nF
C22	10nF
C23	10nF
C24	10µF
X1	9.6MHz

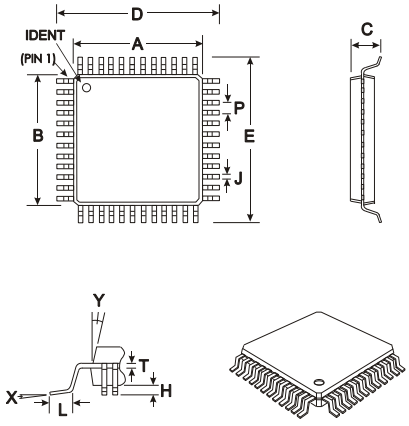
Evaluation Support

The CMX7045 can be evaluated with the PE0402 CMX704x series evaluation kit. Interfacing to a PC can be achieved with our PE0002 universal interface card with GUI and scripts available to assist product evaluation.

Alternatively any microcontroller evaluation/emulator kit can be used to drive the CMX7045's serial bus.



Package Options



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

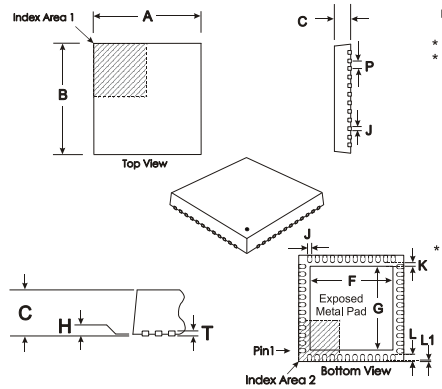
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Mechanical Outline for 48-pin LQFP Package (L4)

Order as CMX7045L4



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 — Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Mechanical Outline for 48-pad VQFN Package (Q3)

Order as CMX7045Q3

Electrical Specification Summary

Operating Limits	Min.	Max.	Unit
Supply Voltage:			
$DV_{DD} – DV_{SS}$	3.0	3.6	V
$AV_{DD} – AV_{SS}$	3.0	3.6	V
$V_{DEC} – DV_{SS}$	2.25	2.75	V
Operating Temperature	-40	+85	°C
Clock Frequency	9.6	19.2	MHz
Function Image™ size		24	kBytes

DC Parameter - Supply Current	Min.	Typ.	Max.	Unit
All Powersaved (Deep Sleep mode)				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)	–	24	100	µA
AI_{DD} (AV_{DD} = 3.3V)	–	4	20	µA
Tx Mode				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)	–	20	–	mA
AI_{DD} (AV_{DD} = 3.3V)	–	11	–	mA

Transmit Parameters	Min.	Typ.	Max.	Unit
AIS (GMSK 9600bps), 25kHz channel				
Bit rate accuracy	–	–	±50	ppm
BT	–	0.4	–	
Storage time (filter delay)	–	8	–	bits
Tx Buffer size	–	–	176	Bytes
SLOT CLOCK Rise/Fall time	–	–	1.0	µs

Comprehensive technical datasheet and support material is available from the CML website.

Click here to link to the CML website or search for: CMX7045

Infinite Capabilities . . . FirmASIC® . . . Maximum Flexibility

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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