

CCD VERTICAL DRIVER FOR DIGITAL CAMERAS

Check for Samples: [VSP1900](#)

FEATURES

- **CCD Vertical Driver:**
 - Three Field CCD Support
 - Two Field CCD Support
- **Output Drivers:**
 - 3 Levels Driver (V-Transfer) x 5
 - 2 Levels Driver (V-Transfer) x 3
 - 2 Levels Driver (E-Shutter) x 1
- **Driver Capability:**
 - 450 pF to 1890 pF With 60 Ω to 240 Ω
- **Input Phase:**
 - 3 State (V-Transfer) x 5
 - 2 State (V-Transfer) x 3
 - 2 State (E-Shutter) x 1
- **Portable Operation**
 - Input Interface: 2.7 V to 5.5 V

- **Power Supply:**
 - VDD 2.7 V to 5.5 V
 - VL –5 V to –9 V
 - VM GND
 - VH 11.5V to 15.5 V

APPLICATIONS

- Digital Camera
- Video Camera

DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric-shutter support. This device is composed of eight vertical transfer channels, which support both 3-field CCD and 2-field CCD operation. The VSP1900 contributes low power consumption and device count reduction in the system.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGING ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDER NUMBER	TRANSPORT MEDIA
VSP1900	TSSOP30	DBT	–25°C to 85°C	VSP1900	VSP1900	Tube (60 units per tube)

(1) For the most current specification and package information, refer to our web site at www.ti.com

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUES	UNIT
Supply voltage	VDD	GND –0.3 to 7	V
	VL	GND to –10	
	VH	VL + 26	
Input voltage, V_{IN}		GND –0.3 to (VDD + 0.3)	V
Ambient temperature under bias		–25 to 85	°C
Storage temperature, T_{stg}		–55 to 150	°C
Junction temperature, T_J		150	°C
Package temperature (IR reflow, peak)		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	2.7		5.5	V
Supply voltage, VL	–5		–9	V
Supply voltage, VH	11.5		15.5	V
Input voltage, V_{IN}		GND –.03 to (VDD + 0.3)		V

ELECTRICAL CHARACTERISTICS

 All specifications at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
DC power consumption				5.3		mW
Switching power consumption				550		mW
DC CHARACTERISTICS						
V_{IH}	High-level input voltage		0.7VDD			V
V_{IL}	Low-level input voltage		0.2VDD			V
I_{IN}	Input current	$V_{IN} = \text{GND to } 5 \text{ V (without pullup or pulldown resistor)}$	-10	0	10	μA
		$V_{IN} = \text{GND to } 5 \text{ V (pullup or pulldown resistor)}$	-625	0	625	
I_{IH}	Operating supply current		0.1			mA
I_{DD}			1			
I_{IL}			0.125			
I_{OL}	Output current	$V1, V2, V3A, V3B, V4, V5A, V5B, V6 = -8.1 \text{ V}$	10			mA
I_{OM1}		$V1, V2, V3A, V3B, V4, V5A, V5B, V6 = -0.2 \text{ V}$	-5			
I_{OM2}		$V1, V3A, V3B, V5A, V5B = 0.2 \text{ V}$	5			
I_{OH}		$V1, V3A, V3B, V5A, V5B = 14.55 \text{ V}$	-7.2			
I_{OSL}		$\text{SUB} = -8.1 \text{ V}$	5.4			
I_{OSH}		$\text{SUB} = 14.55 \text{ V}$	-4			

(1) Specified by design

SWITCHING CHARACTERISTICS

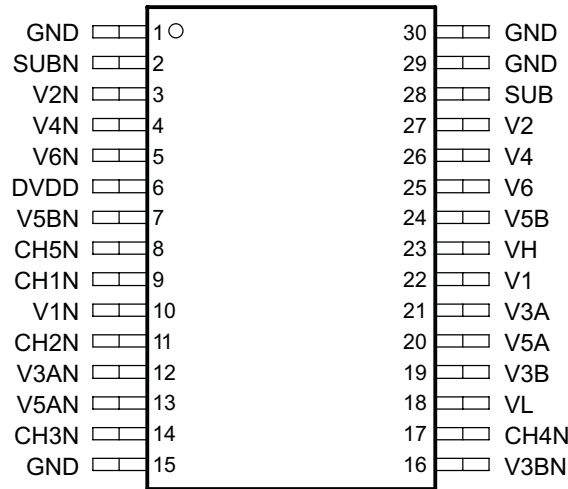
 All specification at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
$t_d(\text{PLM})$ $t_d(\text{PMH})$ $t_d(\text{PLH})$ $t_d(\text{PML})$ $t_d(\text{PHM})$ $t_d(\text{PHL})$	Propagation delay time			15	100	ns
				20	100	
				20	100	
				15	50	
				30	50	
				30	50	
$t_r(\text{TLM})$ $t_r(\text{TMH})$ $t_r(\text{TLH})$	Rise time	$V_L \rightarrow V_M$			300	ns
		$V_M \rightarrow V_H$			300	
		$V_L \rightarrow V_H$			300	
$t_f(\text{TML})$ $t_f(\text{THM})$ $t_f(\text{THL})$	Fall time	$V_M \rightarrow V_L$			300	ns
		$V_H \rightarrow V_M$			300	
		$V_H \rightarrow V_L$			300	
$V_n(\text{CLH})$ $V_n(\text{CLL})$ $V_n(\text{CMH})$ $V_n(\text{CML})$ $V_n(\text{CHL})$	Output noise voltage				2	V

(1) Specified by design

PIN ASSIGNMENTS

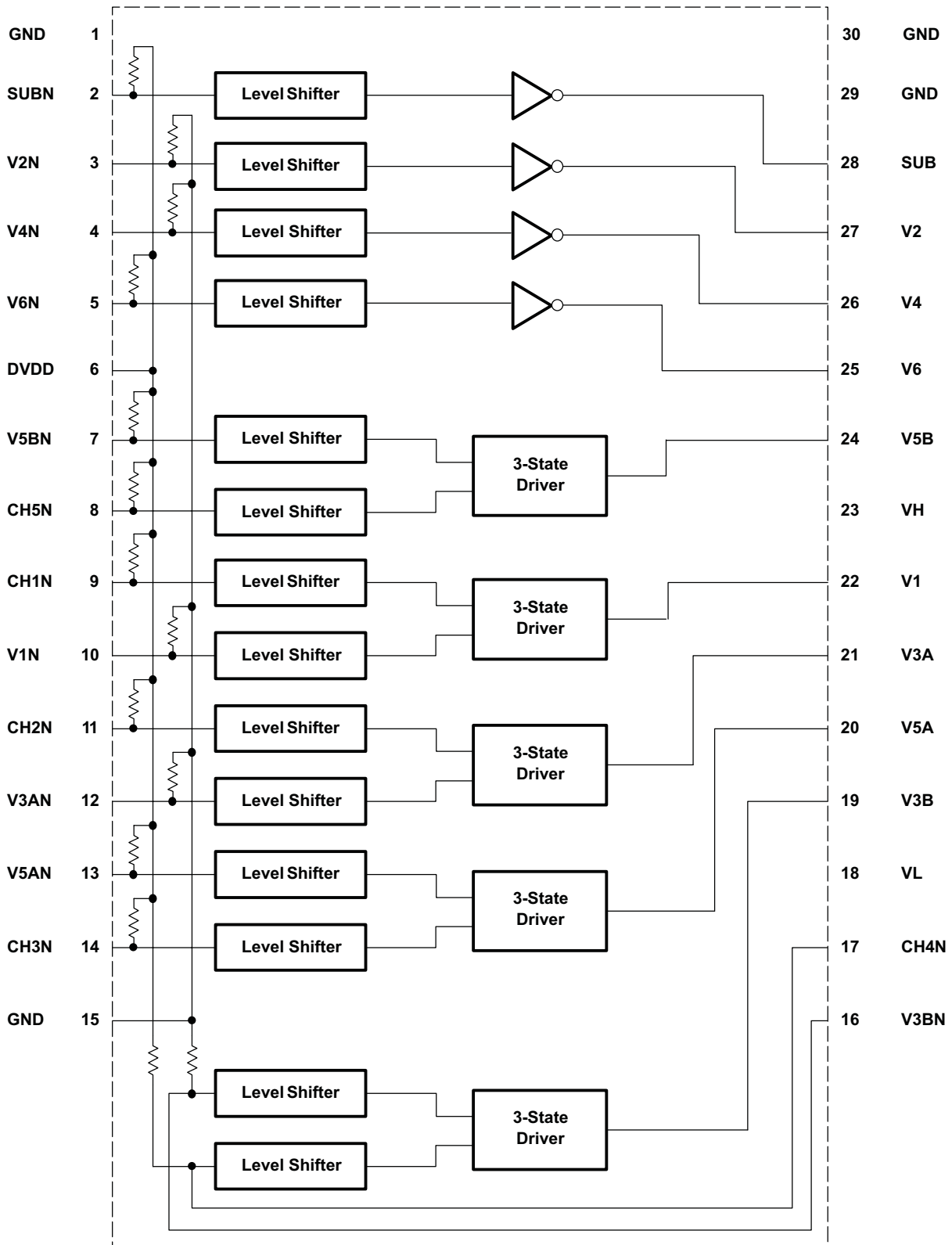
**DBT PACKAGE
(TOP VIEW)**



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 15, 29, 30	P	Ground
SUBN	2	DI	CCD substrate clock SUB input
V2N	3	DI	Vertical transfer clock 2 input
V4N	4	DI	Vertical transfer clock 4 input
V6N	5	DI	Vertical transfer clock 6 input
DVDD	6	P	Digital power supply
V5BN	7	DI	Vertical transfer clock 5B input
CH5N	8	DI	Read out clock 5 input
CH1N	9	DI	Read out clock 1 input
V1N	10	DI	Vertical transfer clock 1 input
CH2N	11	DI	Read out clock 2 input
V3AN	12	DI	Vertical transfer clock 3A input
V5AN	13	DI	Vertical transfer clock 5A input
CH3N	14	DI	Read out clock 3 input
V3BN	16	DI	Vertical transfer clock 3B input
CH4N	17	DI	Read out clock 4 input
VL	18	P	Output driver power supply
V3B	19	DO	Vertical transfer clock 3B output
V5A	20	DO	Vertical transfer clock 5A output
V3A	21	DO	Vertical transfer clock 3A output
V1	22	DO	Vertical transfer clock 1 output
VH	23	P	Output driver power supply
V5B	24	DO	Vertical transfer clock 5B output
V6	25	DO	Vertical transfer clock 6 output
V4	26	DO	Vertical transfer clock 4 output
V2	27	DO	Vertical transfer clock 2 output
SUB	28	DO	CCD substrate clock SUB output

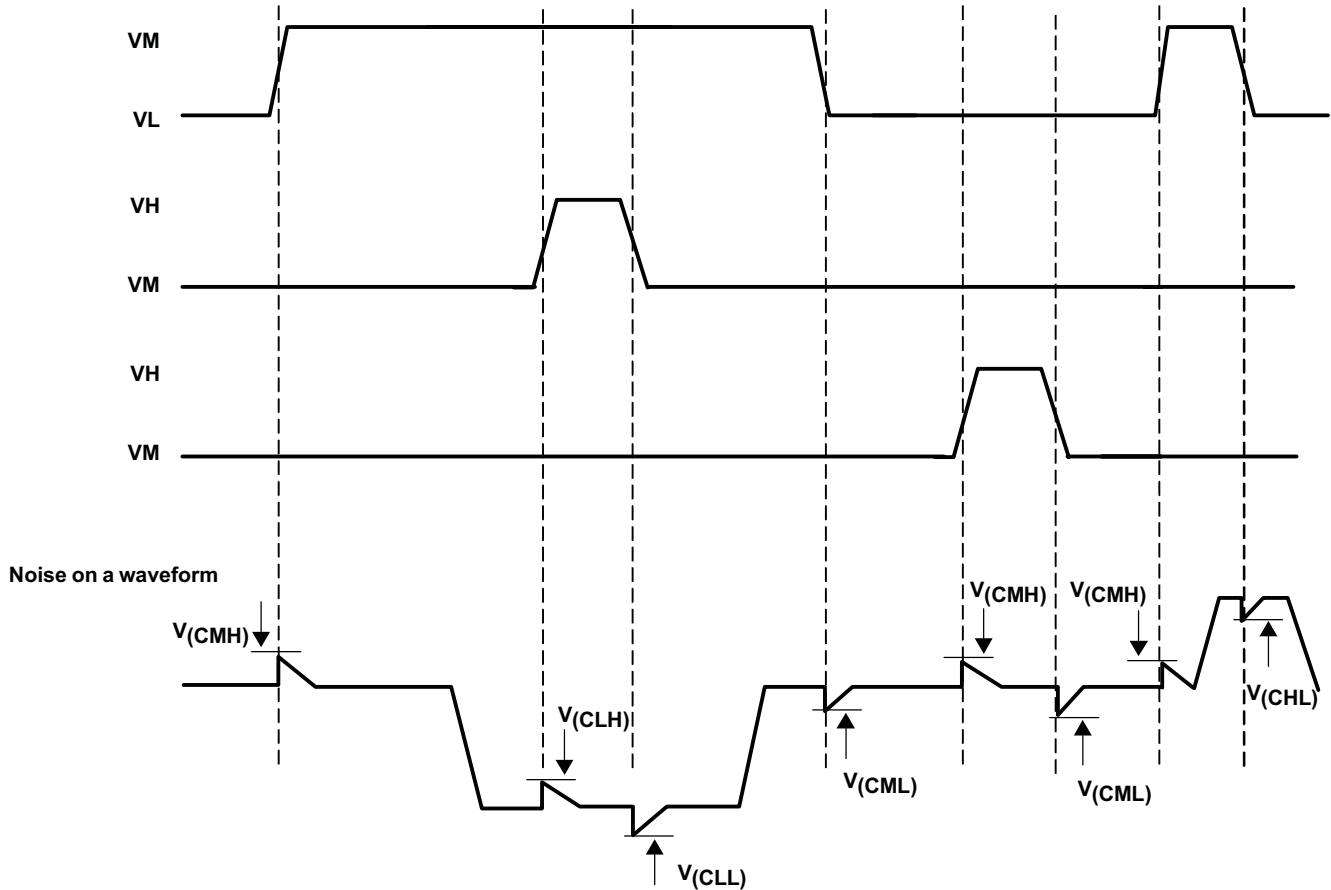
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

INPUT				OUTPUT		
V1N	CH1N			V1		
V3AN	CH2N			V3A	V2	
V3BN	CH4N	V2N		V3B	V4	
V5AN	CH3N	V4N		V5A	V6	
V5BN	CH5N	V6N	SUBN	V5B		SUBN
L	L	X	X	VH	X	X
L	H	X	X	VM	X	X
H	L	X	X	Z	X	X
H	H	X	X	VL	X	X
X	X	L	X	X	VM	X
X	X	H	X	X	VL	X
X	X	X	L	X	X	VH
X	X	X	H	X	X	VL

SWITCHING WAVEFORM



LOADING DIAGRAM

Vertical clock series resistor	R1, R2, R4, R6	60 Ω
	R3A, R5A	240 Ω
	R3B, R5B	80 Ω
Vertical clock to GND	CΦV1	1280 pF
	CΦV3A, CΦV3B	640 pF
	CΦV5A, CΦV5B	640 pF
	CΦV2, CΦV4, CΦV6	400 pF
Between vertical clock	CΦV12	510 pF
	CΦV23A, CΦV23B	50 pF
	CΦV45A, CΦV45B	50 pF
	CΦV3A4, CΦV3B4	260 pF
	CΦV5A6, CΦV5B6	260 pF
	CΦV61	100 pF
	CΦV12	510 pF
Substrate clock to GND	CΦVSUB	1000 pF
Vertical clock GND resistor	R GND	18 Ω

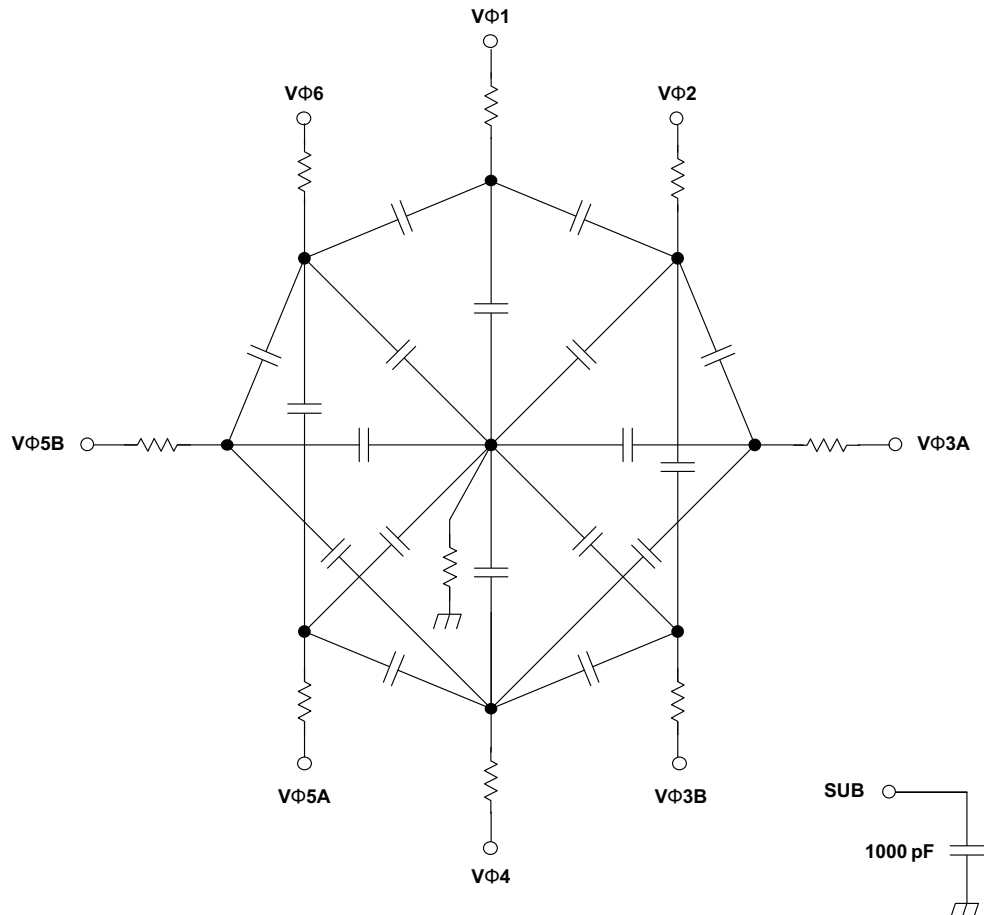


Figure 1. VSP1900 Loading Diagram

DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric shutter. The VSP1900 is composed of five 3-state and three 2-state vertical transfer channels, which support both 3 field and 2 field CCD operation. The VSP1900 contributes low power consumption and parts number reduction in the system.

OPERATION

Power On/Off Sequence

This is the same as the CCD power up sequence, when power on, VDD powers on first, VM powers on second, and VL powers on later. When powering off, VL powers off first, VH, VM powers off second, and VDD powers off later.

Vertical Transfer Signal

The VSP1900 receives signals from TG (CCD timing generator). The input signal is converted into the operating voltage levels of the CCD by the level shifter. The level shifter circuits connect to a 2-state or 3-state driver, which is connected to the CCD input pin. While using a 2-field CCD, one of the 3-state drivers is used as a 2-state driver. The CH#N pin is pulled up internally, so that the VH level does not appear on the output pin.

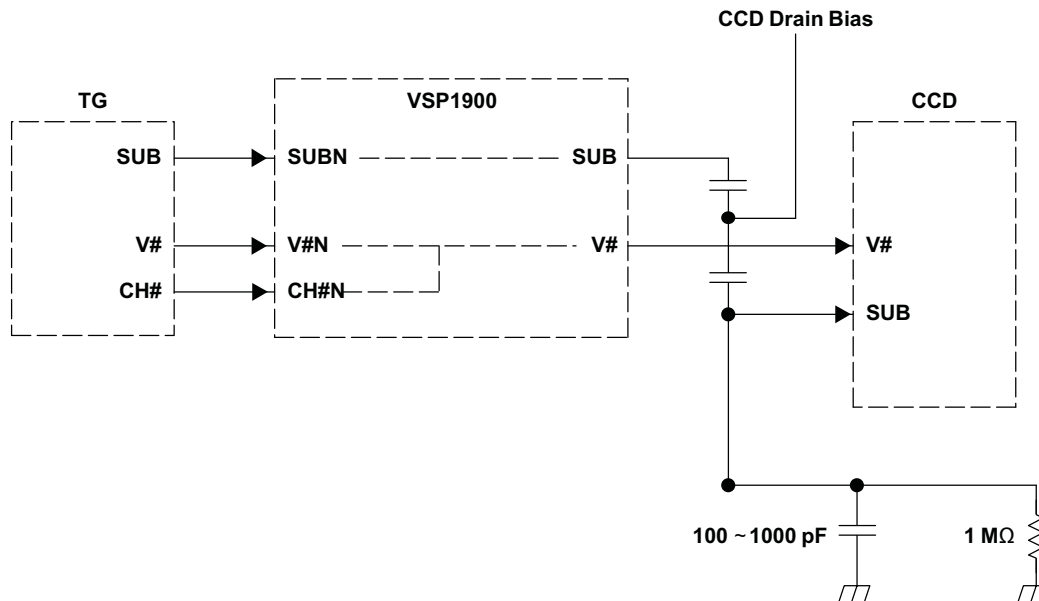


Figure 2. VSP1900 Circuit Application

REVISION HISTORY

Changes from Original (March 2003) to Revision A	Page
• Changed the last sentence of the Description From: "part number reduction in the system." To: " device count reduction in the system.	1
• Deleted the Tape and reel option from the Ordering Information Table	2
• Changed the Package temperature value From 2.35°C to 260°C	2
• Added Table Note " Specified by Design" to the MIN and MAX columns of the ELECTRICAL CHARACTERISTICS and SWITCHING CHARACTERISTICS.	3
• Changed the Truth Table	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP1900DBT	ACTIVE	TSSOP	DBT	30	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	VSP1900	Samples
VSP1900DBTG4	ACTIVE	TSSOP	DBT	30	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	VSP1900	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

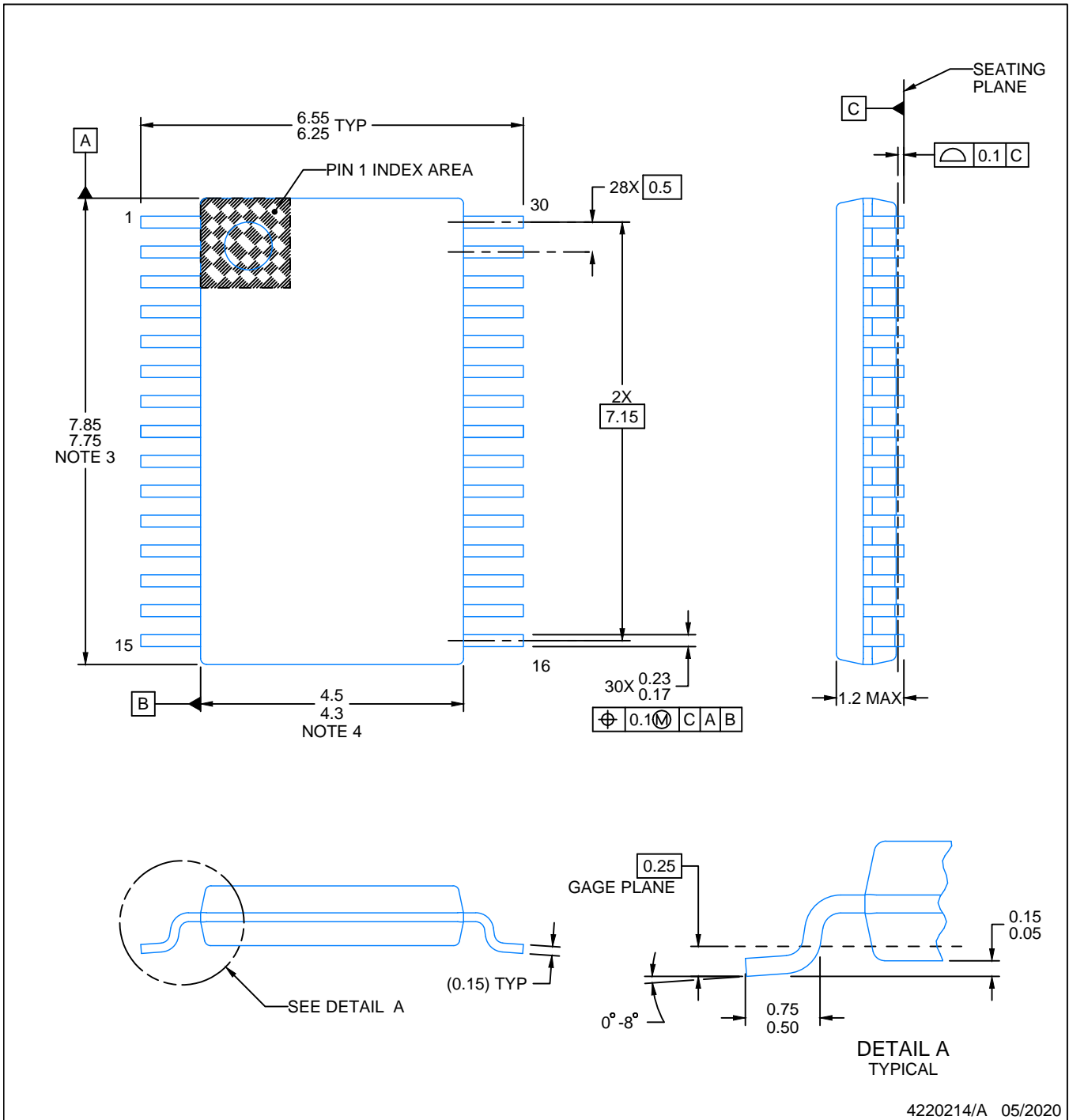
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

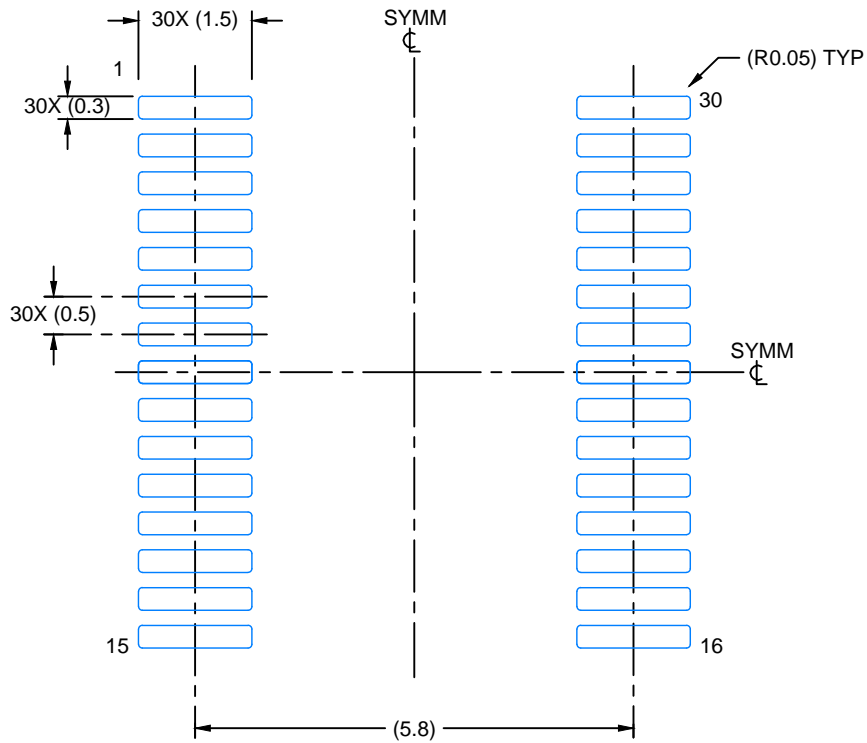
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

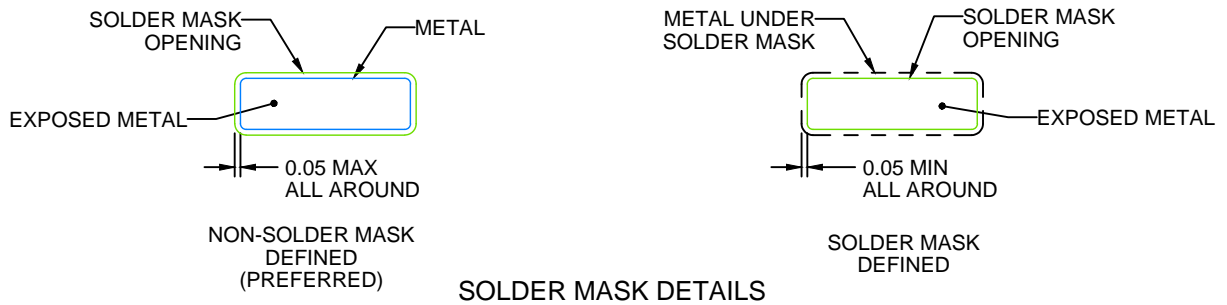
DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220214/A 05/2020

NOTES: (continued)

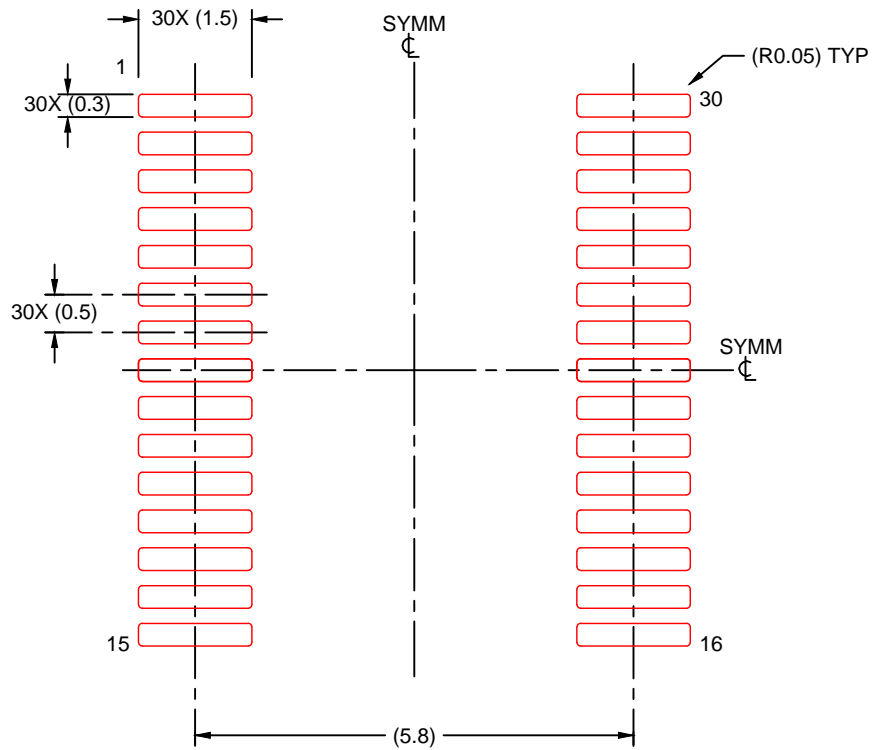
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated