12-Bit, 31-MSPS, Dual-Channel CCD ANALOG FRONT-END FOR DIGITAL COPIERS

FEATURES

- **Dual-Channel CCD Processing:**
  - **Correlated Double Sampler (CDS)**
  - **Sample-and-Hold Mode (S/H)**
  - **Digital Programmable Amplifier**
  - **CCD Offset Correction (OB Loop)**
- **High-Performance ADC:**
  - **12-Bit Resolution**
  - **INL: ±2 LSB**
  - **DNL: ±0.5 LSB**
  - **No Missing Codes Ensured**
- **High-Speed Operation:**
  - **Sample Rate: 31 MHz (max, Design Ensured)**
  - **78-dB SNR (at 0-dB Gain)**
- **Low-Power Consumption:**
  - **Low Voltage: 3.0 V to 3.6 V**
  - **Low Power: 290 mW (typ at 3.3 V)**
  - **Standby Mode: 20 mW (typ)**

APPLICATIONS

- **Copiers**
- **Scanners**
- **Facsimiles**

DESCRIPTION

The VSP5010 is a complete application-specific standard product (ASP) for charge-coupled device (CCD) line sensor applications such as copiers, scanners, and facsimiles. The VSP5010 provides two independent line-processing channels, and performs analog front-end (AFE) data processing and analog-to-digital conversion. Each channel features correlated double sampling (CDS) and sample-and-hold (S/H) processing stages, 14 analog-to-digital converter (ADC) blocks, a digital programmable gain amplifier (DPGA), and an optical black (OB) correction loop. Data are output in a 12-bit word; two-channel ADC data are multiplexed and then output.

The VSP5010 operates from a single 3.3-V supply. The device is available in an LQFP-64 package.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5010PMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

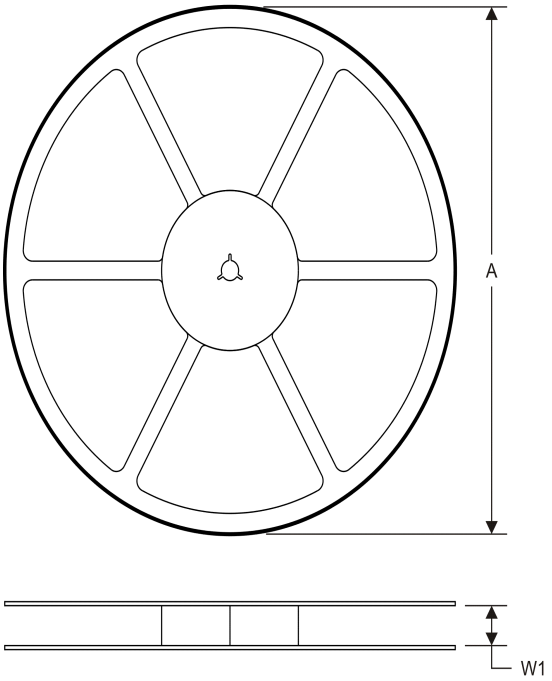
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

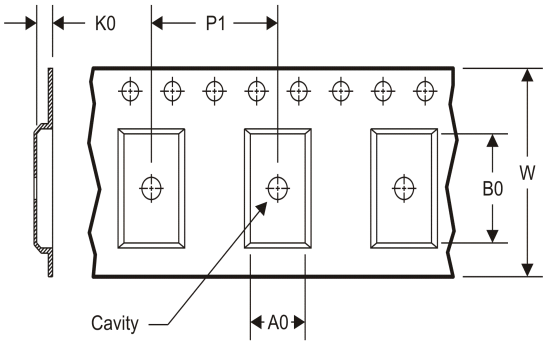
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



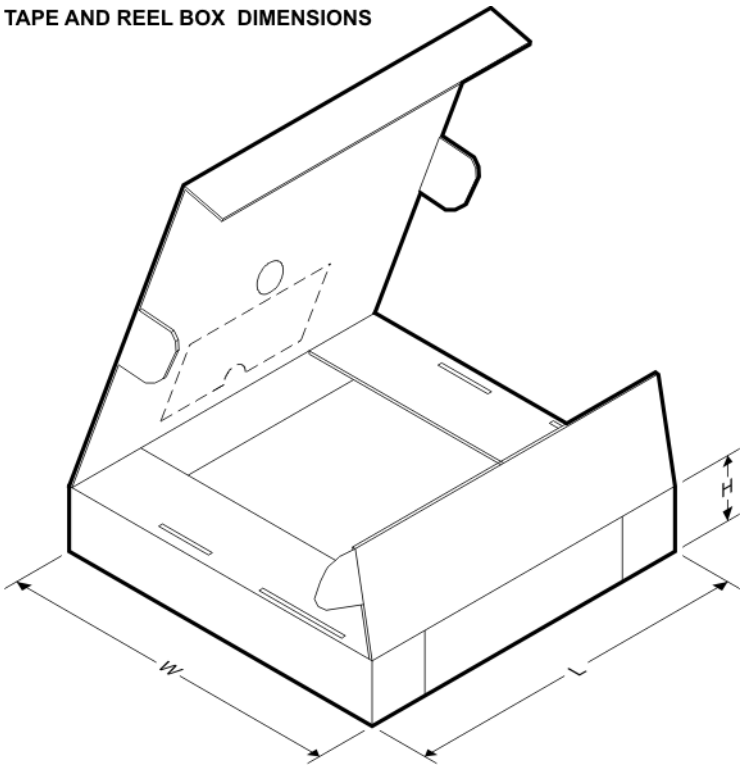
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5010PMR	LQFP	PM	64	1000	330.0	25.4	12.8	12.8	1.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

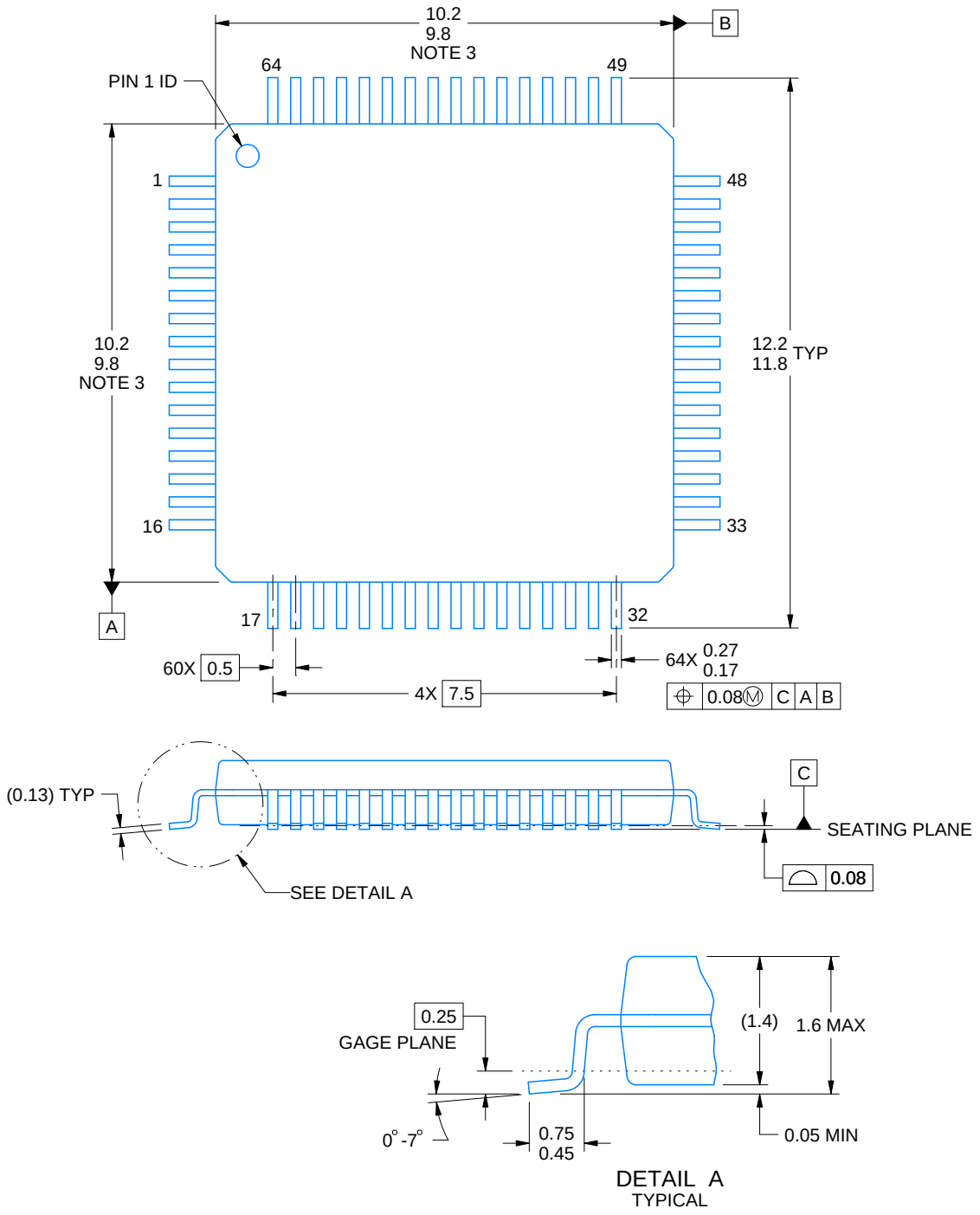
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5010PMR	LQFP	PM	64	1000	367.0	367.0	45.0

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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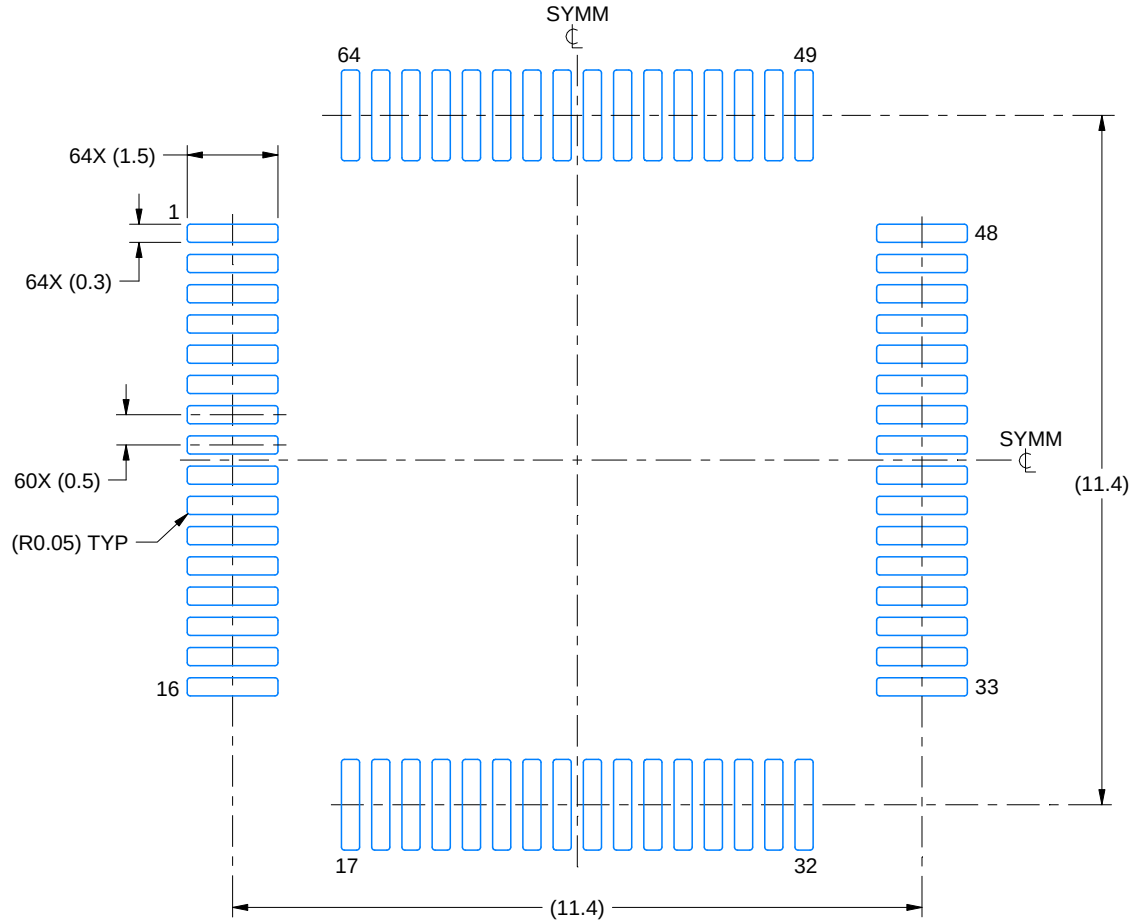
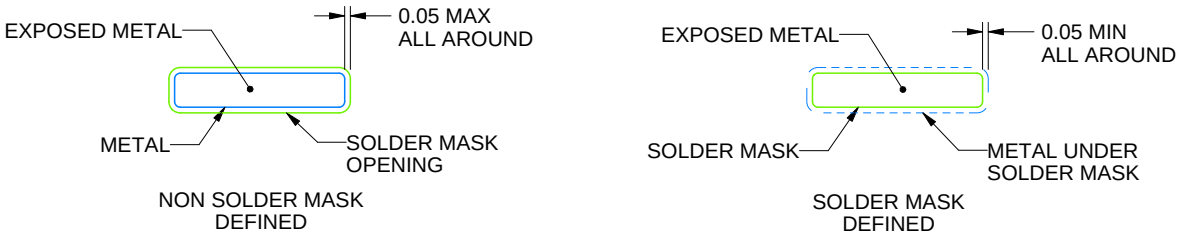
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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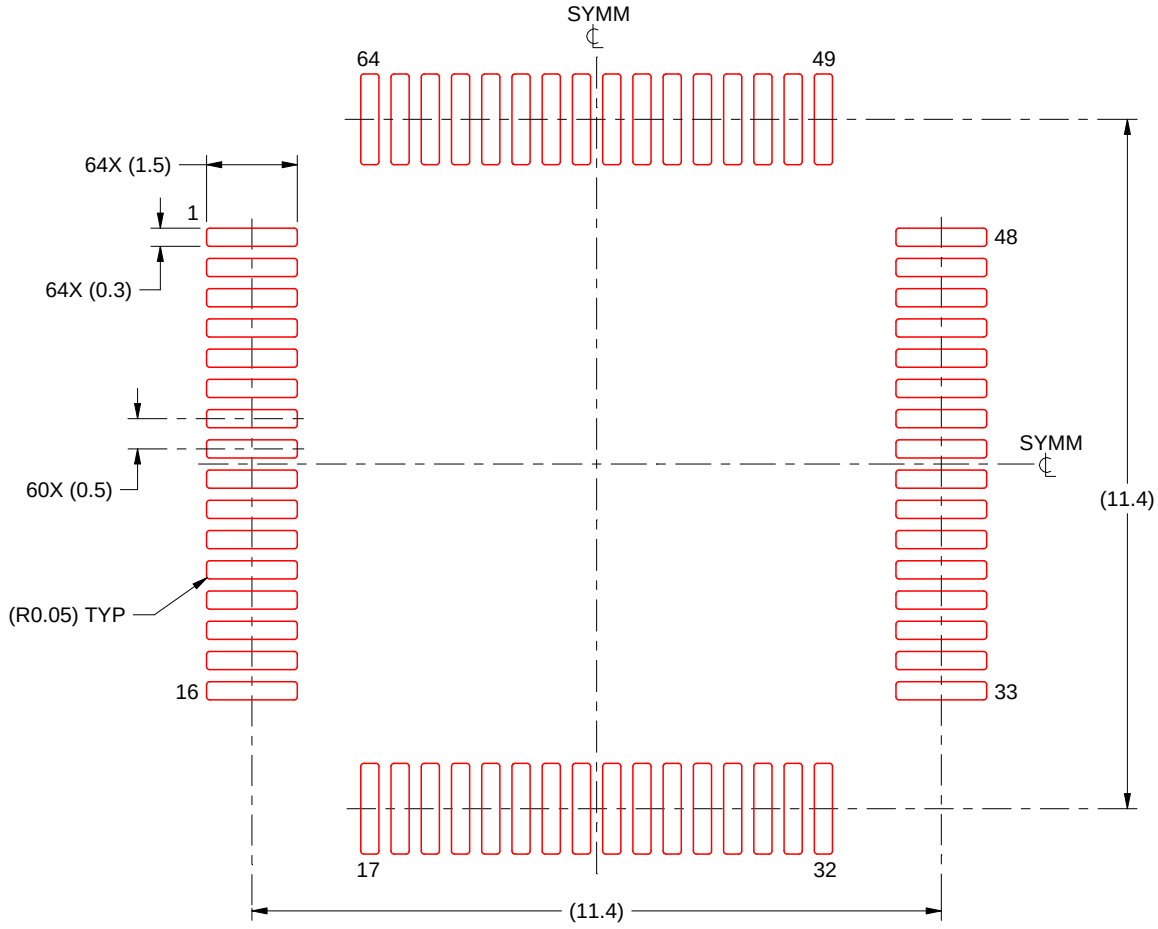
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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