AN4671
Application note

How to fine tune your SiC MOSFET gate driver to minimize losses

L. Abbatelli, C. Brusca, G. Catalisano

Introduction

Power electronics today is about the constant pursuit of efficiency improvements as well as cost and size reduction.

In this challenging power conversion scenario, silicon carbide (SiC) power switches are gaining prominence: for 1200 V power switches, silicon carbide MOSFETs are becoming an increasingly viable alternative to conventional silicon technologies. The advanced and innovative properties of wide band-gap materials help ensure that ST's SiC MOSFETs exhibit low on-state resistance*area in comparison with silicon MOSFETs, even at high temperatures, and excellent switching performance versus the best-in-class 1200 V IGBTs in all temperature ranges, thus simplifying the thermal design of power electronic systems.

With far lower switching losses than for comparable Si-based switches, SiC devices can operate at switching frequencies two to five times greater than present devices and overall system designs can also benefit from smaller and lighter passive components. The very low leakage currents boost system reliability and consistency even when subject to elevated reverse voltages or temperature increases.

This all means that the efficiency delivered by a SiC MOSFET in any application is significantly higher than silicon-based solutions, especially at high frequencies.

It is therefore crucial to drive SiC MOSFETs in such a way as to facilitate lowest possible conduction and switching losses, which is why this document explains the main principles for obtaining the best performance from ST's 1200 V SiC MOSFET in your application.

The first ST SiC MOSFET given is the 80 mΩ version (SCT30N120), the device is packaged in the proprietary HiP247™ package and features the industry's highest junction temperature rating of 200 °C. All the data reported in the present work refers to the SCT30N120.

Contents

1 How to minimize conduction losses

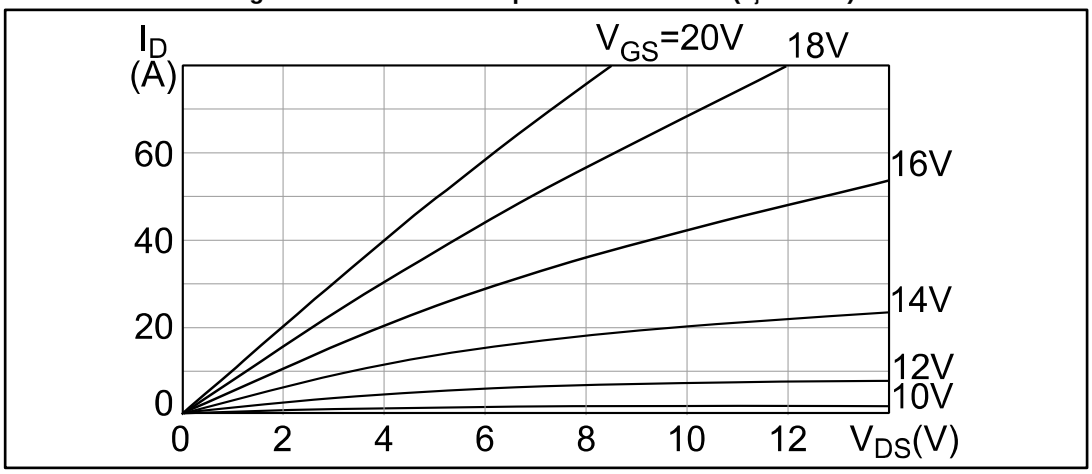
SiC MOSFETs require a higher gate voltage swing than standard super-junction MOSFETs or IGBTs. We recommend a +20 V positive bias gate drive to minimize $R_{DS(on)}$ and hence conduction losses.

It is therefore evident that SiC MOSFETs offer clear advantages over other SiC devices in terms of:

- DC current requirements – it does not require any gate current to sustain the conduction state
- simplified driving circuits – only gate resistors and a simple 0 to 20 V input waveform are needed

It is unnecessary and even undesirable to drive SiC MOSFETs with more than +20 V in the positive direction as the V_{GS} absolute maximum rating is +25 V. It is possible to go as low as +18 V, but this increases the $R_{DS(on)}$ by about 25% at 20 A, 25 °C. The possibility of using a negative bias gate voltage to completely turn-off the device is treated in the following section dedicated to the switching loss minimization.

Figure 1: SCT30N120 output characteristics (T_j = 25 °C)



2 How to minimize switching losses

SiC MOSFETs are tailored for easy-to-drive devices, able to operate at up to five times the switching frequency of comparable IGBTs, resulting in more compact, reliable and efficient designs for applications such as solar inverters, high-voltage power supplies and high efficiency drives.

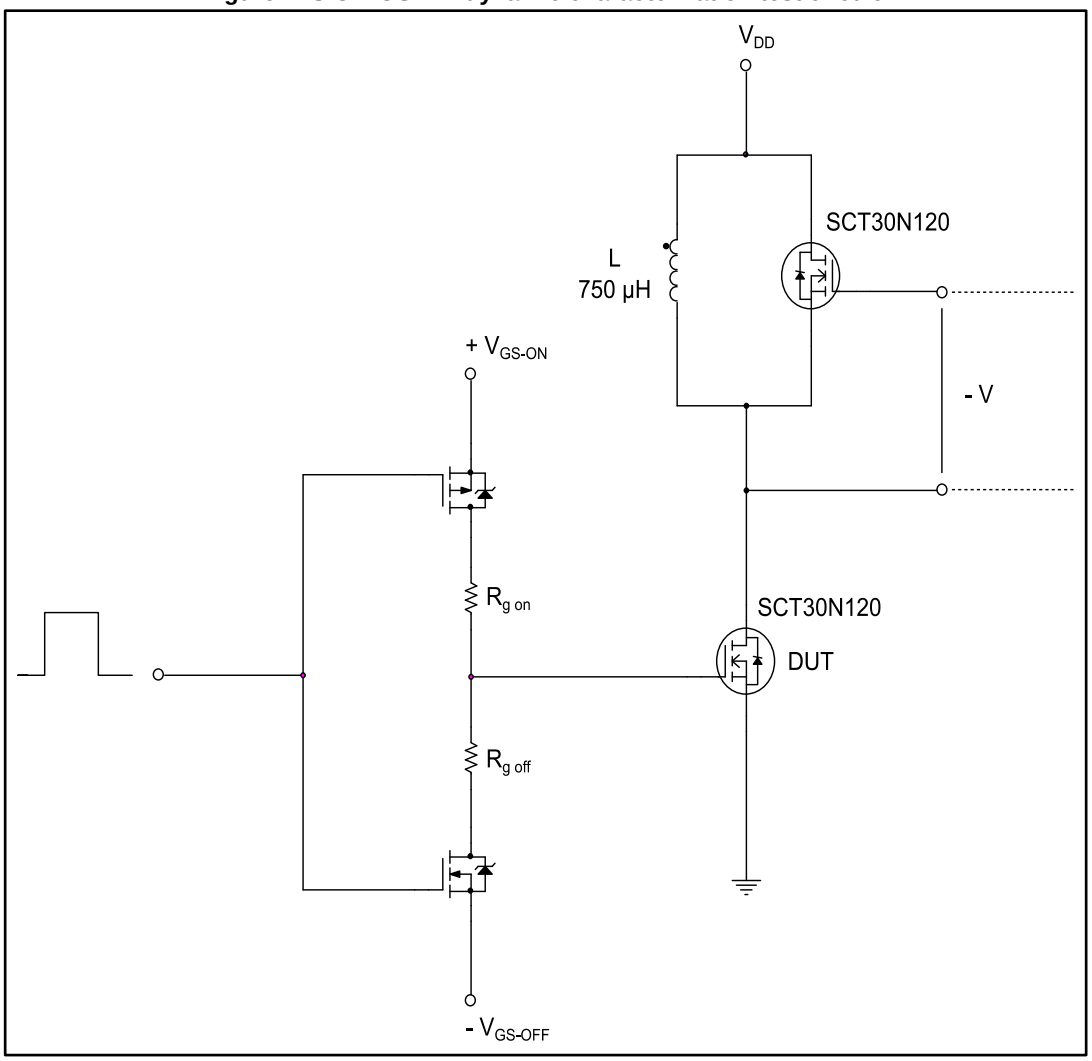
To optimize switching perfomrance, a key factor in achieving the “quantum leap” in power electronics, certain unique operating characteristics need to be understood and implemented.

The main aspects influencing switching behavior are:

- turn-off energy (E_{off}) dependence on R_g and $V_{GS\text{-}off}$ (negative bias gate voltage)
- turn-on energy (E_{on}) dependence on R_g
- Miller effect, which affects E_{on} and E_{rr} (reverse recovery energy)
- gate drive current requirements

All tests are subject to the $V_{GS\text{-}on}$ = +20 V condition for the reasons discussed in the previous section. The results regarding the above mentioned parameters can be extended to the entire SiC MOSFET family, except for gate current requirements that strongly depend on the device current rating associated with the gate charge magnitude.

Figure 2: SiC MOSFET dynamic characterization test circuit



2.1 Turn-off energy (E_{off}) dependence on R_g and V_{gs-off}

As with any majority carrier device, SiC MOSFETs have no tail, so the turn-off switching energy (E_{off}) is due to the overlap between the drain-source voltage and drain current during the voltage rise time and the current fall time.

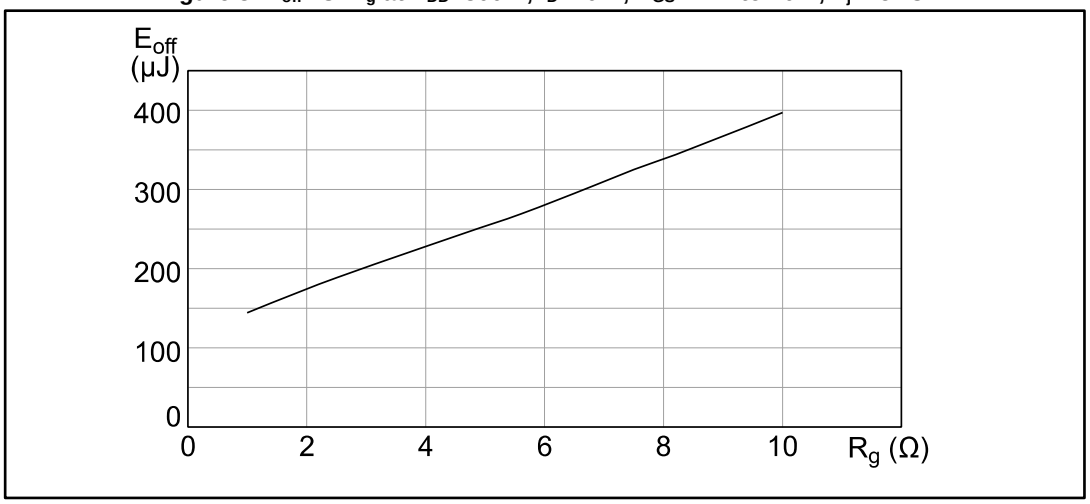
Turn-off losses inherently depend on the device itself (as opposed to turn-on switching losses, which can depend on the reverse recovery charge of an external silicon or SiC diode, as in BOOST converters and many other topologies), hence the unrivaled turn-off speed of the SiC MOSFET is a feature of this new technology that separates it from other 1200 V power actuators.

E_{off} can be lowered by draining more current from the gate, by either:

- reducing the gate resistance (R_g)
- using a negative bias gate voltage during off time

The SCT30N120 E_{off} dependence on gate resistance is illustrated below.

Figure 3: E_{off} vs. R_g at V_{DD}=800 V, I_D=20 A, V_{GS}=-2 V to 20 V, T_j=25 °C



Obviously, as the gate resistance drops, the drain-source overshoot (peak voltage exceeding the V_{DD}) increases, but the SCT30N120 exhibits only slight overshoot variation with gate resistance. The maximum V_{DS} across the MOSFET increases by only 50 V when the gate resistance moves in to the 1 to 10 Ω range, hence the voltage margin is at least 20%, even when R_g = 1 Ω. Parasitic inductance between the drain and the positive clamp voltage should be minimized.

The following electrical waveform diagrams clearly depict the voltage overshoot and E_{off} variation with R_g.

Figure 4: E_{off} at R_g=1 Ω, V_{DD}=800 V, I_D=20 A, V_{GS}=-2 V to 20 V, T_j=25 °C

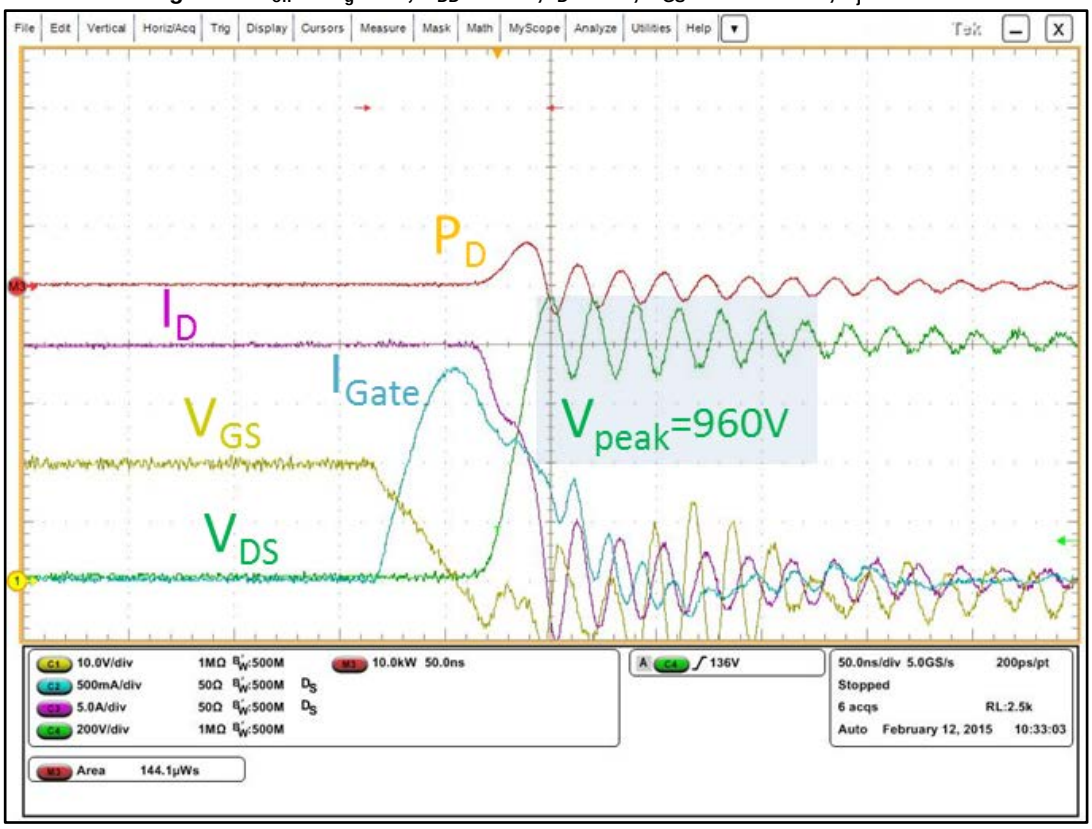
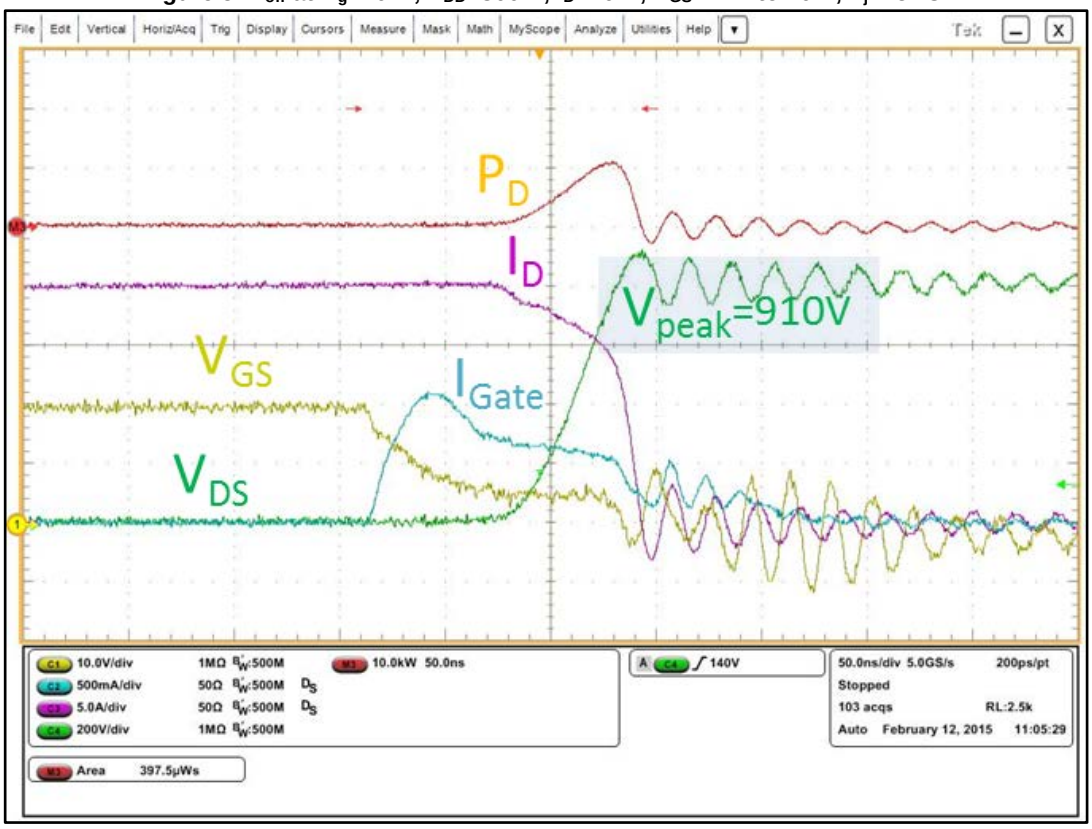


Figure 5: E_{off} at R_g=10 Ω, V_{DD}=800 V, I_D=20 A, V_{GS}=-2 V to 20 V, T_j=25 °C

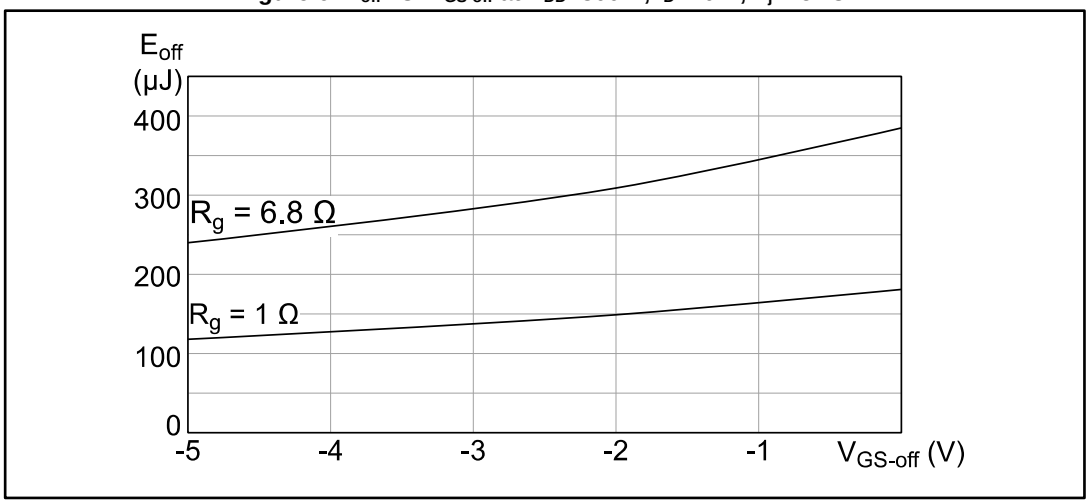


These figures demonstrate that the largest turn-off losses occur during voltage rise time, which can be significantly shortened by lowering the gate resistance. Moreover, the small gate charge needed to switch the device and the low transconductance value:

- eliminate the gate-source Miller plateau when R_g = 1 Ω (see *Figure 4*)
- give a flat V_{GS} for a period in the order of tens of nanoseconds when R_g = 10 Ω (see *Figure 5*)

The use of a negative voltage to turn off the MOSFET helps reduce turn-off losses further since it increases the voltage drop across the gate resistance, thus enabling faster charge extraction from the gate. For any gate resistance value, the E_{off} decreases by 35% to 40% when the off voltage moves from 0 V down to -5 V.

Figure 6: E_{off} vs. V_{GS-off} at V_{DD}=800 V, I_D=20 A, T_j=25 °C

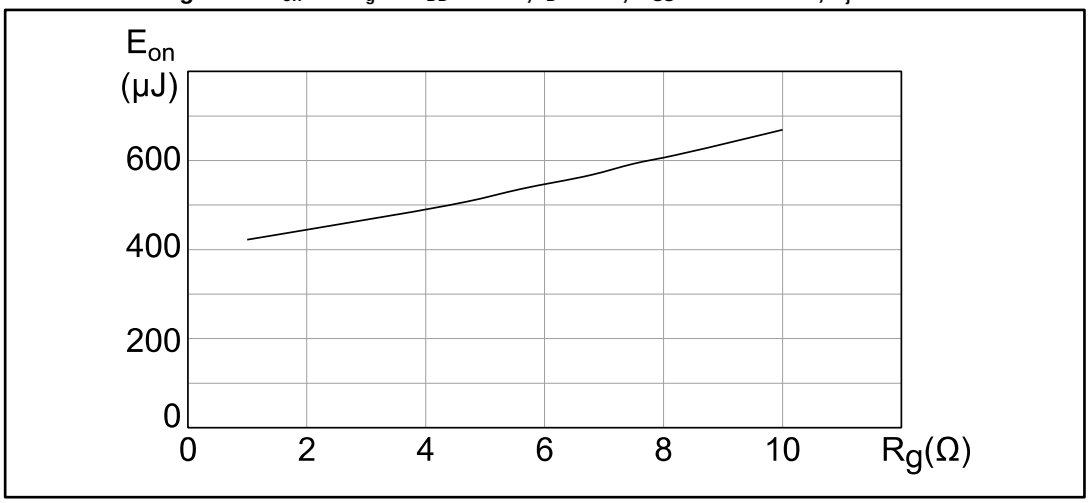


The negative bias gate drive clearly affects energy cutting during turn-off. Later, we discuss how this minimizes the Miller effect.

2.2 Turn-on energy (E_{on}) vs. R_g

Turn-on performance is also improved by reducing the gate resistance. The variation is less evident than turn-off, but when the gate resistance moves in the 1 to 10 Ω range, the turn-on energy decreases almost by 40%. The lower energy must be compatible with the di/dt limits associated with the application's EMI specifications, since di/dt significantly increases with low R_g values.

Figure 7: E_{on} vs. R_g at V_{DD}=800 V, I_D=20 A, V_{GS}=-2 V to 20 V, T_j=25 °C



The negative bias gate voltage has no impact on the turn-on energy of the stand-alone SiC MOSFET, only slightly extending the effective turn-on delay time due to the larger gate voltage swing.

The negative gate drive bias can significantly improve turn-on performance in half-bridge derived topologies (half-bridge, full-bridge, etc.) because the switch E_{on} is influenced by the Miller effect.

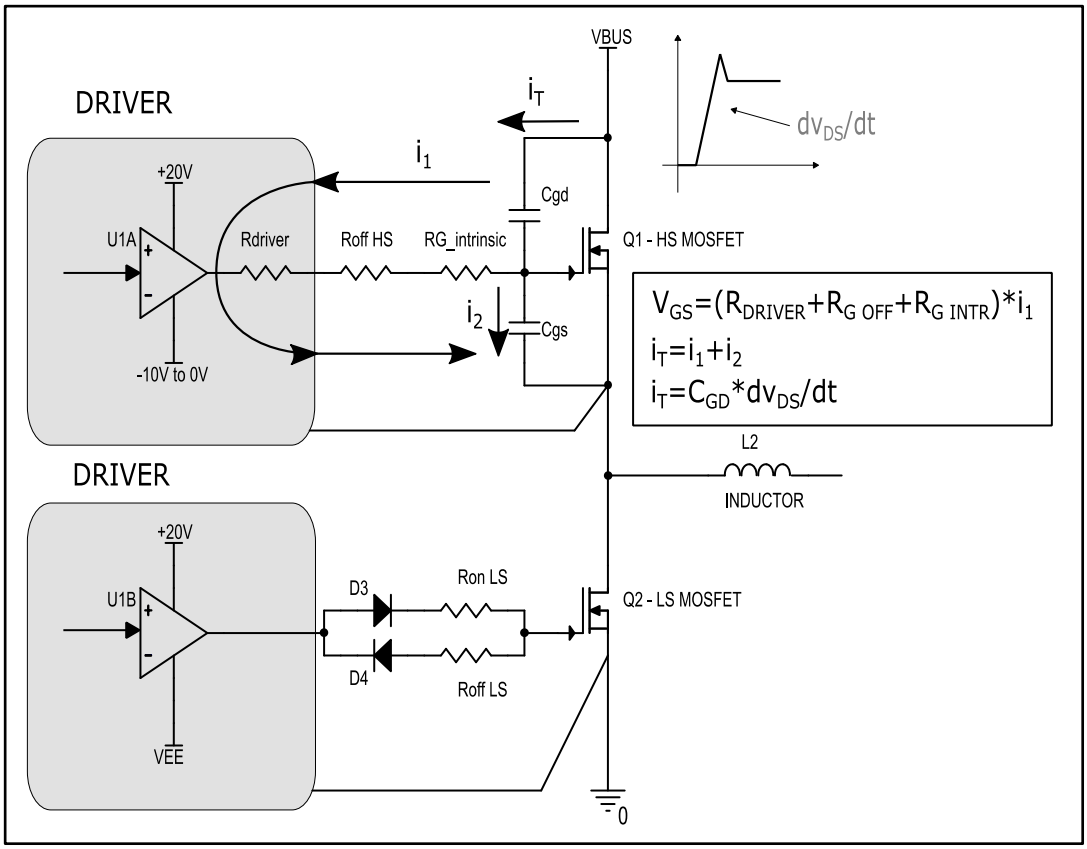
2.3 Miller effect on E_{on} and E_{rr}

A voltage change, dv_{DS}/dt, occurs across the upper switch when turning on the low-side MOSFET in a half-bridge. This creates a current which charges the parasitic capacitance C_{GD} of the upper MOSFET; this current flows via the Miller capacitance, the gate resistor and the C_{GS} (capacitances C_{GD} and C_{GS} form a capacitive voltage divider). If the voltage drop across the gate resistor exceeds the threshold voltage of the upper MOSFET, a parasitic turn-on known as 'Miller turn-on' or 'Miller effect' occurs, which can significantly impact overall leg switching losses. Parasitic turn-on may also occur when the high-side MOSFET is switched-on and a current flows through the Miller capacitance of the lower switch.

The SiC MOSFET is also affected by this phenomenon. In the test circuit below, the SCT30N120 implementing the high-side switch is kept off by a negative supply voltage applied across the gate and source (V_{off-HS} is in the 0 to -10 V range) in series with the turn-off gate resistor (R_{off-HS}).

The turn-on of the low side switch, also implemented by the SCT30N120, causes the dv_{DS}/dt across the HS switch. Gate resistors R_{off-LS} and R_{on-LS} are connected to the gate of the LS MOSFET to manage turn-off and turn-on switching. The test circuit below shows how the HS MOSFET Miller turn-on negatively affects the LS MOSFET E_{on}.

Figure 8: Miller turn-on test circuit



Analysis of the Miller turn-on phenomenon involves investigating how the low-side E_{on} and high-side E_{rr} vary with R_{off-HS}, R_{on-LS} and V_{off-HS}.

E_{rr} is the switching energy dissipated by the SiC MOSFET after the conduction of its intrinsic body diode. In the absence of the Miller effect, it is negligible due to the excellent

SiC reverse recovery characteristics. In the presence of Miller turn-on, however, the reverse recovery energy can significantly impact the global switching loss.

The Miller effect may occur in a half-bridge converter under one or more of the following conditions:

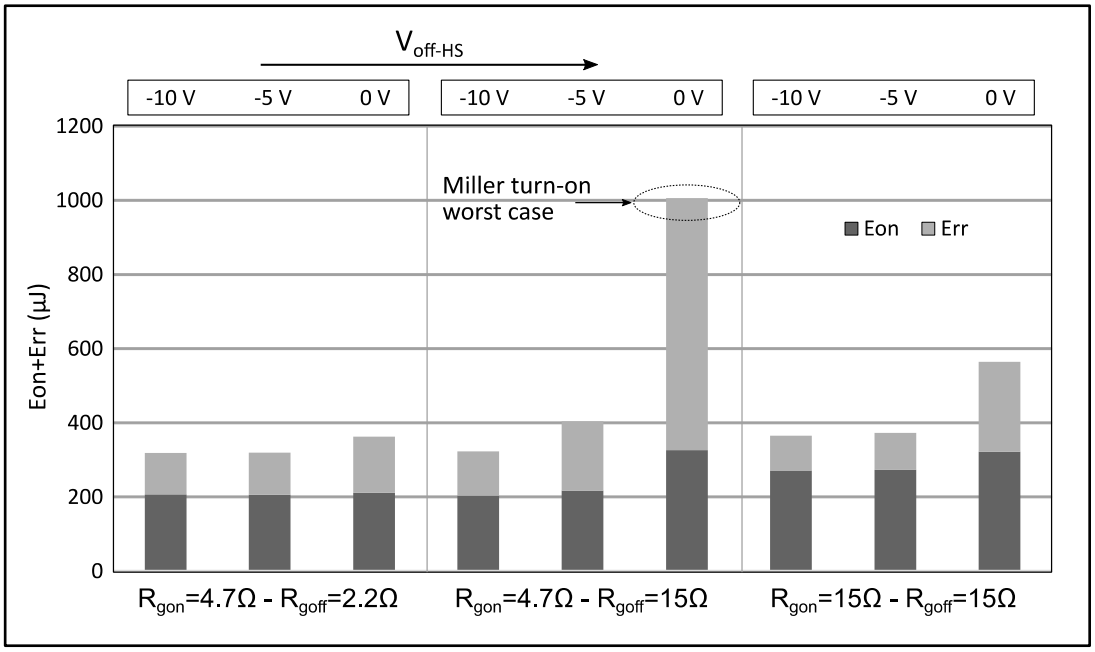
- a high dv/dt (a lower value of R_{on-LS})
- a high value of R_{off-HS}
- a high value of the intrinsic R_G of the MOSFET
- a high value of the capacitive divider C_{GD}/C_{GS}

Three combinations of R_{off-HS}, R_{on-LS} are therefore tested while V_{off-HS} moves from -10 V to 0 V:

1. R_{on-LS} = 4.7 Ω , R_{off-HS} = 2.2 Ω (best case for Miller effect)
2. R_{on-LS} = 4.7 Ω , R_{off-HS} = 15 Ω (worst case for Miller effect)
3. R_{on-LS} = R_{off-HS} = 15 Ω (intermediate case)

Do not exceed -6 V in the negative direction so as to maintain a safe margin with respect to the -10 V V_{GS} absolute maximum rating (the V_{off-HS} = -10 V scenario is included in the results for the purposes of completeness only).

Figure 9: SCT30N120 Miller turn-on test results



Therefore, at least one of the following rules must be adopted when the SCT30N120 operates in half-bridge derived topologies:

1. implement separate turn-on and turn-off paths with the correct ratio between turn-on and turn-off gate resistors: always maintain R_{g-on} >1.5 * R_{g-off}
2. use a negative off voltage in the -6 V to -4 V range to keep the MOSFET off

A small negative gate-source voltage (-2 V approx.), even if it is not mandatory, can further reduce losses and increase robustness when condition 1 (which is easier to implement) is satisfied.

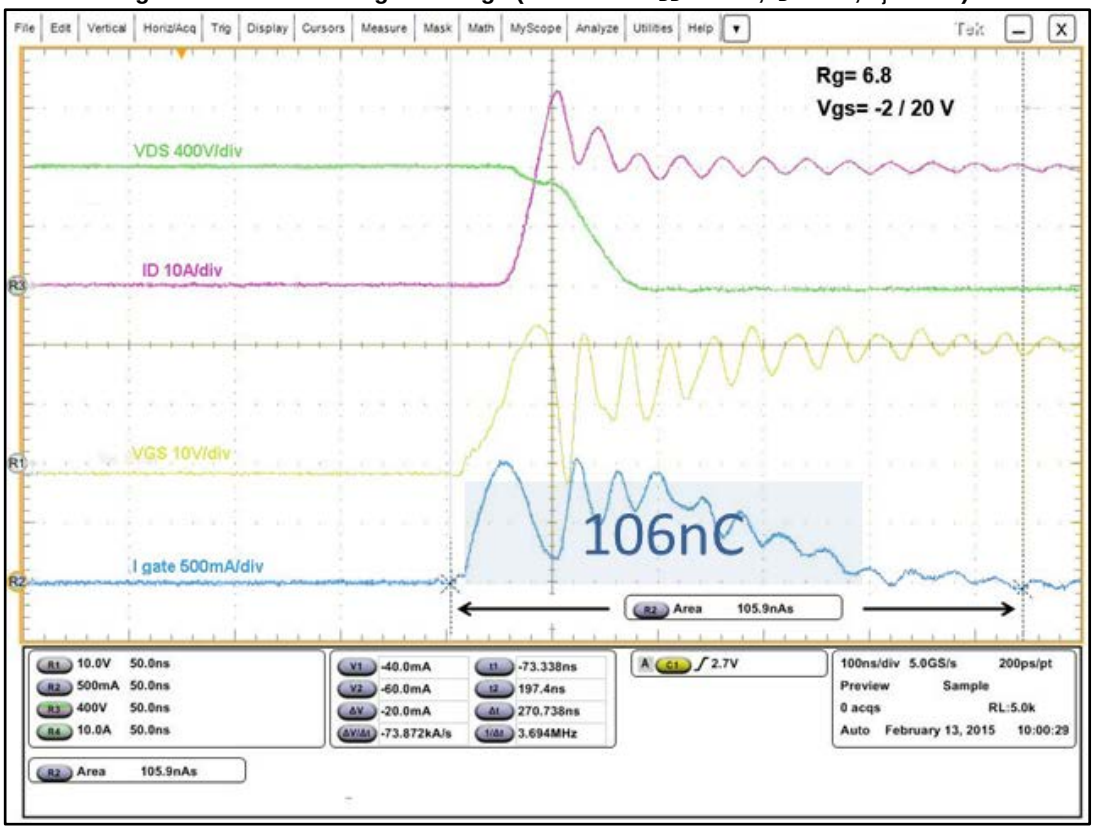
2.5 Gate drive current requirements

The gate current needed to turn a MOSFET on or off can be easily calculated using the gate charge, which can be directly read from the relevant datasheet.

The SCT30N120 total gate charge (Q_g) is typically 106 nC at V_{DD} = 800 V, I_D = 20 A, V_{GS} = -2 to 20 V.

The image below shows the total amount of charge measured as the integral of the gate current during turn-on.

Figure 10: SCT30N120 gate charge (turn-on at V_{DD}=800 V, I_D=20 A, T_j=25 °C)



The relatively small total gate charge that the driver must source and sink for any switching cycle is due to the SiC MOSFET having the lowest Figure-of-Merit $R_{ds(on)}$*Q_g of all 1200 V switches.

Inadequate driver current capability during sourcing and sinking will compromise the excellent switching performance of the SiC MOSFET because, as mentioned above, the switching energy strongly decreases with gate resistance.

For maximum switching speed, the driver must be able to source or sink the gate peak current measured at R_g = 1 Ω, $V_{GS\text{-}on}$ = +20 V and $V_{GS\text{-}off}$ = -2 V (see *Figure 2*).

The following turn-on and turn-off commutation images clearly show the driver sourcing and sinking requirements when driving the SCT30N120.

Figure 11: Gate source current at V_{DD}=800 V, I_D=20 A, R_g=1 Ω, V_{GS}=-2 V to 20 V, T_j=25 °C)

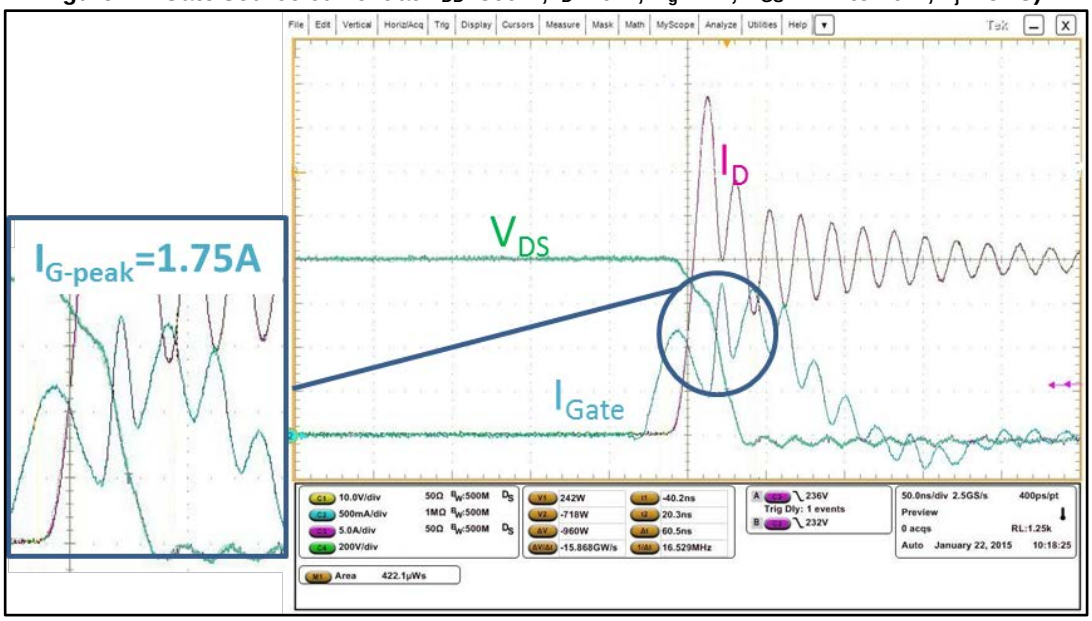
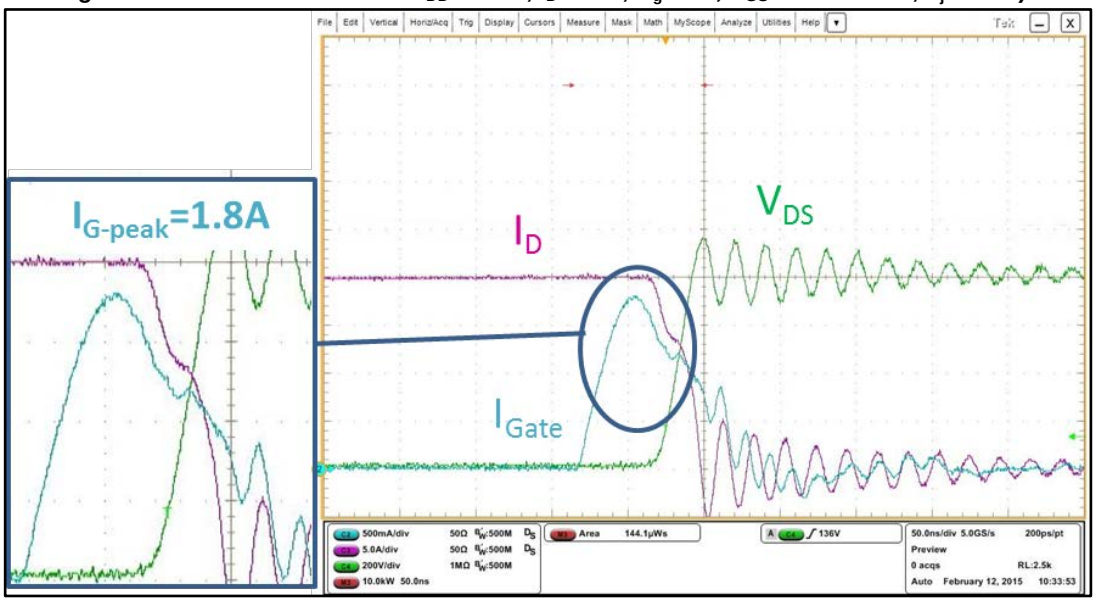


Figure 12: Gate sink current at V_{DD}=800 V, I_D=20 A, R_g=1 Ω, V_{GS}=-2 V to 20 V, T_j=25 °C)



The peak gate current is lower than 2 A in both cases; under any other test condition (higher case temperatures and lower drain current values), the gate current decreases slightly at turn-off and increases by a similar amount at turn-on.

Both the voltage across the gate resistor and the gate current are limited by the parasitic source inductance and the drain current di/dt; *Figure 11* in fact shows a high degree of ringing on the gate current caused by the oscillating I_D and the source inductance at turn-on.

Ideally, if the effect of the parasitic L were removed, we would expect the source current to exceed 2 A during turn-on, while during turn-off at R_g=1 Ω (see *Figure 12*) the gate current is quite stable and independent of the drain current.

3 Gate driver specs and implementation

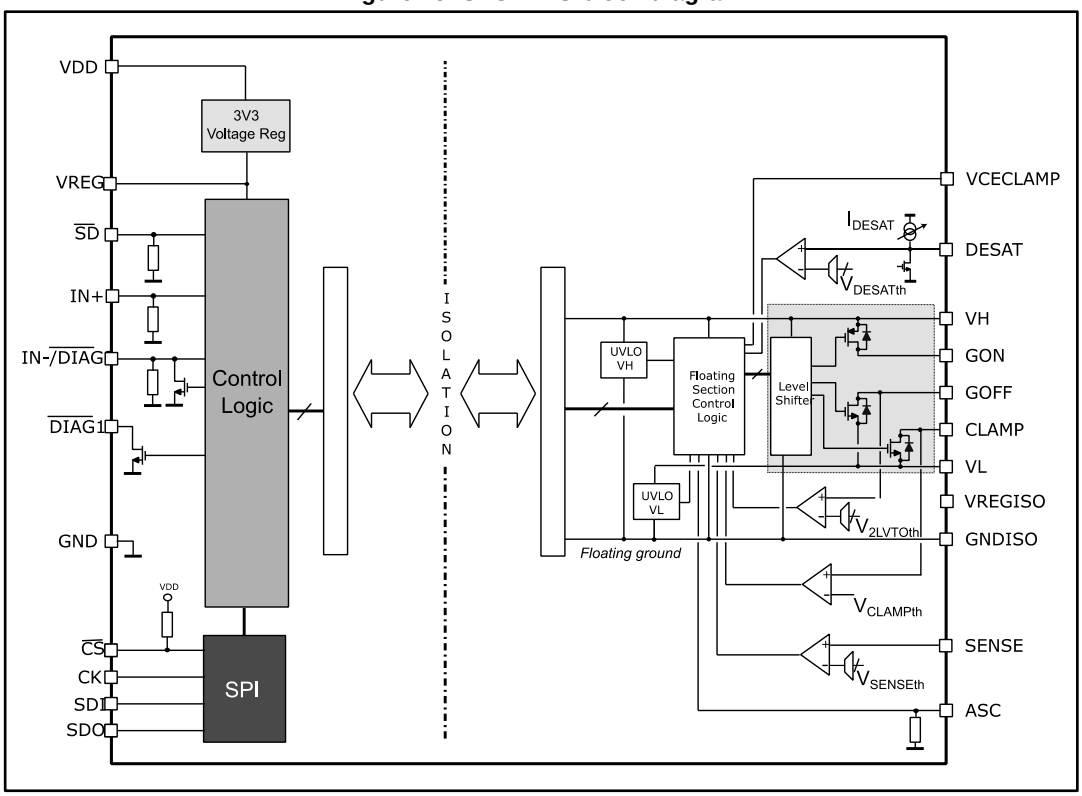
The following is a short list of the minimum gate driving requirements:

1. Dv/dt transient immunity: ±50 V/ns across the entire temperature range
   SiC MOSFETs are tailored to switch fast and operate at high frequencies, hence the intrinsic device dv/dt is higher than that observed on silicon IGBTs.
2. Minimum differential supply voltage swing: 22-28 V
   SiC MOSFETs require a higher positive gate drive voltage (+20 V) and, depending on the application, a negative OFF gate voltage in the -2 V to -6 V range. The maximum supply voltage rating of the driver must be between 22 V and 28 V depending on whether a negative OFF voltage is applied. Given that the gate charge required to switch the device is low, the higher voltage swing doesn't affect the required gate drive power.
3. The current capability (sink/source current) to drive the 1200 V,100 mΩ SCT30N120 is 2 A minimum across all temperatures
   It is required to enable the lowest achievable switching losses as the waveforms reported in the previous paragraph clearly show that the gate peak current is close to 2 A at maximum switching speeds (external gate resistor = 1 Ω).

The ideal SiC MOSFET gate driver therefore represents a 'black box' that enables the full potential of the device. It must therefore drive the gate with a higher voltage swing and larger current capability than common IGBT drivers.

The STGAP1S gapDRIVE™ is the preferred ST option to drive SiC MOSFETs among the several ST solutions available: it is a galvanically isolated single gate driver with advanced protection, configuration and diagnostic features for N-channel MOSFETs and IGBTs.

Figure 13: STGAP1S block diagram

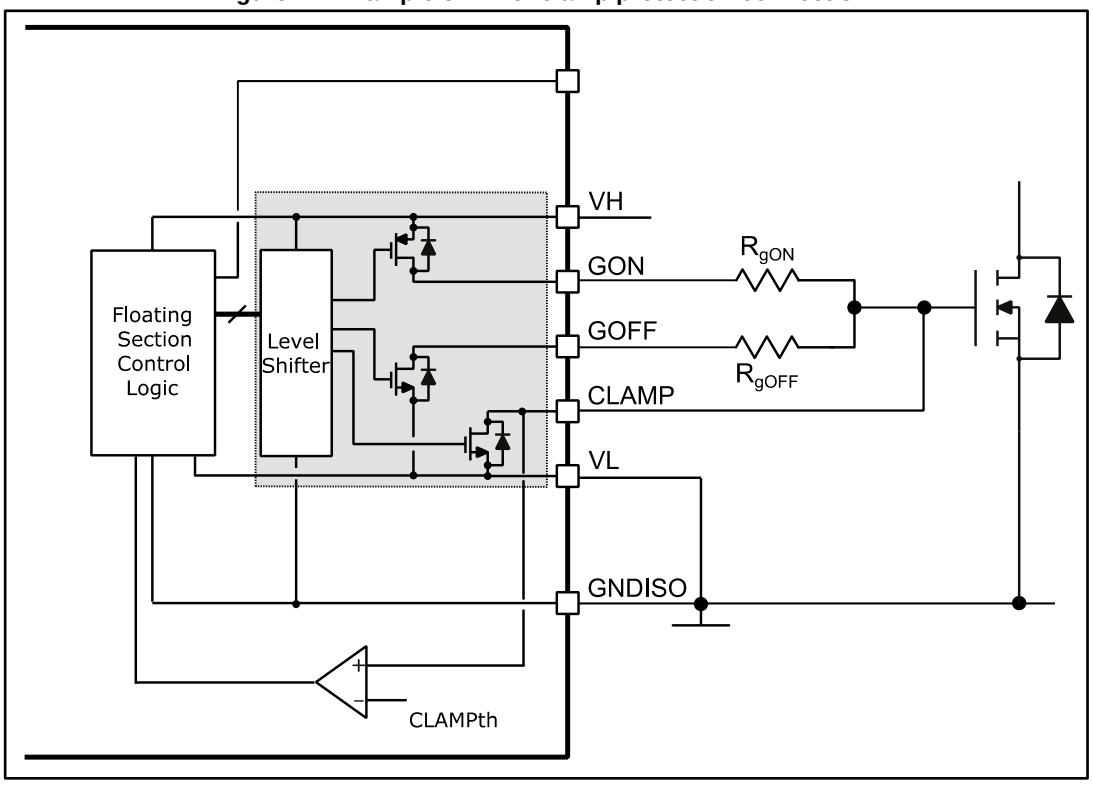


The STGAP1S driver features 5 A current capability and the output driver section provides a rail-to-rail output with the possibility of using a negative gate driver supply. Furthermore, separate sink and source outputs provide high flexibility and facilitate BoM reduction for external components.

The Miller clamp protection function is included to control the Miller current during power stage switching in half-bridge configurations. When the power switch is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur due to the C_{GD} capacitance when the other switch in the same leg is being turned on.

During the turn-off period, the switch gate is monitored via the CLAMP pin. The CLAMP switch is activated when gate voltage drops below the voltage threshold $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the VL pin, see the figure below.

Figure 14: Example of Miller clamp protection connection



4 References

1. 1200 V SiC MOSFET and N-off SiC JFET performances and driving in high power-high frequency power converter – Bettina Rubino, Luigi Abbatelli, Giuseppe Catalisano, Simone Buonomo, PCIM Europe 2013
2. Direct Comparison among different technologies in Silicon Carbide - Bettina Rubino, Michele Macauda, Massimo Nania, Simone Buonomo
3. Direct Comparison of Silicon and Silicon Carbide Power Transistors in High-Frequency Hard-Switched Applications - John S. Glaser, Jeffrey J. Nasadoski, Peter A. Losee, Avinash S. Kashyap, Kevin S. Matocha, Jerome L.
4. SCT30N120 datasheet
5. STGAP1S datasheet

5 Revision history

Table 1: Document revision history

Date	Revision	Changes
02-Apr-2015	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.