

**OCTAL  $\pm 100V$  1.8A 3-LEVEL  
ULTRASOUND PULSER**
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Rev.2.0\_01

The ABLIC Inc. HDL6V5583 is an octal, high-voltage, high-speed fully-integrated pulser for medical ultrasound imaging applications. The HDL6V5583 consists of logic interface, level translators, MOSFET gate drive buffers with embedded/external-selectable floating voltage regulators, and high-voltage, high-current MOSFETs for pulsing and active ground clamping for each channel. The HDL6V5583 is pin-compatible with HDL6V5582/5583E.

**Functions**

- 8-channel, 3-level pulser with active ground clamping with 2-input per channel

**Features**

- 0 to  $\pm 100V$  output voltage
- $\pm 1.8A$  source and sink peak current for pulsing without output blocking high-voltage (HV) diodes
- $\pm 1.0A$  source and sink peak current for active ground clamping with output blocking HV diodes
- $500\Omega$  ( $\pm 0.05A$ ) active output termination working with active ground clamping
- Embedded/external-selectable floating voltage regulators to the gate drive buffers
- Input data synchronization with a clock signal (user-selectable)
- Integrated noise-cut low-voltage (LV) diodes
- Up to 20MHz operation frequency (@ $\pm 60V$  output, 220pF load)
- 1.8V to 5V CMOS logic interface
- 4-mode output drive current control for power saving
- Thermal protection
- Power supply sequence free
- Latch-up free, lower crosstalk between channels by SOI CMOS technology
- 52-lead 8mm x 8mm QFN package (RoHS compliant)
- Pin-compatible with HDL6V5582/83E

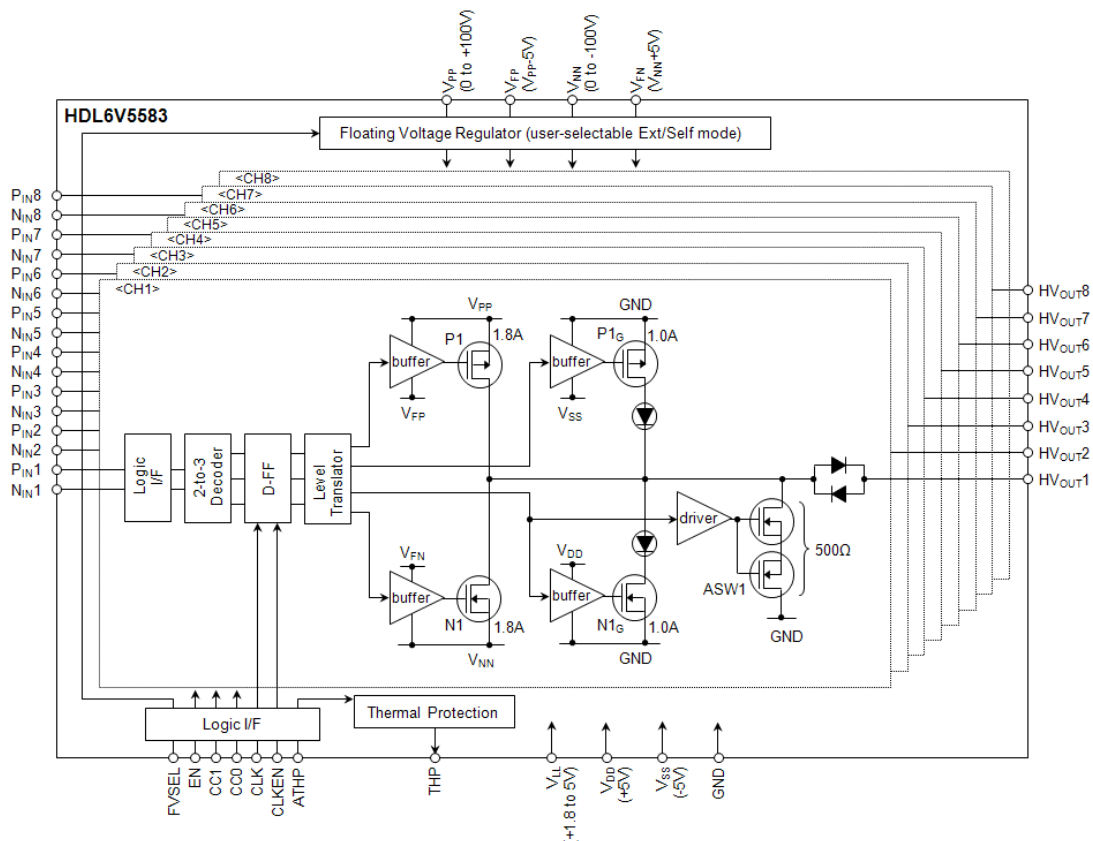


Fig.1 Block diagram

## 1. Absolute Maximum Ratings

T<sub>A</sub>=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply	V <sub>LL</sub>	-0.4 to +7	V	
2	Positive logic and level translator supply	V <sub>DD</sub>	-0.4 to +7	V	
3	Negative logic and level translator supply	V <sub>SS</sub>	-7 to +0.4	V	
4	Positive high voltage supply	V <sub>PP</sub>	-0.5 to +105	V	
5	Negative high voltage supply	V <sub>NN</sub>	-105 to +0.5	V	
6	Differential high voltage supply	V <sub>PP</sub> - V <sub>NN</sub>	+210	V	
7	High voltage outputs (x=1~8)*	HV <sub>OUTX</sub>	-105 to +105	V	
8	Gate drive buffer voltages	(V <sub>PP</sub> - V <sub>FP</sub> ), (V <sub>FN</sub> - V <sub>NN</sub> )	-0.4 to +7	V	FVSEL=0
9	THP (THermal Protection) output	THP	-0.4 to +7	V	
10	All logic input voltages (x=1~8)	P <sub>INX</sub> , N <sub>INX</sub> , EN, CLK, CLKEN, CC1, CC0, ATHP, FVSEL	-0.4 to +7	V	
11	Operating junction temperature	T <sub>Jop</sub>	-20 to +150	°C	
12	Storage temperature	T <sub>STG</sub>	-55 to +150	°C	
13	Maximum power dissipation	P <sub>Dmax</sub>	4	W	

Note: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

## 2. Operating Supply Voltages, Conditions, and Circuits (Recommended)

### 2.1 Operating Supply Voltages and Conditions

Table 2 Recommended Operating Supply Voltages and Conditions

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic voltage supply	V <sub>LL</sub>	2.4	2.5 to 5	V <sub>DD</sub>	V	Clock mode(≤80MHz)
			2.6	2.7 to 5	V <sub>DD</sub>	V	Clock mode(≤100MHz)
			1.7	1.8 to 5	V <sub>DD</sub>	V	Transparent mode
2	Positive low voltage supply	V <sub>DD</sub>	4.75	5	5.25	V	
3	Negative low voltage supply	V <sub>SS</sub>	-5.25	-5	-4.75	V	
4	Positive high voltage supply	V <sub>PP</sub>	0	-	100	V	
5	Negative high voltage supply	V <sub>NN</sub>	-100	-	0	V	
6	Differential high voltage supply	V <sub>PP</sub> - V <sub>NN</sub>	0	-	200	V	
7	P-ch floating gate drive voltage supply	V <sub>FP</sub>	V <sub>PP</sub> -5.25	V <sub>PP</sub> -5	V <sub>PP</sub> -4.75	V	FVSEL=0
8	N-ch floating gate drive voltage supply	V <sub>FN</sub>	V <sub>NN</sub> +4.75	V <sub>NN</sub> +5	V <sub>NN</sub> +5.25	V	FVSEL=0
9	High-level logic input voltage	V <sub>IH</sub>	0.8V <sub>LL</sub>	-	V <sub>LL</sub>	V	
10	Low-level logic input voltage	V <sub>IL</sub>	0	-	0.2V <sub>LL</sub>	V	
11	IC substrate voltage *	V <sub>SUB</sub>	-	0	-	V	
12	Slew rate limit of V <sub>PP</sub> , V <sub>NN</sub>	SR <sub>MAX</sub>	-	-	25	V/ms	
13	Operating free-air temperature	T <sub>A</sub>	0	25	75	°C	

Note: \* The package exposed pad internally connected to the chip substrate must be soldered to the ground.

## 2.2 Power-Up/Down Sequence

Power-Supply Sequence is not required.

## 2.3 Application Circuits

(a) EMBEDDED floating voltage supplies (FVSEL=1)

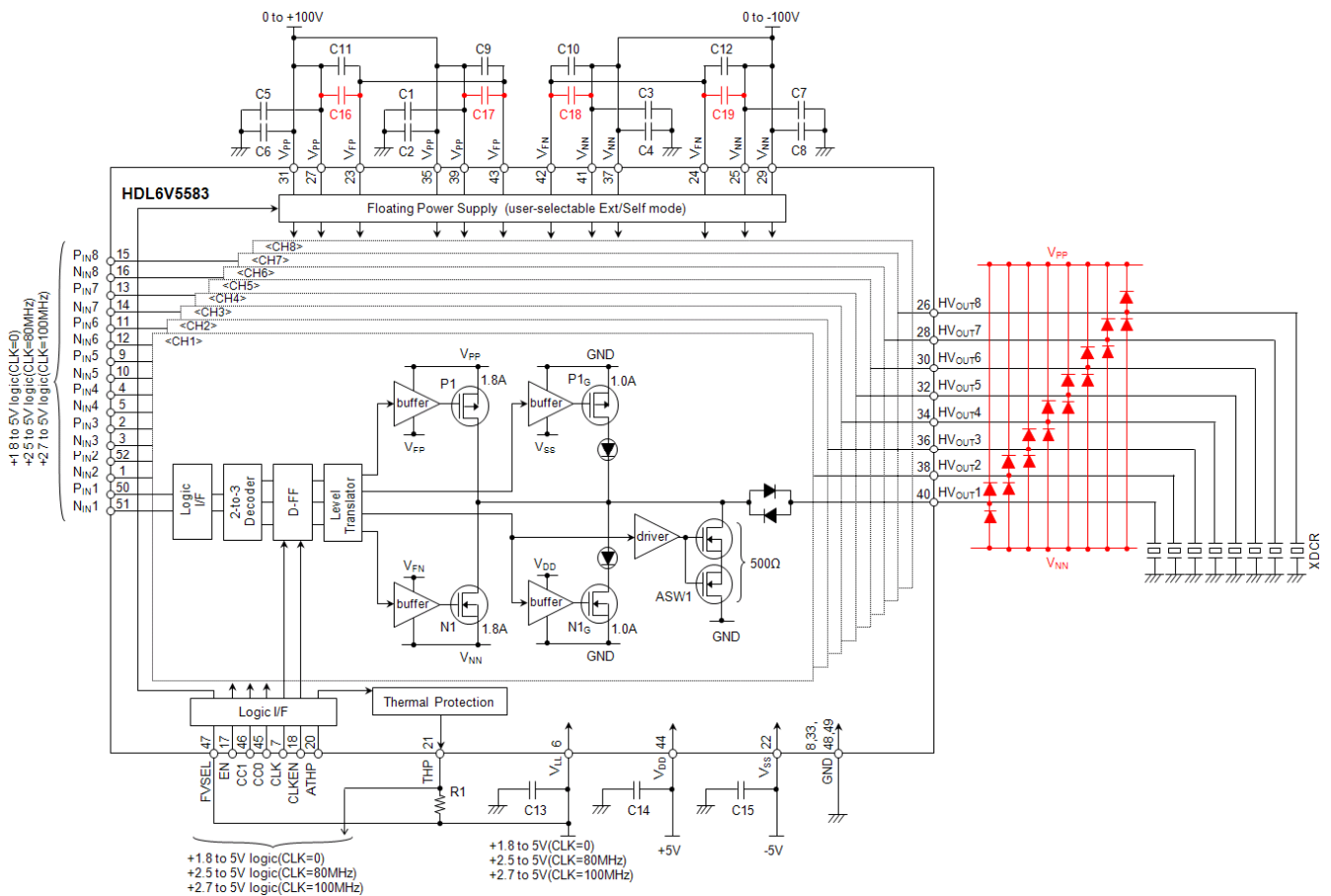


Fig. 2-(a) Typical Application Circuit-1

Note:

1. High-voltage power supply pins,  $V_{PP}/V_{NN}$ , can draw fast transient currents up to  $\pm 1.8A$ . Therefore, ceramic capacitors of over 200V 0.1 $\mu F$  to 1 $\mu F$  (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1 $\mu F$  to 1 $\mu F$  (C13~15) should also be connected close to the low-voltage power supply pins,  $V_{LL}/V_{DD}/V_{SS}$ .
2. Ceramic capacitors of over 15V 100nF (C9~12) and over 15V 10 $\mu F$  (C16~19) should be connected between each floating voltage pin ( $V_{FP}/V_{FN}$ ) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between  $HV_{OUTX}$  and  $V_{PP}/V_{NN}$  as shown in Fig.2-(a) are strongly recommended to mitigate excessive voltage overshoot caused by a reflection from a probe.

2.3 Application Circuits (Cont.)

(b) EXTERNAL floating voltage supplies (FVSEL=0)

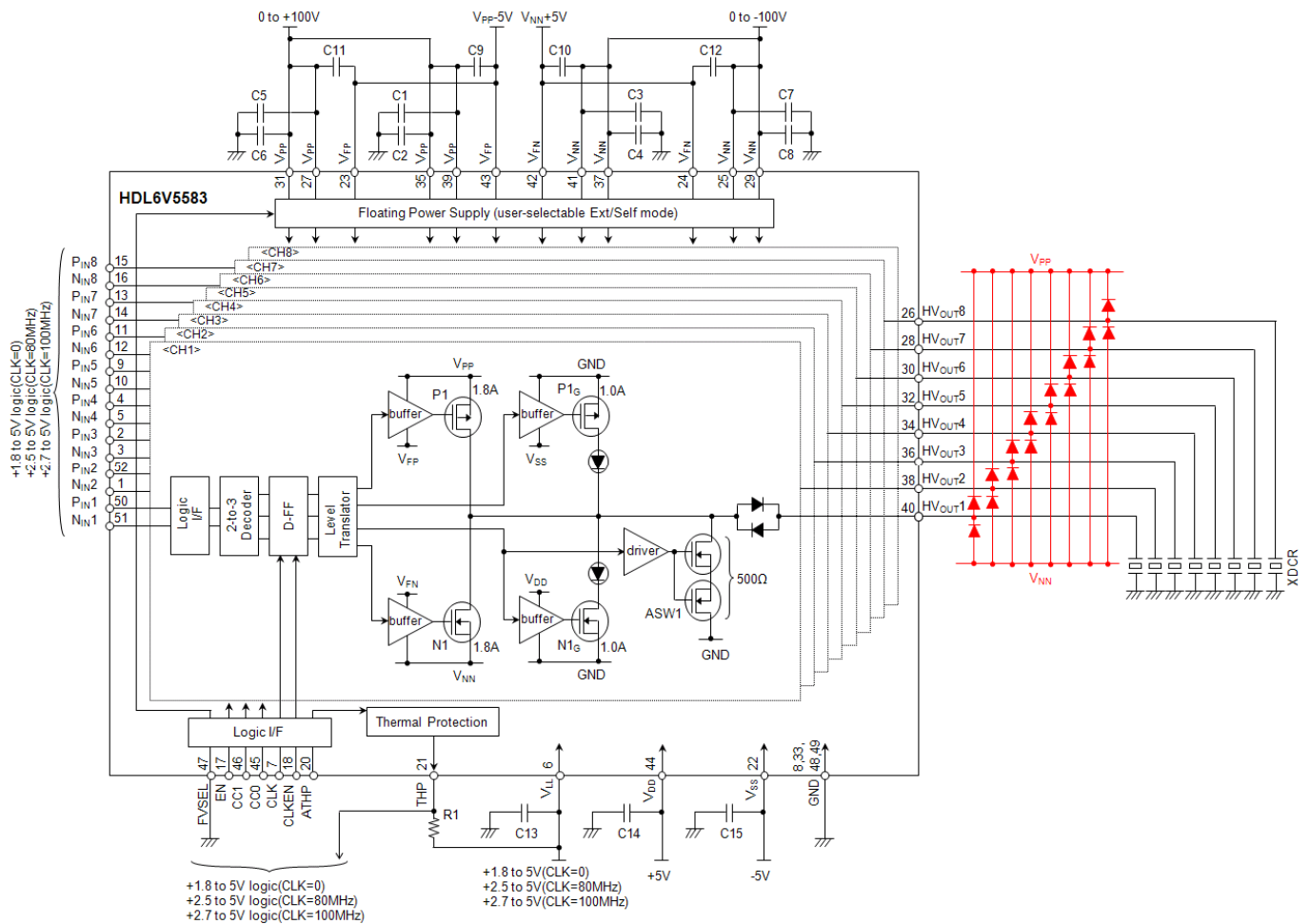


Fig. 2-(b) Typical Application Circuit-2

Note:

1. High-voltage power supply pins, V<sub>PP</sub>/V<sub>NN</sub>, can draw fast transient currents up to ±1.8A. Therefore, ceramic capacitors of over 200V 0.1μF to 1μF (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1μF to 1μF (C13~15) should also be connected close to the low-voltage power supply pins, V<sub>LL</sub>/V<sub>DD</sub>/V<sub>SS</sub>.
2. Ceramic capacitors of over 15V 1μF to 2.2μF (C9~12) should be connected between each floating voltage pin (V<sub>FP</sub>/V<sub>FN</sub>) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between HV<sub>OUTX</sub> and V<sub>PP</sub>/V<sub>NN</sub> as shown in Fig.2-(b) are strongly recommended to mitigate excessive voltage overshoot caused by a reflection from a probe.

### 3. Electrical Characteristics

#### 3.1 FVSEL=1 (EMBEDDED floating voltage supplies)

##### 3.1.1 Clock Mode (CLKEN=0)

#### DC Characteristics

Table 3 DC Characteristics (Embedded FV, Clock mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=100MHz, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	$I_{IH}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	$\mu A$	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	$I_{IL}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , CLK, ATHP
			-	66	-	$\mu A$	EN, CC1, CC0, CLKEN, FVSEL 50kΩ internal pull-up resistor
3	Input logic capacitance	$C_{IN}$	-	2	-	pF	-
4	$V_{LL}$ current	$I_{LLQD}$	-	1.0	-	mA	Quiescent current-1
5	$V_{DD}$ current	$I_{DDQD}$	-	14	-	mA	EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$
6	$V_{SS}$ current	$I_{SSQD}$	-	0.15	-	mA	
7	$V_{PP}$ current	$I_{PPQD}$	-	0.03	-	mA	
8	$V_{NN}$ current	$I_{NNQD}$	-	0.03	-	mA	
9	$V_{LL}$ current	$I_{LLQE}$	-	1.1	-	mA	Quiescent current-2
10	$V_{DD}$ current	$I_{DDQE}$	-	18	-	mA	EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$ $P_{INX}=1$ , $N_{INX}=1$ (x=1~8)
11	$V_{SS}$ current	$I_{SSQE}$	-	5.0	-	mA	
12	$V_{PP}$ current	$I_{PPQE}$	-	0.20	-	mA	
13	$V_{NN}$ current	$I_{NNQE}$	-	0.20	-	mA	
14	$V_{LL}$ current	$I_{LLPW}$	-	1.1	-	mA	Operating current-1
15	$V_{DD}$ current	$I_{DDPW}$	-	18	-	mA	8-channel active Bipolar 1-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ EN=0, Current mode=4
16	$V_{SS}$ current	$I_{SSPW}$	-	7.6	-	mA	
17	$V_{PP}$ current	$I_{PPPW}$	-	1.2	-	mA	
18	$V_{NN}$ current	$I_{NNPW}$	-	1.8	-	mA	
19	$V_{LL}$ current	$I_{LLCW4}$	-	1.2	-	mA	Operating current-2
20	$V_{DD}$ current	$I_{DDCW4}$	-	43	-	mA	8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, $V_{PP}/V_{NN}=\pm 5V$ EN=0
21	$V_{SS}$ current	$I_{SSCW4}$	-	33	-	mA	
22	$V_{PP}$ current	$I_{PPCW4}$	-	178	-	mA	
23	$V_{NN}$ current	$I_{NNCW4}$	-	174	-	mA	
24	$V_{LL}$ current	$I_{LLCW3}$	-	1.2	-	mA	Operating current-3
25	$V_{DD}$ current	$I_{DDCW3}$	-	39	-	mA	8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, $V_{PP}/V_{NN}=\pm 5V$ EN=0
26	$V_{SS}$ current	$I_{SSCW3}$	-	28	-	mA	
27	$V_{PP}$ current	$I_{PPCW3}$	-	170	-	mA	
28	$V_{NN}$ current	$I_{NNCW3}$	-	166	-	mA	

Table 3 DC Characteristics (Embedded FV, Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
29	V <sub>LL</sub> current	I <sub>LLCW2</sub>	-	1.2	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
30	V <sub>DD</sub> current	I <sub>DDCW2</sub>	-	35	-	mA	
31	V <sub>SS</sub> current	I <sub>SSCW2</sub>	-	22	-	mA	
32	V <sub>PP</sub> current	I <sub>PPCW2</sub>	-	162	-	mA	
33	V <sub>NN</sub> current	I <sub>NNCW2</sub>	-	158	-	mA	
34	V <sub>LL</sub> current	I <sub>LLCW1</sub>	-	1.3	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
35	V <sub>DD</sub> current	I <sub>DDCW1</sub>	-	31	-	mA	
36	V <sub>SS</sub> current	I <sub>SSCW1</sub>	-	17	-	mA	
37	V <sub>PP</sub> current	I <sub>PPCW1</sub>	-	148	-	mA	
38	V <sub>NN</sub> current	I <sub>NNCW1</sub>	-	146	-	mA	

### AC Characteristics

Table 4 AC Characteristics (Embedded FV, Clock mode)

V<sub>LL</sub>=3.3V, V<sub>DD</sub>=5V, V<sub>SS</sub>=-5V, T<sub>A</sub>=25°C, 220pF//1kΩ load, CLK=100MHz, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	f <sub>CLK</sub>	-	100	-	MHz	See Fig.6 D= τ /T
2	Duty cycle	D	40	50	60	%	
3	Setup time	t <sub>SU</sub>	-0.2	-	-	ns	
4	Hold time	t <sub>HOLD</sub>	3.4	-	-	ns	
5	Delay time on outputs rise	t <sub>dr(on)</sub>	-	53	-	ns	Bipolar half cycle f=5MHz, PRT=200μs V <sub>PP</sub> /V <sub>NN</sub> =+/-60V Current mode=4 See Fig.3
6	Delay time on outputs fall	t <sub>df(on)</sub>	-	53	-	ns	
7	Delay time off outputs rise	t <sub>dr(off)</sub>	-	53	-	ns	
8	Delay time off outputs fall	t <sub>df(off)</sub>	-	53	-	ns	
9	t <sub>dr(on)</sub> -t <sub>df(on)</sub>   Delay time matching	Δt <sub>delay(on)</sub>	-	±1	±3	ns	
10	t <sub>dr(off)</sub> -t <sub>df(off)</sub>   Delay time matching	Δt <sub>delay(off)</sub>	-	±1	±3	ns	Bipolar 2-cycle f=5MHz, PRT=200μs V <sub>PP</sub> /V <sub>NN</sub> =+/-60V Current mode=4 See Fig.4
11	Output frequency range	f <sub>OUT</sub>	-	-	20	MHz	
12	Output rise time	t <sub>r</sub>	-	18	-	ns	
13	Output fall time	t <sub>f</sub>	-	18	-	ns	
14	Second harmonic distortion	HD2	-	-40	-	dBc	Bipolar CW, f=5MHz V <sub>PP</sub> /V <sub>NN</sub> =+/-5V, Current mode=1 See Fig.5
15	Delay jitter on rise or fall	t <sub>Jr</sub> , t <sub>Jf</sub>	-	20	-	ps	
16	Enable time	t <sub>EN</sub>	-	57	-	ns	
17	Disable time	t <sub>DIS</sub>	-	83	-	ns	EN rise edge to output HiZ
18	Clock Enable time	t <sub>CLKEN</sub>	-	57	-	ns	CLKEN fall edge to output burst
19	Clock Disable time	t <sub>CLKDIS</sub>	-	83	-	ns	CLKEN rise edge to output HiZ

Thermal Protection Characteristics

Table 5 Thermal Protection Characteristics

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V <sub>PUTHP</sub>	-	-	5.25	V	Open drain
2	THP output current	I <sub>THP</sub>	-	1.0	-	mA	-
3	THP output low voltage	V <sub>OLTHP</sub>	-	-	1.0	V	V <sub>LL</sub> =3.3V, I <sub>THP</sub> =1mA
4	THP temperature threshold	T <sub>THP</sub>	90	110	130	°C	
5	THP reset hysteresis	T <sub>HYSTHP</sub>	-	10	-	°C	

Device Characteristics

Table 6 Output P-Channel MOSFET (Px) Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I <sub>OUTP</sub>	-	-1.8	-	A	V <sub>gs</sub> =-5V, V <sub>ds</sub> =-100V
2	Channel resistance	R <sub>ONP</sub>	-	7	-	Ω	V <sub>gs</sub> =-5V, I <sub>d</sub> =-0.5A
3	Output capacitance	C <sub>OSSP</sub>	-	27	-	pF	V <sub>gs</sub> =0V, V <sub>ds</sub> =-10V, f=1MHz

Note: These items above are not tested when shipped.

Table 7 Output N-Channel MOSFET (Nx) Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I <sub>OUTN</sub>	-	1.8	-	A	V <sub>gs</sub> =5V, V <sub>ds</sub> =100V
2	Channel resistance	R <sub>ONN</sub>	-	7	-	Ω	V <sub>gs</sub> =5V, I <sub>d</sub> =0.5A
3	Output capacitance	C <sub>OSSN</sub>	-	11	-	pF	V <sub>gs</sub> =0V, V <sub>ds</sub> =10V, f=1MHz

Note: These items above are not tested when shipped.

Table 8 Output GND-Clamp P-Channel MOSFET (Px<sub>G</sub>) Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I <sub>OUTP<sub>G</sub></sub>	-	-1.0	-	A	V <sub>gs</sub> =-5V, V <sub>ds</sub> =-100V
2	Channel resistance	R <sub>ONP<sub>G</sub></sub>	-	13	-	Ω	V <sub>gs</sub> =-5V, I <sub>d</sub> =-0.1A
3	Output capacitance	C <sub>OSSP<sub>G</sub></sub>	-	15	-	pF	V <sub>gs</sub> =0V, V <sub>ds</sub> =-10V, f=1MHz

Note: These items above are not tested when shipped.

Table 9 Output GND-Clamp N-Channel MOSFET (Nx<sub>G</sub>) Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I <sub>OUTN<sub>G</sub></sub>	-	1.0	-	A	V <sub>gs</sub> =5V, V <sub>ds</sub> =100V
2	Channel resistance	R <sub>ONN<sub>G</sub></sub>	-	13	-	Ω	V <sub>gs</sub> =5V, I <sub>d</sub> =0.1A
3	Output capacitance	C <sub>OSSN<sub>G</sub></sub>	-	6	-	pF	V <sub>gs</sub> =0V, V <sub>ds</sub> =10V, f=1MHz

Note: These items above are not tested when shipped.

Table 10 Output GND-Clamp Analog Switch (ASWx) Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	On-state resistance	R <sub>ONASW</sub>	-	500	-	Ω	V <sub>gs</sub> =5V, I <sub>d</sub> =0.01A

Note: These items above are not tested when shipped.

Table 11 Output Blocking HV Diode Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V <sub>FDHV</sub>	-	1.0	-	V	I <sub>F</sub> =100mA
2	Reverse voltage	V <sub>RDHV</sub>	200	-	-	V	I <sub>R</sub> =1μA

Note: These items above are not tested when shipped.

Table 12 Output Noise-Cut LV Diode Characteristics

T<sub>A</sub>=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V <sub>FDLV</sub>	-	0.85	-	V	I <sub>F</sub> =100mA

Note: These items above are not tested when shipped.



### 3.1.2 Transparent Mode (CLKEN=1)

#### DC Characteristics

Table 13 DC Characteristics (Embedded FV, Transparent mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=0, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	$I_{IH}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	$\mu A$	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	$I_{IL}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , CLK, ATHP
			-	66	-	$\mu A$	EN, CC1, CC0, CLKEN, FVSEL 50kΩ internal pull-up resistor
3	Input logic capacitance	$C_{IN}$	-	2	-	pF	-
4	$V_{LL}$ current	$I_{LLQD}$	-	0.5	-	$\mu A$	Quiescent current-1
5	$V_{DD}$ current	$I_{DDQD}$	-	1.1	-	mA	EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$
6	$V_{SS}$ current	$I_{SSQD}$	-	0.10	-	mA	
7	$V_{PP}$ current	$I_{PPQD}$	-	0.03	-	mA	
8	$V_{NN}$ current	$I_{NNQD}$	-	0.03	-	mA	
9	$V_{LL}$ current	$I_{LLQE}$	-	66	-	$\mu A$	Quiescent current-2
10	$V_{DD}$ current	$I_{DDQE}$	-	5.5	-	mA	EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$ $P_{INX}=1$ , $N_{INX}=1$ (x=1~8)
11	$V_{SS}$ current	$I_{SSQE}$	-	5.0	-	mA	
12	$V_{PP}$ current	$I_{PPQE}$	-	0.15	-	mA	
13	$V_{NN}$ current	$I_{NNQE}$	-	0.15	-	mA	
14	$V_{LL}$ current	$I_{LLPW}$	-	75	-	$\mu A$	Operating current-1
15	$V_{DD}$ current	$I_{DDPW}$	-	5.6	-	mA	8-channel active Bipolar 1-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ EN=0, Current mode=4
16	$V_{SS}$ current	$I_{SSPW}$	-	5.1	-	mA	
17	$V_{PP}$ current	$I_{PPPW}$	-	1.2	-	mA	
18	$V_{NN}$ current	$I_{NNPW}$	-	1.8	-	mA	
19	$V_{LL}$ current	$I_{LLCW4}$	-	0.60	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, $V_{PP}/V_{NN}=\pm 5V$ EN=0
20	$V_{DD}$ current	$I_{DDCW4}$	-	32	-	mA	
21	$V_{SS}$ current	$I_{SSCW4}$	-	34	-	mA	
22	$V_{PP}$ current	$I_{PPCW4}$	-	178	-	mA	
23	$V_{NN}$ current	$I_{NNCW4}$	-	174	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, $V_{PP}/V_{NN}=\pm 5V$ EN=0
24	$V_{LL}$ current	$I_{LLCW3}$	-	0.65	-	mA	
25	$V_{DD}$ current	$I_{DDCW3}$	-	28	-	mA	
26	$V_{SS}$ current	$I_{SSCW3}$	-	28	-	mA	
27	$V_{PP}$ current	$I_{PPCW3}$	-	170	-	mA	
28	$V_{NN}$ current	$I_{NNCW3}$	-	166	-	mA	

Table 13 DC Characteristics (Embedded FV, Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
29	V <sub>LL</sub> current	I <sub>LLCW2</sub>	-	0.65	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
30	V <sub>DD</sub> current	I <sub>DCCW2</sub>	-	24	-	mA	
31	V <sub>SS</sub> current	I <sub>SSCW2</sub>	-	22	-	mA	
32	V <sub>PP</sub> current	I <sub>PPCW2</sub>	-	162	-	mA	
33	V <sub>NN</sub> current	I <sub>NNCW2</sub>	-	158	-	mA	
34	V <sub>LL</sub> current	I <sub>LLCW1</sub>	-	0.70	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
35	V <sub>DD</sub> current	I <sub>DCCW1</sub>	-	20	-	mA	
36	V <sub>SS</sub> current	I <sub>SSCW1</sub>	-	17	-	mA	
37	V <sub>PP</sub> current	I <sub>PPCW1</sub>	-	148	-	mA	
38	V <sub>NN</sub> current	I <sub>NNCW1</sub>	-	146	-	mA	

### AC Characteristics

Table 14 AC Characteristics (Embedded FV, Transparent mode)

V<sub>LL</sub>=3.3V, V<sub>DD</sub>=5V, V<sub>SS</sub>=-5V, T<sub>A</sub>=25°C, 220pF//1kΩ load, CLK=0, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	t <sub>dr(on)</sub>	-	48	-	ns	Bipolar half cycle f=5MHz, PRT=200μs V <sub>PP</sub> /V <sub>NN</sub> =+/-60V Current mode=4 See Fig.3
2	Delay time on outputs fall	t <sub>df(on)</sub>	-	48	-	ns	
3	Delay time off outputs rise	t <sub>dr(off)</sub>	-	48	-	ns	
4	Delay time off outputs fall	t <sub>df(off)</sub>	-	48	-	ns	
5	t <sub>dr(on)</sub> -t <sub>df(on)</sub>   Delay time matching	Δt <sub>delay(on)</sub>	-	±1	±3	ns	
6	t <sub>dr(off)</sub> -t <sub>df(off)</sub>   Delay time matching	Δt <sub>delay(off)</sub>	-	±1	±3	ns	
7	Output frequency range	f <sub>OUT</sub>	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200μs V <sub>PP</sub> /V <sub>NN</sub> =+/-60V Current mode=4 See Fig.4
8	Output rise time	t <sub>r</sub>	-	18	-	ns	
9	Output fall time	t <sub>f</sub>	-	18	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Delay jitter on rise or fall	t <sub>Jr</sub> , t <sub>Jf</sub>	-	20	-	ps	Bipolar CW, f=5MHz V <sub>PP</sub> /V <sub>NN</sub> =+/-5V, Current mode=1 See Fig.5
12	Enable time	t <sub>EN</sub>	-	52	-	ns	EN fall edge to output burst
13	Disable time	t <sub>DIS</sub>	-	78	-	ns	EN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.

### 3.2 FVSEL=0 (EXTERNAL floating voltage supplies)

#### 3.2.1 Clock Mode (CLKEN=0)

##### DC Characteristics

Table 15 DC Characteristics (External FV, Clock mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $V_{FP}=V_{PP}-5V$ ,  $V_{FN}=V_{NN}+5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=100MHz, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions	
			Min	Typ	Max			
1	Input logic high current	$I_{IH}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , EN, CC1, CC0, CLK, CLKEN, FVSEL	
			-	66	-	$\mu A$	ATHP 50kΩ internal pull-down resistor	
2	Input logic low current	$I_{IL}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , CLK, ATHP	
			-	66	-	$\mu A$	EN, CC1, CC0, CLKEN, FVSEL 50kΩ internal pull-up resistor	
3	Input logic capacitance	$C_{IN}$	-	2	-	pF	-	
4	$V_{LL}$ current	$I_{LLQD}$	-	1.0	-	mA	Quiescent current-1  EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$	
5	$V_{DD}$ current	$I_{DDQD}$	-	14	-	mA		
6	$V_{SS}$ current	$I_{SSQD}$	-	0.1	-	mA		
7	$V_{PP}$ current	$I_{PPQD}$	-	0	-	mA		
8	$V_{NN}$ current	$I_{NNQD}$	-	0	-	mA		
9	$V_{FP}$ current	$I_{FPQD}$	-	0.02	-	mA		
10	$V_{FN}$ current	$I_{FNQD}$	-	0.02	-	mA		
11	$V_{LL}$ current	$I_{LLQE}$	-	1.1	-	mA		Quiescent current-2  EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$ $P_{INX}=1$ , $N_{INX}=1$ (x=1~8)
12	$V_{DD}$ current	$I_{DDQE}$	-	18	-	mA		
13	$V_{SS}$ current	$I_{SSQE}$	-	5.0	-	mA		
14	$V_{PP}$ current	$I_{PPQE}$	-	0	-	mA		
15	$V_{NN}$ current	$I_{NNQE}$	-	0	-	mA		
16	$V_{FP}$ current	$I_{FPQE}$	-	0.02	-	mA		
17	$V_{FN}$ current	$I_{FNQE}$	-	0.02	-	mA		
18	$V_{LL}$ current	$I_{LLPW}$	-	1.1	-	mA	Operating current-1 8-channel active Bipolar 1-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ EN=0, Current mode=4	
19	$V_{DD}$ current	$I_{DDPW}$	-	18	-	mA		
20	$V_{SS}$ current	$I_{SSPW}$	-	5.1	-	mA		
21	$V_{PP}$ current	$I_{PPPW}$	-	2.0	-	mA		
22	$V_{NN}$ current	$I_{NNPW}$	-	2.0	-	mA		
23	$V_{FP}$ current	$I_{FPPW}$	-	0.20	-	mA		
24	$V_{FN}$ current	$I_{FNPW}$	-	0.20	-	mA		

Table 15 DC Characteristics (External FV, Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V <sub>LL</sub> current	I <sub>LLCW4</sub>	-	1.2	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
26	V <sub>DD</sub> current	I <sub>DCCW4</sub>	-	24	-		
27	V <sub>SS</sub> current	I <sub>SSCW4</sub>	-	8.0	-		
28	V <sub>PP</sub> current	I <sub>PPCW4</sub>	-	160	-		
29	V <sub>NN</sub> current	I <sub>NNCW4</sub>	-	160	-		
30	V <sub>FP</sub> current	I <sub>FPCW4</sub>	-	31	-		
31	V <sub>FN</sub> current	I <sub>FNCW4</sub>	-	20	-		
32	V <sub>LL</sub> current	I <sub>LLCW3</sub>	-	1.2	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
33	V <sub>DD</sub> current	I <sub>DCCW3</sub>	-	24	-		
34	V <sub>SS</sub> current	I <sub>SSCW3</sub>	-	8.0	-		
35	V <sub>PP</sub> current	I <sub>PPCW3</sub>	-	156	-		
36	V <sub>NN</sub> current	I <sub>NNCW3</sub>	-	156	-		
37	V <sub>FP</sub> current	I <sub>FPCW3</sub>	-	22	-		
38	V <sub>FN</sub> current	I <sub>FNCW3</sub>	-	15	-		
39	V <sub>LL</sub> current	I <sub>LLCW2</sub>	-	1.2	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
40	V <sub>DD</sub> current	I <sub>DCCW2</sub>	-	24	-		
41	V <sub>SS</sub> current	I <sub>SSCW2</sub>	-	8.0	-		
42	V <sub>PP</sub> current	I <sub>PPCW2</sub>	-	148	-		
43	V <sub>NN</sub> current	I <sub>NNCW2</sub>	-	148	-		
44	V <sub>FP</sub> current	I <sub>FPCW2</sub>	-	16	-		
45	V <sub>FN</sub> current	I <sub>FNCW2</sub>	-	11	-		
46	V <sub>LL</sub> current	I <sub>LLCW1</sub>	-	1.3	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
47	V <sub>DD</sub> current	I <sub>DCCW1</sub>	-	24	-		
48	V <sub>SS</sub> current	I <sub>SSCW1</sub>	-	8.0	-		
49	V <sub>PP</sub> current	I <sub>PPCW1</sub>	-	136	-		
50	V <sub>NN</sub> current	I <sub>NNCW1</sub>	-	136	-		
51	V <sub>FP</sub> current	I <sub>FPCW1</sub>	-	8.0	-		
52	V <sub>FN</sub> current	I <sub>FNCW1</sub>	-	6.0	-		

AC Characteristics

Table 16 AC Characteristics (External FV, Clock mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $V_{FP}=V_{PP}-5V$ ,  $V_{FN}=V_{NN}+5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=100MHz, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	$f_{CLK}$	-	100	-	MHz	See Fig.6 $D = \tau / T$
2	Duty cycle	D	40	50	60	%	
3	Setup time	$t_{SU}$	-0.2	-	-	ns	
4	Hold time	$t_{HOLD}$	3.4	-	-	ns	
5	Delay time on outputs rise	$t_{dr(on)}$	-	53	-	ns	Bipolar half cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ Current mode=4 See Fig.3
6	Delay time on outputs fall	$t_{df(on)}$	-	53	-	ns	
7	Delay time off outputs rise	$t_{dr(off)}$	-	53	-	ns	
8	Delay time off outputs fall	$t_{df(off)}$	-	53	-	ns	
9	$ t_{dr(on)}-t_{df(on)} $ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
10	$ t_{dr(off)}-t_{df(off)} $ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
11	Output frequency range	$f_{OUT}$	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ Current mode=4 See Fig.4
12	Output rise time	$t_r$	-	18	-	ns	
13	Output fall time	$t_f$	-	18	-	ns	
14	Second harmonic distortion	HD2	-	-40	-	dBc	See Fig.4
15	Delay jitter on rise or fall	$t_{Jr}$ , $t_{Jf}$	-	20	-	ps	Bipolar CW, f=5MHz $V_{PP}/V_{NN}=\pm 5V$ , Current mode=1 See Fig.5
16	Enable time	$t_{EN}$	-	57	-	ns	EN fall edge to output burst
17	Disable time	$t_{DIS}$	-	83	-	ns	EN rise edge to output HiZ
18	Clock Enable time	$t_{CLKEN}$	-	57	-	ns	CLKEN fall edge to output burst
19	Clock Disable time	$t_{CLKDIS}$	-	83	-	ns	CLKEN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.

### 3.2.2 Transparent Mode (CLKEN=1)

#### DC Characteristics

Table 17 DC Characteristics (External FV, Transparent mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $V_{FP}=V_{PP}-5V$ ,  $V_{FN}=V_{NN}+5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=0, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	$I_{IH}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	$\mu A$	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	$I_{IL}$	-10	-	10	$\mu A$	$P_{INX}$ , $N_{INX}$ , CLK, ATHP
			-	66	-	$\mu A$	EN, CC1, CC0, CLKEN, FVSEL 50kΩ internal pull-up resistor
3	Input logic capacitance	$C_{IN}$	-	2	-	pF	-
4	$V_{LL}$ current	$I_{LLQD}$	-	66	-	$\mu A$	Quiescent current-1  EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$
5	$V_{DD}$ current	$I_{DDQD}$	-	1.1	-	mA	
6	$V_{SS}$ current	$I_{SSQD}$	-	0.10	-	mA	
7	$V_{PP}$ current	$I_{PPQD}$	-	0	-	mA	
8	$V_{NN}$ current	$I_{NNQD}$	-	0	-	mA	
9	$V_{FP}$ current	$I_{FPQD}$	-	0.02	-	mA	
10	$V_{FN}$ current	$I_{FNQD}$	-	0.02	-	mA	
11	$V_{LL}$ current	$I_{LLQE}$	-	134	-	$\mu A$	Quiescent current-2  EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=\pm 100V$ $P_{INX}=1$ , $N_{INX}=1$ (x=1~8)
12	$V_{DD}$ current	$I_{DDQE}$	-	5.5	-	mA	
13	$V_{SS}$ current	$I_{SSQE}$	-	5.0	-	mA	
14	$V_{PP}$ current	$I_{PPQE}$	-	0	-	mA	
15	$V_{NN}$ current	$I_{NNQE}$	-	0	-	mA	
16	$V_{FP}$ current	$I_{FPQE}$	-	0.02	-	mA	
17	$V_{FN}$ current	$I_{FNQE}$	-	0.02	-	mA	
18	$V_{LL}$ current	$I_{LLPW}$	-	142	-	$\mu A$	Operating current-1 8-channel active Bipolar 1-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ EN=0, Current mode=4
19	$V_{DD}$ current	$I_{DDPW}$	-	5.6	-	mA	
20	$V_{SS}$ current	$I_{SSPW}$	-	5.1	-	mA	
21	$V_{PP}$ current	$I_{PPPW}$	-	2.0	-	mA	
22	$V_{NN}$ current	$I_{NNPW}$	-	2.0	-	mA	
23	$V_{FP}$ current	$I_{FPPW}$	-	0.20	-	mA	
24	$V_{FN}$ current	$I_{FNPW}$	-	0.20	-	mA	

Table 17 DC Characteristics (External FV, Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V <sub>LL</sub> current	I <sub>LLCW4</sub>	-	0.60	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
26	V <sub>DD</sub> current	I <sub>DCCW4</sub>	-	13	-	mA	
27	V <sub>SS</sub> current	I <sub>SSCW4</sub>	-	8.0	-	mA	
28	V <sub>PP</sub> current	I <sub>PPCW4</sub>	-	160	-	mA	
29	V <sub>NN</sub> current	I <sub>NNCW4</sub>	-	160	-	mA	
30	V <sub>FP</sub> current	I <sub>FPCW4</sub>	-	31	-	mA	
31	V <sub>FN</sub> current	I <sub>FNCW4</sub>	-	20	-	mA	
32	V <sub>LL</sub> current	I <sub>LLCW3</sub>	-	0.65	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
33	V <sub>DD</sub> current	I <sub>DCCW3</sub>	-	13	-	mA	
34	V <sub>SS</sub> current	I <sub>SSCW3</sub>	-	8.0	-	mA	
35	V <sub>PP</sub> current	I <sub>PPCW3</sub>	-	156	-	mA	
36	V <sub>NN</sub> current	I <sub>NNCW3</sub>	-	156	-	mA	
37	V <sub>FP</sub> current	I <sub>FPCW3</sub>	-	22	-	mA	
38	V <sub>FN</sub> current	I <sub>FNCW3</sub>	-	15	-	mA	
39	V <sub>LL</sub> current	I <sub>LLCW2</sub>	-	0.65	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
40	V <sub>DD</sub> current	I <sub>DCCW2</sub>	-	13	-	mA	
41	V <sub>SS</sub> current	I <sub>SSCW2</sub>	-	8.0	-	mA	
42	V <sub>PP</sub> current	I <sub>PPCW2</sub>	-	148	-	mA	
43	V <sub>NN</sub> current	I <sub>NNCW2</sub>	-	148	-	mA	
44	V <sub>FP</sub> current	I <sub>FPCW2</sub>	-	16	-	mA	
45	V <sub>FN</sub> current	I <sub>FNCW2</sub>	-	11	-	mA	
46	V <sub>LL</sub> current	I <sub>LLCW1</sub>	-	0.70	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V <sub>PP</sub> /V <sub>NN</sub> =+/-5V EN=0
47	V <sub>DD</sub> current	I <sub>DCCW1</sub>	-	13	-	mA	
48	V <sub>SS</sub> current	I <sub>SSCW1</sub>	-	8	-	mA	
49	V <sub>PP</sub> current	I <sub>PPCW1</sub>	-	136	-	mA	
50	V <sub>NN</sub> current	I <sub>NNCW1</sub>	-	136	-	mA	
51	V <sub>FP</sub> current	I <sub>FPCW1</sub>	-	8.0	-	mA	
52	V <sub>FN</sub> current	I <sub>FNCW1</sub>	-	6.0	-	mA	

AC Characteristics

Table 18 AC Characteristics (External FV, Transparent mode)

$V_{LL}=3.3V$ ,  $V_{DD}=5V$ ,  $V_{SS}=-5V$ ,  $V_{FP}=V_{PP}-5V$ ,  $V_{FN}=V_{NN}+5V$ ,  $T_A=25^{\circ}C$ , 220pF//1kΩ load, CLK=0, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

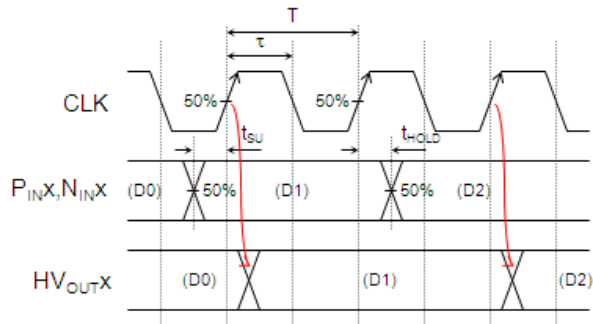
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	$t_{dr(on)}$	-	48	-	ns	Bipolar half cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ Current mode=4 See Fig.3
2	Delay time on outputs fall	$t_{df(on)}$	-	48	-	ns	
3	Delay time off outputs rise	$t_{dr(off)}$	-	48	-	ns	
4	Delay time off outputs fall	$t_{df(off)}$	-	48	-	ns	
5	$ t_{dr(on)}-t_{df(on)} $ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
6	$ t_{dr(off)}-t_{df(off)} $ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
7	Output frequency range	$f_{OUT}$	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200μs $V_{PP}/V_{NN}=\pm 60V$ Current mode=4 See Fig.4
8	Output rise time	$t_r$	-	18	-	ns	
9	Output fall time	$t_f$	-	18	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Delay jitter on rise or fall	$t_{Jr}$ , $t_{Jf}$	-	20	-	ps	Bipolar CW, f=5MHz $V_{PP}/V_{NN}=\pm 5V$ , Current mode=1 See Fig.5
12	Enable time	$t_{EN}$	-	52	-	ns	EN fall edge to output burst
13	Disable time	$t_{DIS}$	-	78	-	ns	EN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.



### 4. Switching Time Diagram (EN=0)

Clock mode (CLKEN=0)



Transparent mode (CLKEN=1)

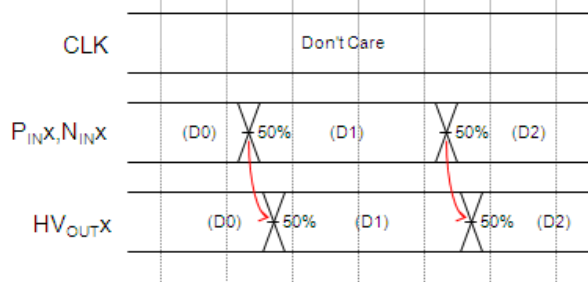


Fig. 3 Setup/hold time

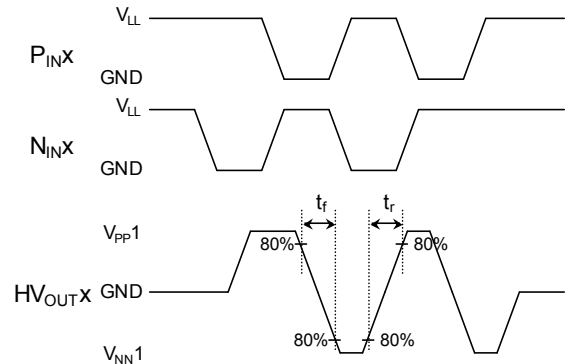


Fig. 5 Output rise/fall time

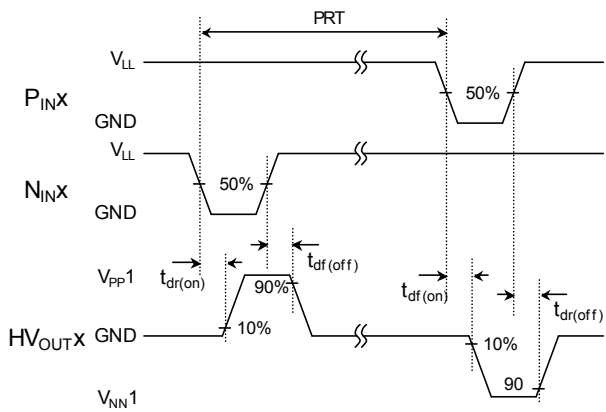


Fig. 4 Propagation delay time

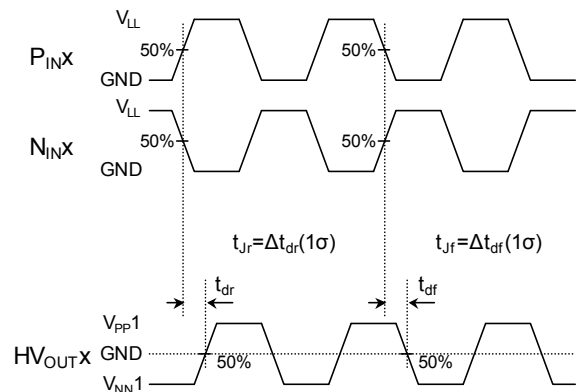


Fig. 6 Delay jitter on rise/fall

## 5. Truth Table

Table 19 Truth Table

Logic Inputs			HV MOSFET status					Output
EN	P <sub>INx</sub>	N <sub>INx</sub>	P <sub>x</sub>	N <sub>x</sub>	P <sub>xG</sub>	N <sub>xG</sub>	ASW <sub>x</sub>	HV <sub>OUTx</sub>
			+HV	-HV	GND	GND	GND	
0	0	0	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	1	OFF	<b>ON</b>	OFF	OFF	OFF	-HV
0	1	0	<b>ON</b>	OFF	OFF	OFF	OFF	+HV
0	1	1	OFF	OFF	<b>ON</b>	<b>ON</b>	<b>ON</b>	GND
1	X	X	OFF	OFF	OFF	OFF	OFF	HiZ

Note:

- x=1~8
- V<sub>PP</sub> / V<sub>NN</sub> = +/-HV
- 2-input / channel

## 6. Drive Current Mode Control

Table 20 Drive Current Mode Control Table

Current Mode	CC1	CC0	I <sub>OUT</sub>   [A] *1	
			P <sub>x</sub>	N <sub>x</sub>
1	0	0	0.45	0.45
2	0	1	0.9	0.9
3	1	0	1.35	1.35
4	1	1	1.8	1.8

Note:

\*1) Output saturation current @ |V<sub>ds</sub>|=100V

Recommended current mode is as follows:

- Current mode=4 for high-voltage, short pulse train operations
- Current mode=1~3 for low-voltage, long pulse train or continuous wave operations

## 7. Pin Configuration

Table 21 Pin Configuration

Pin#	Pin Name	I/O	Function
1	N <sub>IN2</sub>	I	Input logic control of the output of channel 2
2	P <sub>IN3</sub>	I	Input logic control of the output of channel 3
3	N <sub>IN3</sub>	I	Input logic control of the output of channel 3
4	P <sub>IN4</sub>	I	Input logic control of the output of channel 4
5	N <sub>IN4</sub>	I	Input logic control of the output of channel 4
6	V <sub>LL</sub>	-	Positive voltage supply of low voltage interface (+1.8~5V)
7	CLK	I	Clock Input (100MHz)
8	GND	-	Drive power ground (0V)
9	P <sub>IN5</sub>	I	Input logic control of the output of channel 5
10	N <sub>IN5</sub>	I	Input logic control of the output of channel 5
11	P <sub>IN6</sub>	I	Input logic control of the output of channel 6
12	N <sub>IN6</sub>	I	Input logic control of the output of channel 6
13	P <sub>IN7</sub>	I	Input logic control of the output of channel 7
14	N <sub>IN7</sub>	I	Input logic control of the output of channel 7
15	P <sub>IN8</sub>	I	Input logic control of the output of channel 8
16	N <sub>IN8</sub>	I	Input logic control of the output of channel 8
17	EN	I	Control of drive output enable, 1=off, 0=on (50kΩ pull-up resistor embedded)
18	CLKEN	I	Control of clock enable, 1=clock disable, 0=clock enable (50kΩ pull-up resistor embedded)
19	NC	-	No connection.
20	ATHP	I	Control of active THP enable, 1=disable, 0=enable (50kΩ pull-down resistor embedded)
21	THP	O	Thermal protection output, open N-MOS drain
22	V <sub>SS</sub>	-	Negative low voltage power supply (-5V)
23	V <sub>FP</sub>	-	Built-in floating gate drive power supply for HV P-MOS @FVSEL=1 External floating gate drive power supply for HV P-MOS @FVSEL=0 (V <sub>PP</sub> -5V)
24	V <sub>FN</sub>	-	Built-in floating gate drive power supply for HV N-MOS @FVSEL=1 External floating gate drive power supply for HV N-MOS @FVSEL=0 (V <sub>NN</sub> +5V)
25	V <sub>NN</sub>	-	Negative high voltage power supply (-100 to 0V)
26	HV <sub>OUT8</sub>	O	High voltage output of channel 8

Table 21 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
27	V <sub>PP</sub>	-	Positive high voltage power supply (0 to +100V)
28	HV <sub>OUT7</sub>	O	High voltage output of channel 7
29	V <sub>NN</sub>	-	Negative high voltage power supply (-100 to 0V)
30	HV <sub>OUT6</sub>	O	High voltage output of channel 6
31	V <sub>PP</sub>	-	Positive high voltage power supply (0 to +100V)
32	HV <sub>OUT5</sub>	O	High voltage output of channel 5
33	GND	-	Drive power ground (0V)
34	HV <sub>OUT4</sub>	O	High voltage output of channel 4
35	V <sub>PP</sub>	-	Positive high voltage power supply (0 to +100V)
36	HV <sub>OUT3</sub>	O	High voltage output of channel 3
37	V <sub>NN</sub>	-	Negative high voltage power supply (-100 to 0V)
38	HV <sub>OUT2</sub>	O	High voltage output of channel 2
39	V <sub>PP</sub>	-	Positive high voltage power supply (0 to +100V)
40	HV <sub>OUT1</sub>	O	High voltage output of channel 1
41	V <sub>NN</sub>	-	Negative high voltage power supply (-100 to 0V)
42	V <sub>FN</sub>	-	Built-in floating gate drive power supply for HV N-MOS @FVSEL=1 External floating gate drive power supply for HV N-MOS @FVSEL=0 (V <sub>NN</sub> +5V)
43	V <sub>FP</sub>	-	Built-in floating gate drive power supply for HV P-MOS @FVSEL=1 External floating gate drive power supply for HV P-MOS @FVSEL=0 (V <sub>PP</sub> -5V)
44	V <sub>DD</sub>	-	Positive low voltage power supply (+5V)
45	CC0	I	Control of the least significant bit for drive current mode (50kΩ pull-up resistor embedded)
46	CC1	I	Control of the most significant bit for drive current mode (50kΩ pull-up resistor embedded)
47	FVSEL	I	Control of floating gate drive power supply, 1=built-in, 0=external (50kΩ pull-up resistor embedded)
48	GND	-	Drive power ground (0V)
49	GND	-	Drive power ground (0V)
50	P <sub>IN1</sub>	I	Input logic control of the output of channel 1
51	N <sub>IN1</sub>	I	Input logic control of the output of channel 1
52	P <sub>IN2</sub>	I	Input logic control of the output of channel 2

8. Package Outline

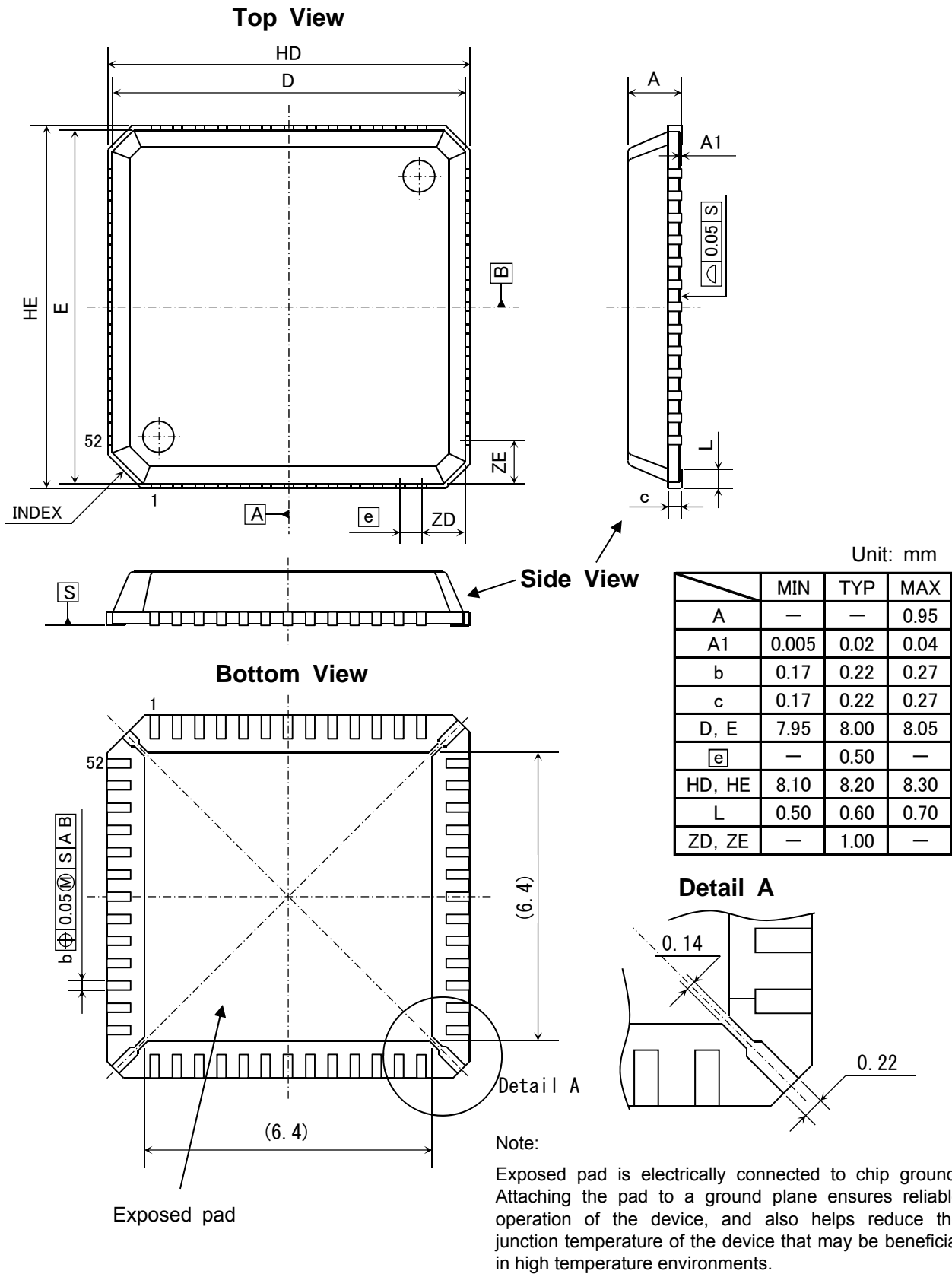
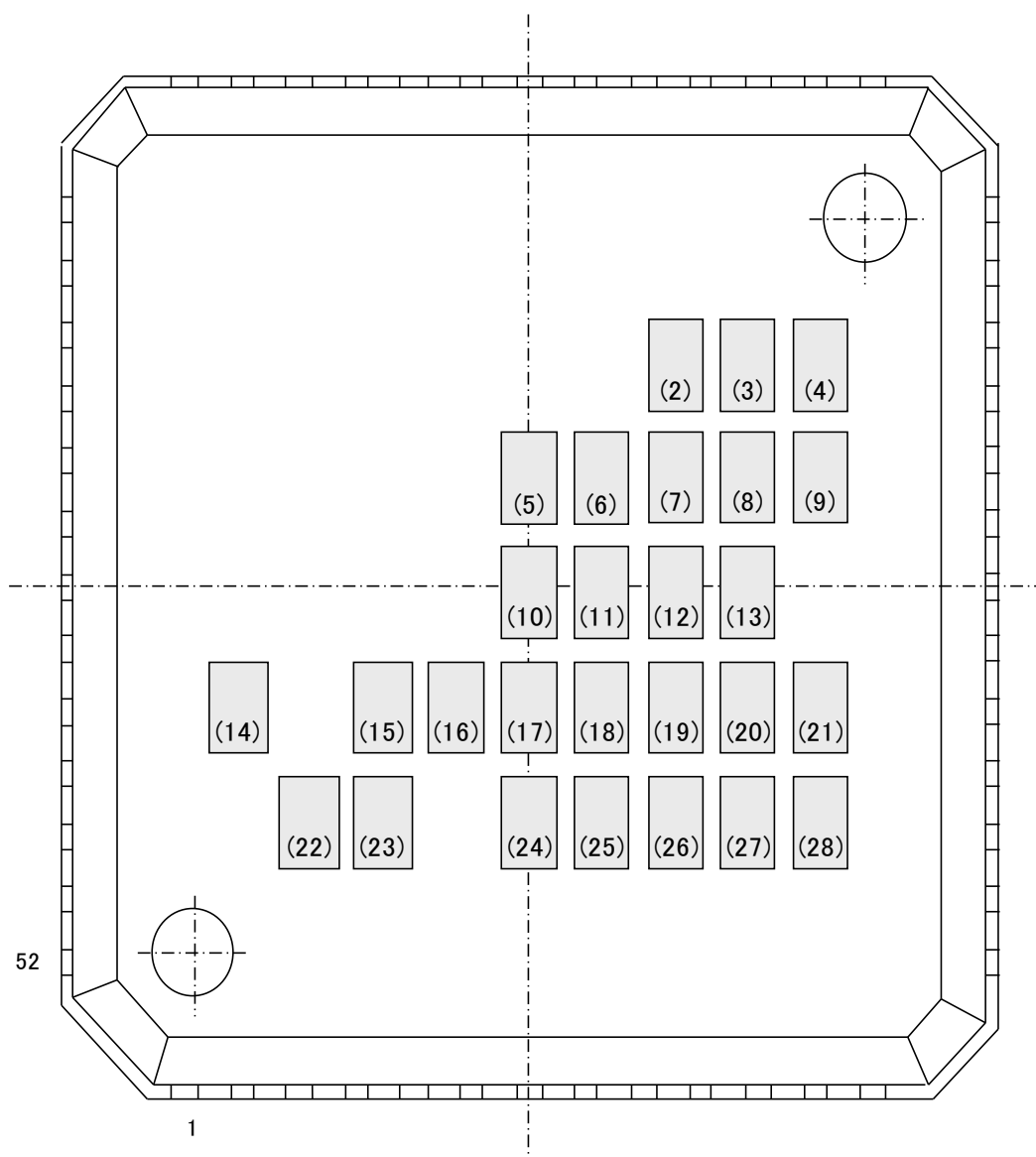


Fig.7 Package Outline (52-Lead QFN Package)

9. Package Marking



No.	Code
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc. " I ") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(13)	HDL6V5583 (product name)
(14)~(23)	Quality control code
(24)~(28)	Country of origin

Fig.8 Package Marking

**ABLIC Inc.**

10. Transport Media, Quantity

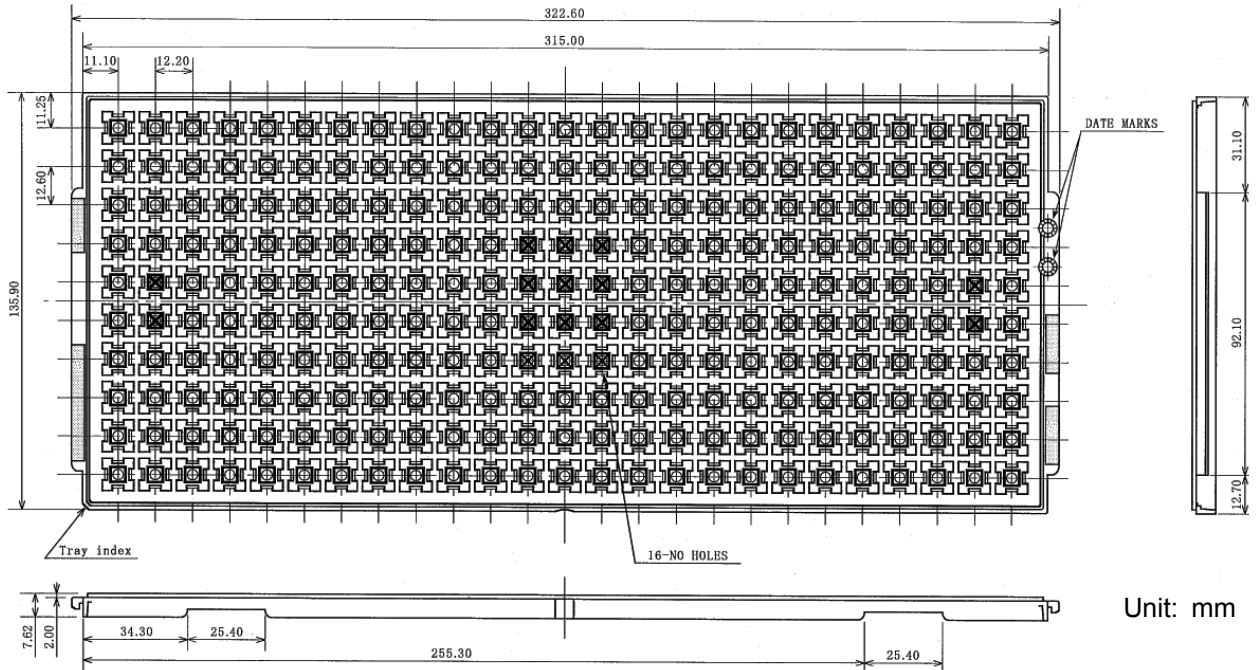


Fig.9 IC Tray Outline

1. Max 250 IC/Tray
2. 16 positions without holes (\*)
3. PPE containing carbon and static proof
4. Heat proof: 130°C, 24hr

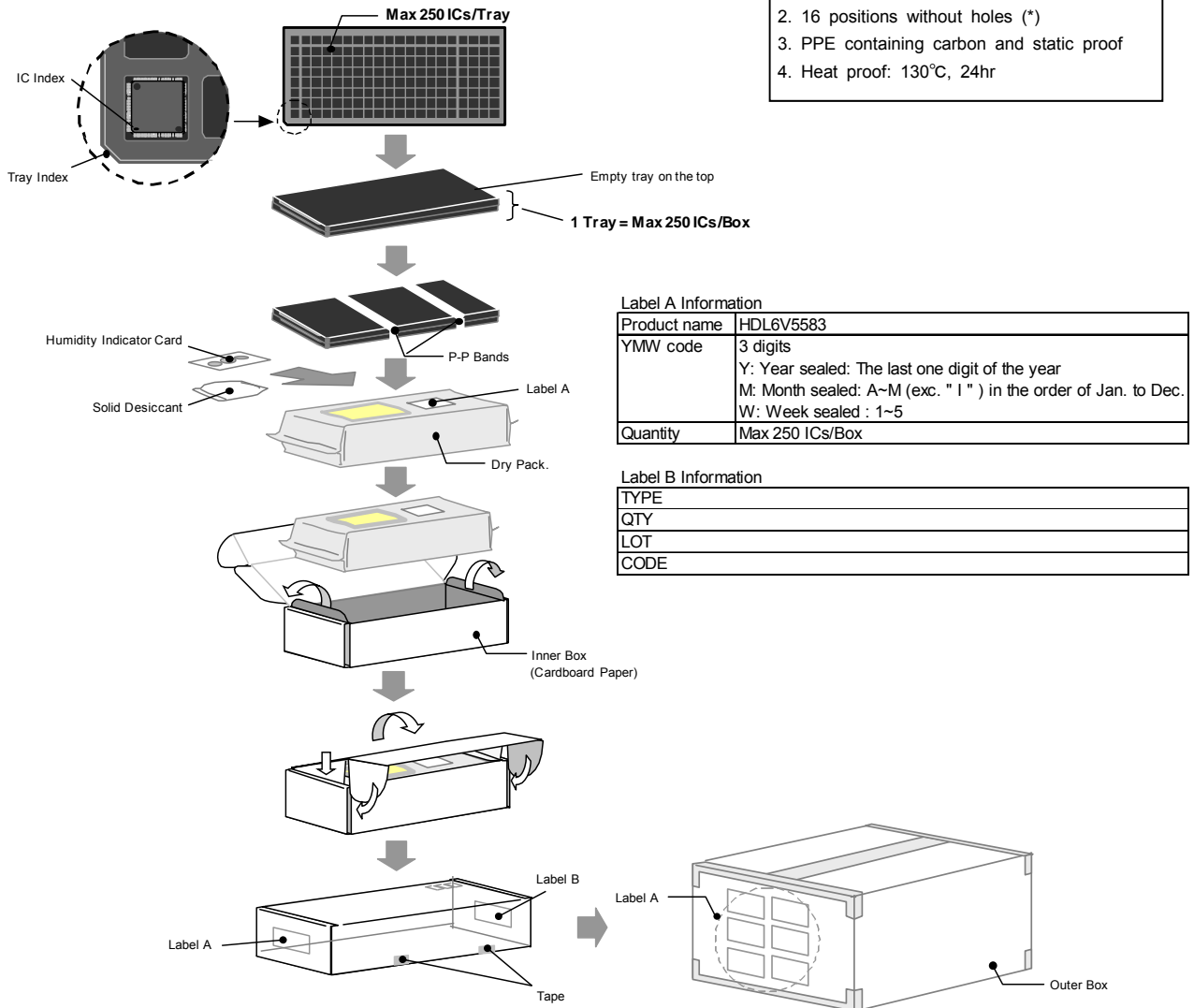


Fig.10 Transport Media, Quantity

## 11. Mounting, Storage

### 11.1 Mounting Pad Design Example

Unit: mm

HE	8.20
HD	8.20
e	0.50
b3	0.32±0.05
L2	0.55±0.05
L1	0.20±0.05

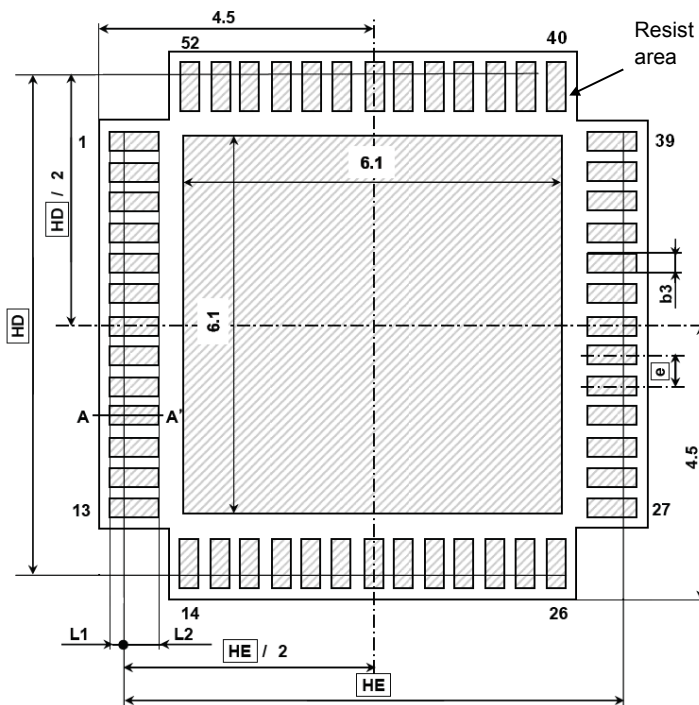


Fig.11 Mounting Pad Design Example

### 11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking, or within 10 days of total exposure after the second dehumidification.

### 11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable. IR/Air reflow heating conditions are shown below.

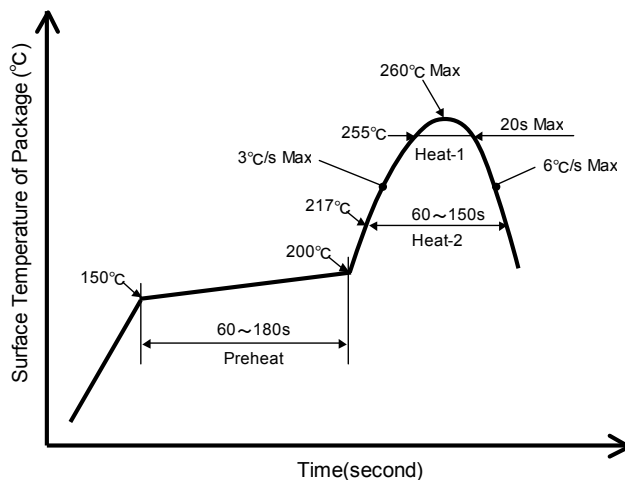


Fig.12 IR/Air Reflow Heating Conditions



## 12. Inspection

Hundred percent inspections shall be conducted on electrical characteristics.

## 13. Important Notice

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## **14. Cautions**

- 14.1 Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
  - 14.1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
  - 14.1.2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.
  - 14.1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
  - 14.1.4 Prevent friction with other materials made with high polymer.
  - 14.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
  - 14.1.6 Avoid dealing with or storing products in an extremely arid environment.
- 14.2 "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
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- 14.4 Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
- 14.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

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