# NDS8926
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.5 A, 20 V. $R_{DS(ON)} = 0.035\ \Omega$ @ $V_{GS} = 4.5$ V
  $R_{DS(ON)} = 0.045\ \Omega$ @ $V_{GS} = 2.7$ V.

- High density cell design for extremely low $R_{DS(ON)}$.

- High power and current handling capability in a widely used surface mount package.

- Dual MOSFET in surface mount package.
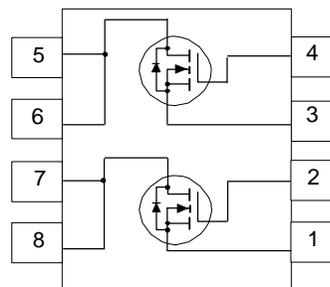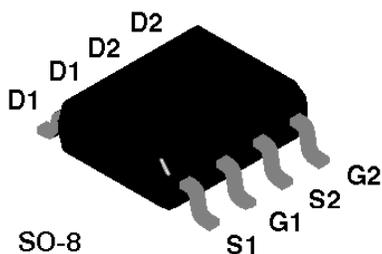
Absolute Maximum Ratings $T_A = 25°C$ unless otherwise note

Symbol	Parameter		NDS8926	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		8	V
I_D	Drain Current - Continuous	(Note 1a)	5.5	A
	- Pulsed		20	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note1b)	1	
		(Note1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA		20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16$ V, $V_{GS} = 0$ V				1	µA
			$T_J = 55°C$			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 8$ V, $V_{DS} = 0$ V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -8$ V, $V_{DS} = 0$ V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA		0.4	0.6	1	V
			$T_J = 125°C$	0.3	0.35	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5$ V, $I_D = 5.5$ A			0.029	0.035	Ω
			$T_J = 125°C$		0.04	0.063	
		$V_{GS} = 2.7$ V, $I_D = 5$ A			0.035	0.045	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5$ V, $V_{DS} = 5$ V		20			A
		$V_{GS} = 2.7$ V, $V_{DS} = 5$ V		10			
g_{FS}	Forward Transconductance	$V_{DS} = 10$ V, $I_D = 5.5$ A			14		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1.0 MHz			760		pF
C_{oss}	Output Capacitance				440		pF
C_{rss}	Reverse Transfer Capacitance				160		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 6$ V, $I_D = 1$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 6$ Ω			10	20	ns
t_r	Turn - On Rise Time				30	50	ns
$t_{D(off)}$	Turn - Off Delay Time				55	80	ns
t_f	Turn - Off Fall Time				20	40	ns
Q_g	Total Gate Charge	$V_{DS} = 10$ V, $I_D = 5.5$ A, $V_{GS} = 4.5$ V			21	30	nC
Q_{gs}	Gate-Source Charge				2.3		nC
Q_{gd}	Gate-Drain Charge				6.8		nC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS\,(ON)}@T_J$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

   a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

   b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

   c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.
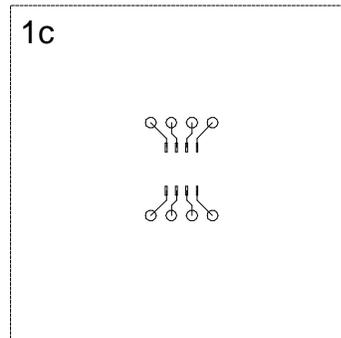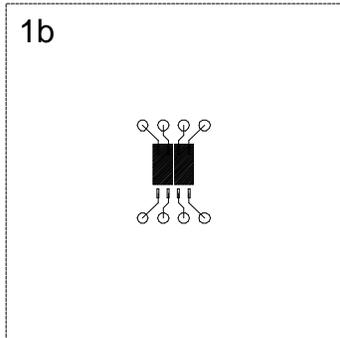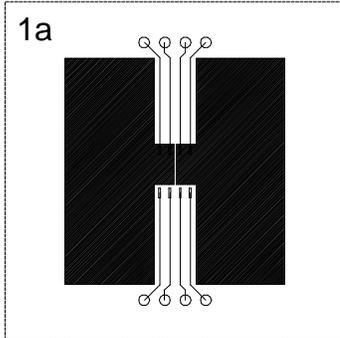
Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 2.0%.

Typical Electrical Characteristics
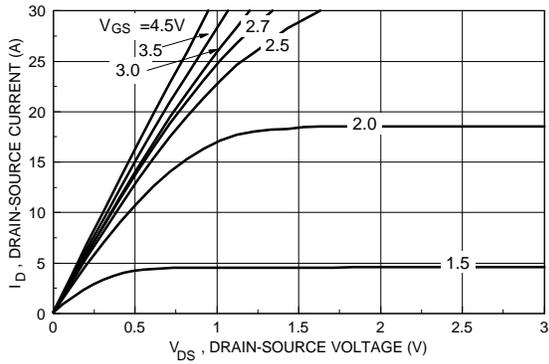

Figure 1. On-Region Characteristics.
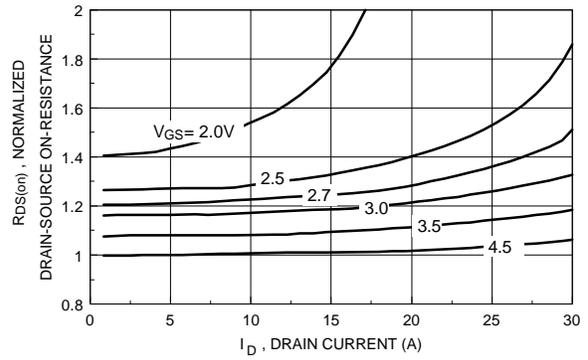
Figure 2. On-Resistance Variation with Gate
Voltage and Drain Current.
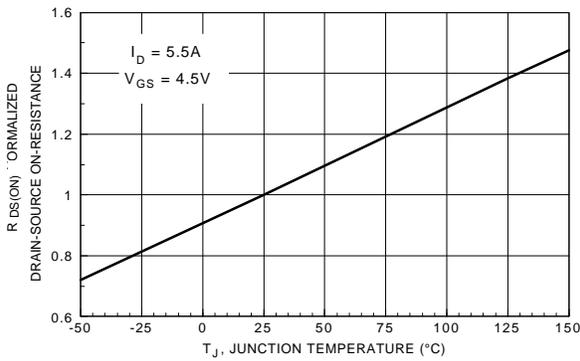
Figure 3. On-Resistance Variation with
Temperature.
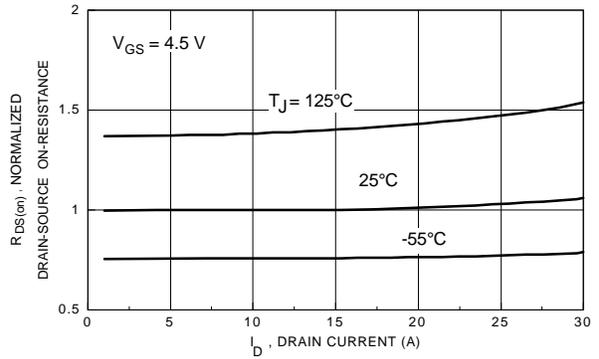
Figure 4. On-Resistance Variation with Drain
Current and Temperature.
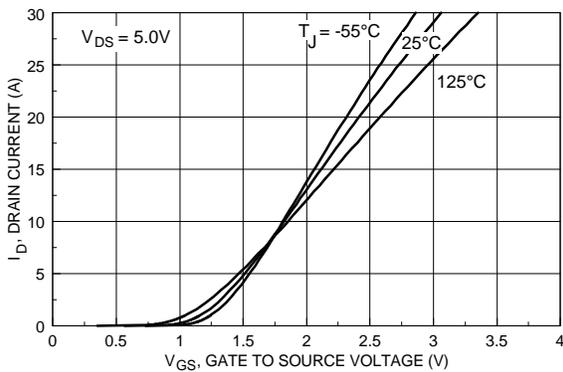

Figure 5. Transfer Characteristics.
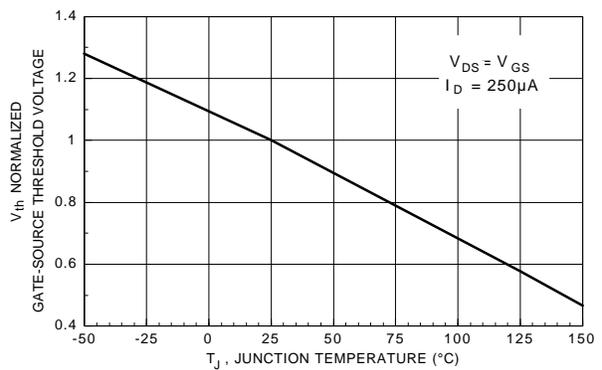
Figure 6. Gate Threshold Variation with
Temperature.

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# Typical Electrical Characteristics
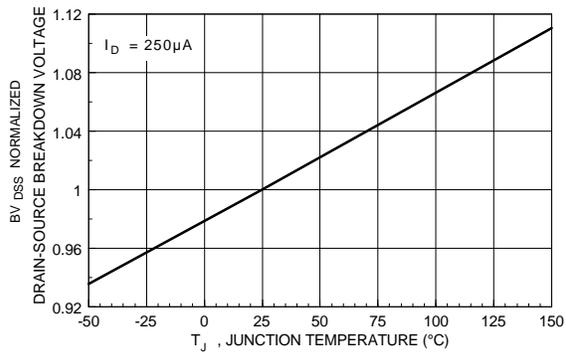
Figure 7. Breakdown Voltage Variation with Temperature.
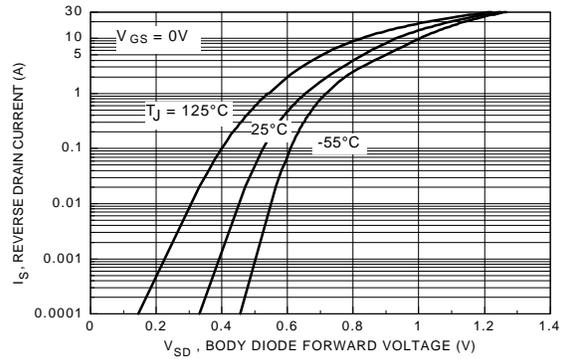
Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.
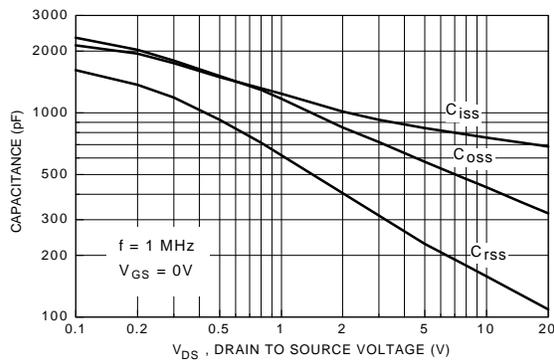
Figure 9. Capacitance Characteristics.
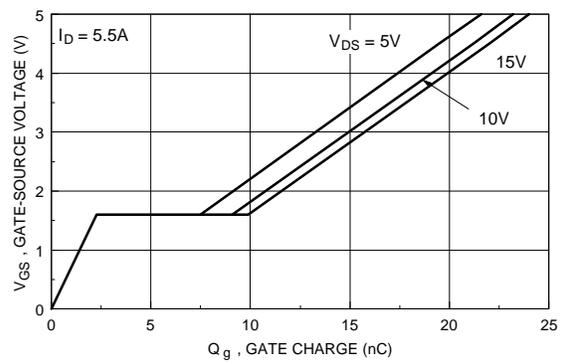

Figure 10. Gate Charge Characteristics.
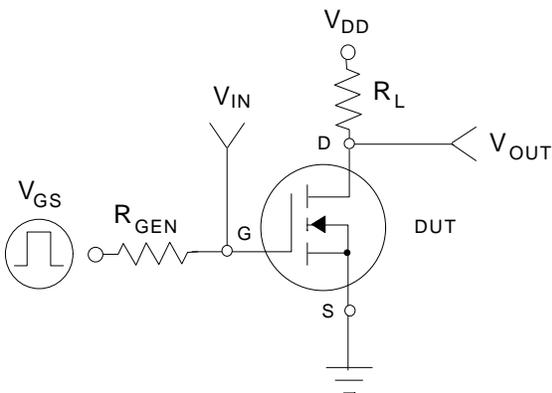

Figure 11. Switching Test Circuit.
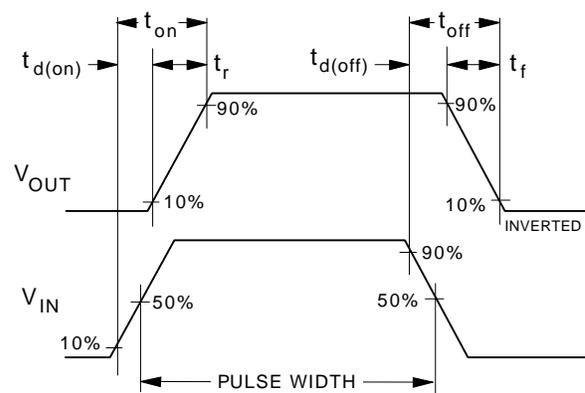
Figure 12. Switching Waveforms.

Electrical and Thermal Characteristics
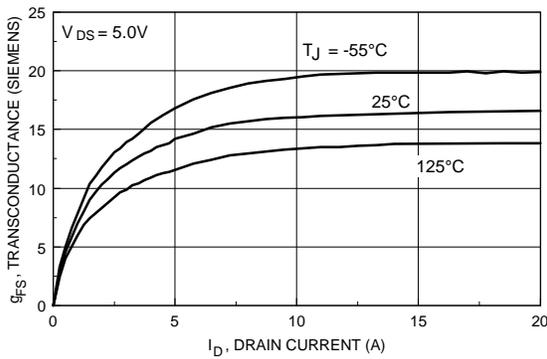
Figure 13. Transconductance Variation with Drain
Current and Temperature.
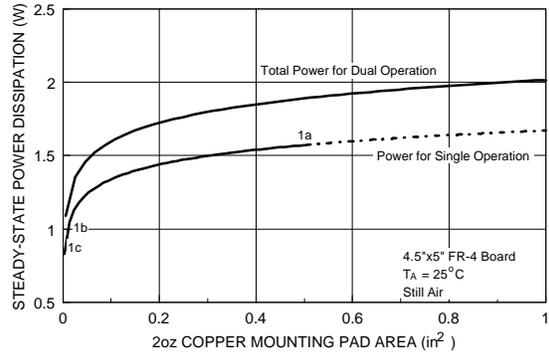
Figure 14. SO-8 Dual Package Maximum
Steady-State Power Dissipation versus
Copper Mounting Pad Area.
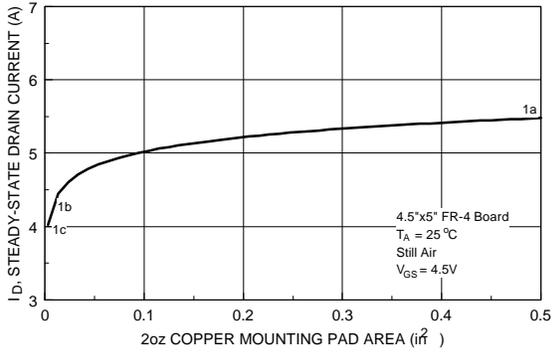
Figure 15. Maximum Steady-State Drain
Current versus Copper Mounting Pad
Area.
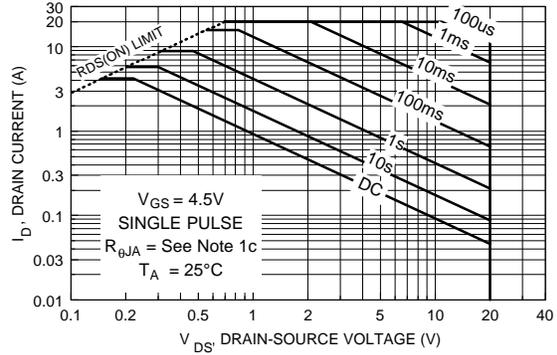
Figure 16. Maximum Safe Operating Area.
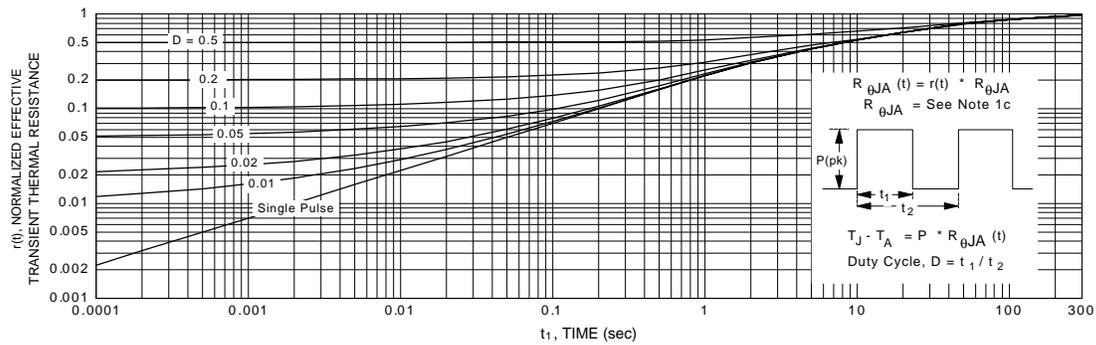
Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change
depending on the circuit board design.