Fully Accurate, 16-Bit, Unbuffered V_{OUT}, Quad SPI Interface, 2.7 V to 5.5 V *nano*DAC in a TSSOP

AD5066

FEATURES

Low power quad 16-bit *nano*DAC, ±1 LSB INL
Low total unadjusted error of ±0.1 mV typically
Low zero code error of 0.05 mV typically
Individually buffered reference pins
2.7 V to 5.5 V power supply
Specified over full code range of 0 to 65535
Power-on reset to zero scale or midscale
Per channel power-down with 3 power-down functions
Hardware $\overline{\text{LDAC}}$ with software $\overline{\text{LDAC}}$ override function
$\overline{\text{CLR}}$ function to programmable code
Small 16-lead TSSOP

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources

GENERAL DESCRIPTION

The AD5066 is a low power, 16-bit quad-channel, unbuffered voltage output *nano*DAC® offering relative accuracy specifications of ±1 LSB INL with individual reference pins and can operate from a single 2.7 V to 5.5 V supply. The AD5066 also offers a differential accuracy specification of ±1 LSB DNL. Reference buffers are also provided on-chip. The part uses a versatile 3-wire, low power Schmitt trigger serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and most DSP interface standards. The AD5066 incorporates a power-on reset circuit that ensures the DAC output powers up to zero scale or midscale and remains there until a valid write to the device takes place.

Total unadjusted error for the part is <0.8 mV. Zero code error for the part is 0.05 mV typically.

The AD5066 contains a power-down feature that reduces the current consumption of the device to typically 400 nA at 5 V and provides software selectable output loads while in power-down mode.

The outputs of all DACs can be updated simultaneously using the hardware $\overline{\text{LDAC}}$ function, with the added functionality of user software selectable DAC channels to update simultaneously. There is also an asynchronous $\overline{\text{CLR}}$ that clears all DACs to a software-selectable code—0 V, midscale, or full scale.

PRODUCT HIGHLIGHTS

1. Quad channel available in 16-lead TSSOP, ±1 LSB INL.
2. Individually buffered voltage reference pins.
3. TUE = ±0.8 mV max and zero code error = 0.1 mV max.
4. High speed serial interface with clock speeds up to 50 MHz.
5. Three power-down modes available to the user.
6. Reset to known output voltage (zero scale or midscale).

Table 1. Related Devices

Part No.	Description
AD5666	Quad,16-bit buffered DAC,16 LSB INL, TSSOP
AD5025/AD5045/AD5065[1]	Dual,12-/14-/16-bit buffered *nano*DAC, TSSOP
AD5024/AD5044/AD5064[1]	Quad 16-bit *nano*DAC, TSSOP
AD5062[1]	Single, 16-bit *nano*DAC, SOT-23
AD5063[1]	Single, 16-bit *nano*DAC, MSOP
AD5061	Single,16-bit *nano*DAC, ±4 LSB INL, SOT-23
AD5040/AD5060[1]	14-/16-bit *nano*DAC, SOT-23

[1] ±1 LSB INL

FUNCTIONAL BLOCK DIAGRAM

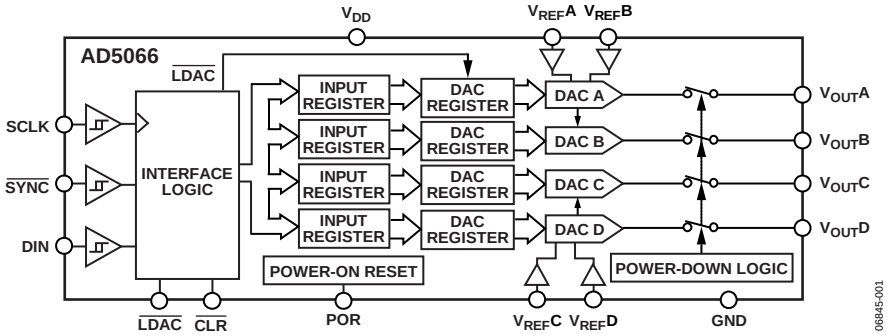

Figure 1.

Rev. A

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REVISION HISTORY

8/10—Rev. 0 to Rev. A

Change to Minimum $\overline{\text{SYNC}}$ High Time, Single Channel Update Parameter, Table 4 ... 5

7/09—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 2.0 V ≤ V_{REF}A, V_{REF}B, V_{REF}C, V_{REF}D ≤ V_{DD} − 0.4 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A Grade[1]			B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]								
Resolution	16			16			Bits	
Relative Accuracy (INL)		±0.5	±4		±0.5	±1	LSB	T_A = −40°C to +105°C
		±0.5	±4		±0.5	±2		T_A = −40°C to +125°C
Differential Nonlinearity (DNL)		±0.2	±1		±0.2	±1	LSB	
Total Unadjusted Error (TUE)		±0.1	±0.8		±0.1	±0.8	mV	V_{DD} = 2.7 V, V_{REF} = 2 V
Zero-Code Error		0.05	0.1		0.05	0.1	mV	All 0s loaded to the DAC register
Zero-Code Error Drift[3]		±0.5			±0.5		µV/°C	
Full-Scale Error		±0.01	±0.05		±0.01	±0.05	% FSR	All 1s loaded to the DAC register
Gain Error		±0.005	±0.05		±0.005	±0.05	% FSR	
Gain Error Drift[3]		±0.5			±0.5		ppm	ppm of FSR/°C
DC Crosstalk[3]		1	5		1	5	µV	Due to single-channel full-scale output change
		5	25		5	25	µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{REF}	0		V_{REF}	V	
DC Output Impedance (Normal Mode)		8			8		kΩ	Output impedance tolerance ± 10%
DC Output Impedance								DAC in power-down mode
Output Connected to 100 kΩ Network		100			100		kΩ	Output impedance tolerance ± 20 kΩ
Output Connected to 1 kΩ Network		1			1		kΩ	Output impedance tolerance ± 400 Ω
Power-Up Time[4]		2.9			2.9		µs	
DC PSRR		−120			−120		dB	V_{DD} ± 10%, DAC = full scale
REFERENCE INPUTS								
Reference Input Range	2		V_{DD} − 0.4	2		V_{DD} − 0.4	V	
Reference Current		0.002	±1		0.002	±1	µA	Per DAC channel
Reference Input Impedance		40			40		MΩ	Per DAC channel
LOGIC INPUTS[3]								
Input Current[5]			±1			±1	µA	
Input Low Voltage, V_{INL}			0.8			0.8	V	
Input High Voltage, V_{INH}	2.2			2.2			V	
Pin Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD}								DAC active, excludes load current V_{IH} = V_{DD} and V_{IL} = GND
Normal Mode[6]		2.5	3		2.5	3	mA	
All Power-Down Modes[7]		0.4			0.4		µA	

[1] Temperature range is −40°C to +125°C, typical at 25°C.
[2] Linearity calculated using a code range of 0 to 65,535; output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Time taken to exit power-down mode and enter normal mode, 32nd clock edge to 90% of DAC midscale value, output unloaded.
[5] Current flowing into individual digital pins. V_{DD} = 5.5 V; V_{REF} = 4.096 V; Code = midscale.
[6] Interface inactive. All DACs active. DAC outputs unloaded.
[7] All four DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 2.0 V ≤ $V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ ≤ V_{DD} − 0.4 V all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
DYNAMIC PERFORMACE					
Output Voltage Settling Time		7.5	10	µs	¼ to ¾ scale settling to ±2 LSB, single channel update, output unloaded
Output Voltage Settling Time		12	15	µs	¼ to ¾ scale settling to ±2 LSB, all channel update, output unloaded
Slew Rate		1.7		V/µs	
Digital-to-Analog Glitch Impulse		3		nV-sec	1 LSB change around major carry
Reference Feedthrough		−70		dB	V_{REF} = 3 V ± 0.5 V p-p, frequency = 60 Hz to 20 MHz
Digital Feedthrough		0.02		nV-sec	
Digital Crosstalk		1.7		nV-sec	
Analog Crosstalk		3.7		nV-sec	
DAC-to-DAC Crosstalk		5.4		nV-sec	
Total Harmonic Distortion		−83		dB	V_{REF} = 3 V ± 0.2 V p-p, frequency = 10 kHz
Output Noise Spectral Density		30		nV/√Hz	DAC code = 0x8000, 1 kHz
		25		nV/√Hz	DAC code = 0x8000, 10 kHz
Output Noise		4.7		µV p-p	0.1 Hz to 10 Hz

[1] Temperature range is −40°C to +125°C, typical at +25°C.
[2] See the Terminology section.
[3] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$, V_{DD} = 2.7 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 2.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SCLK Cycle Time	t_1	20			ns
SCLK High Time	t_2	10			ns
SCLK Low Time	t_3	10			ns
$\overline{SYNC}$ to SCLK Falling Edge Set-Up Time	t_4	17			ns
Data Set-Up Time	t_5	5			ns
Data Hold Time	t_6	5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	5		30	ns
Minimum $\overline{SYNC}$ High Time	t_8				
Single Channel Update		3			µs
All Channel Update		8			µs
$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore	t_9	17			ns
$\overline{LDAC}$ Pulse Width Low	t_{10}	20			ns
SCLK Falling Edge to $\overline{LDAC}$ Rising Edge	t_{11}	20			ns
$\overline{CLR}$ Pulse Width Low	t_{12}	10			ns
SCLK Falling Edge to $\overline{LDAC}$ Falling Edge	t_{13}	10			ns
$\overline{CLR}$ Pulse Activation Time	t_{14}	10.6			µs

[1] Maximum SCLK frequency is 50 MHz. Guaranteed by design and characterization; not production tested.

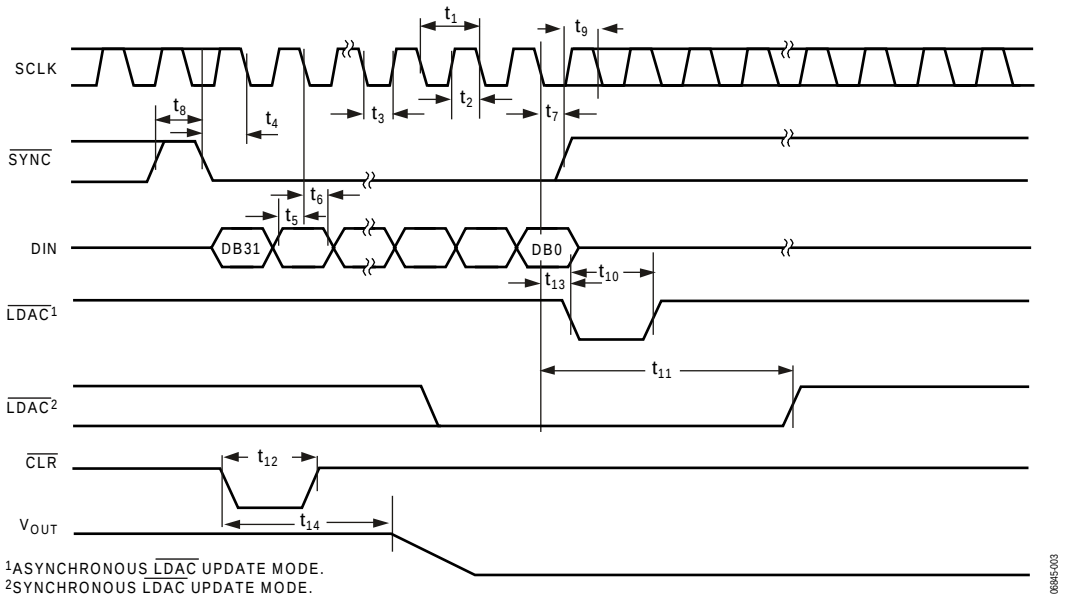

Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT}x to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF}x to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	+150°C
TSSOP Package	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

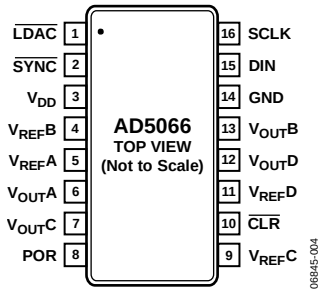

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Load DAC. Logic input. This is used to update the DAC register and, consequently, the analog outputs. When tied permanently low, the addressed DAC register is updated on the falling edge of the 32nd clock. If $\overline{\text{LDAC}}$ is held high during the write cycle, the addressed DAC input shift register is updated but the output is held off until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. The AD5066 can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{REF}B$	External Reference Voltage Input for DAC B.
5	$V_{REF}A$	External Reference Voltage Input for DAC A.
6	$V_{OUT}A$	Unbuffered Analog Output Voltage from DAC A.
7	$V_{OUT}C$	Unbuffered Analog Output Voltage from DAC C.
8	POR	Power-On Reset Pin. Tying this pin to GND powers the DAC outputs to zero scale on power-up. Tying this pin to V_{DD} powers the DAC outputs to midscale.
9	$V_{REF}C$	External Reference Voltage Input for DAC C.
10	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
11	$V_{REF}D$	External Reference Voltage Input for DAC D.
12	$V_{OUT}D$	Unbuffered Analog Output Voltage from DAC D.
13	$V_{OUT}B$	Unbuffered Analog Output Voltage from DAC B.
14	GND	Ground Reference Point for All Circuitry on the Part.
15	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

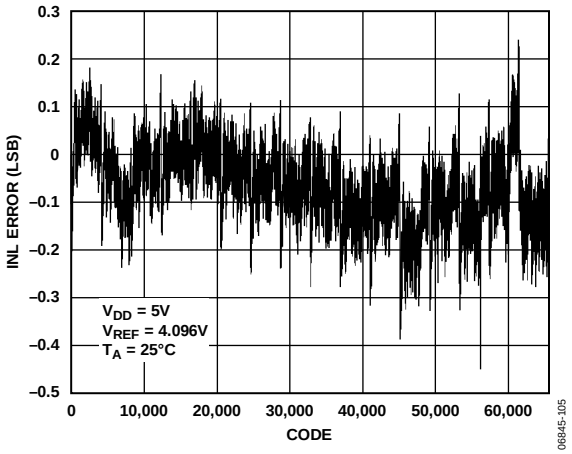

Figure 4. INL Error vs. Code

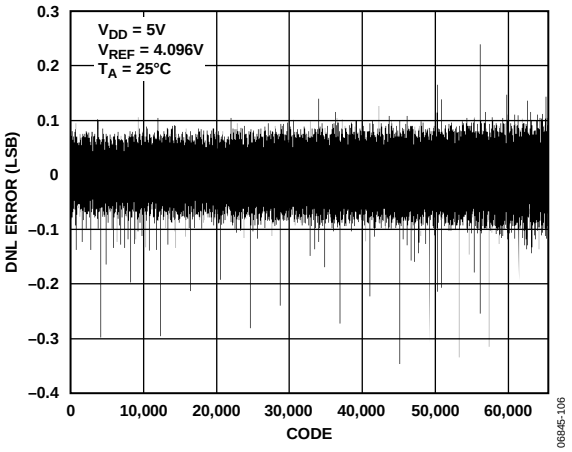

Figure 5. DNL Error vs. Code

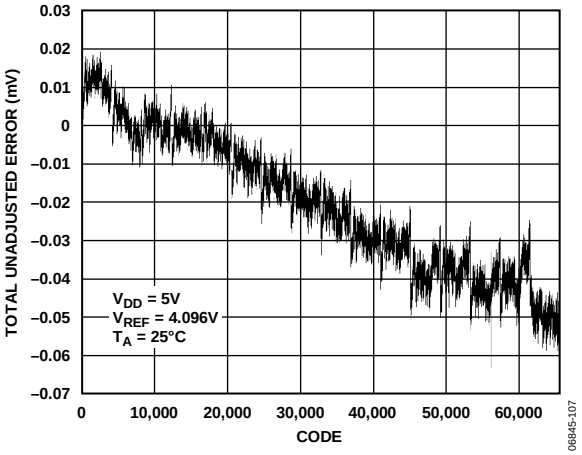

Figure 6. Total Unadjusted Error vs. Code

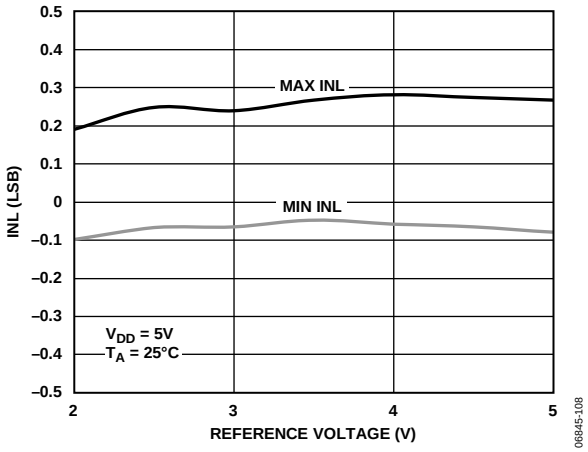

Figure 7. INL vs. Reference Input Voltage

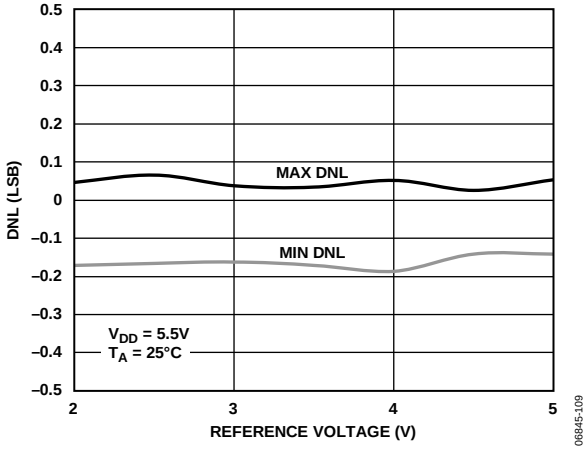

Figure 8. DNL vs. Reference Input Voltage

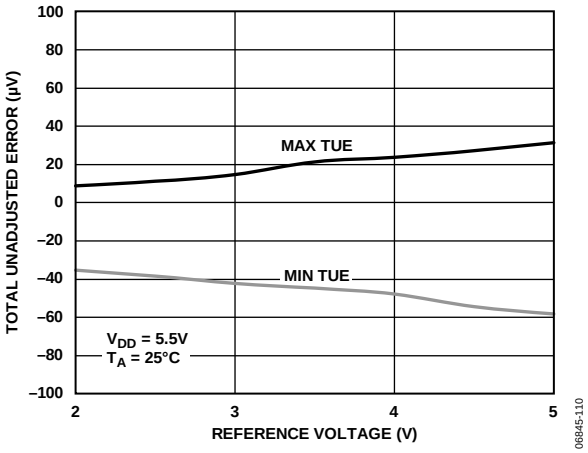

Figure 9. Total Unadjusted Error vs. Reference Input Voltage

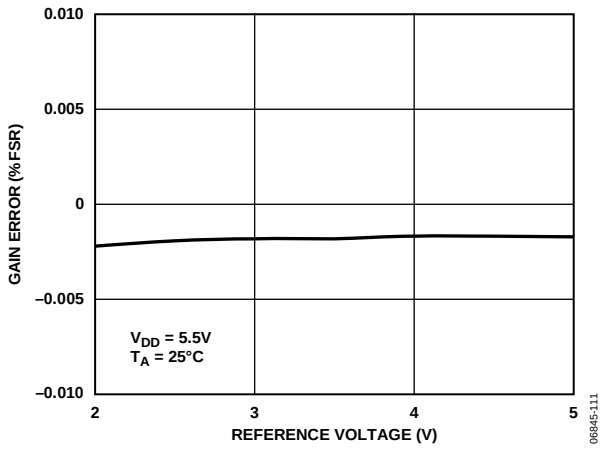

Figure 10. Gain Error Vs. Reference Input Voltage

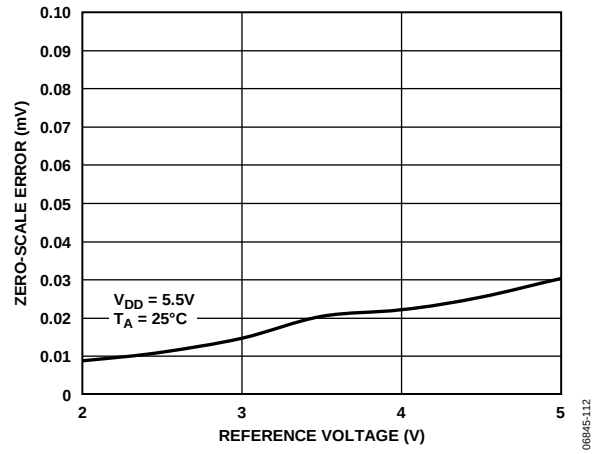

Figure 11. Zero-Code Error Vs. Reference Input Voltage

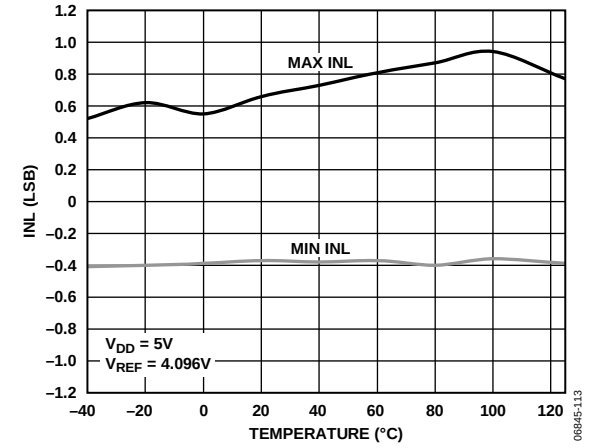

Figure 12. INL vs. Temperature

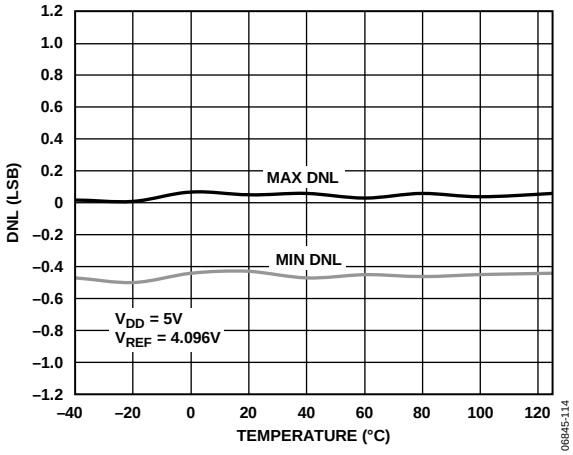

Figure 13. DNL vs. Temperature

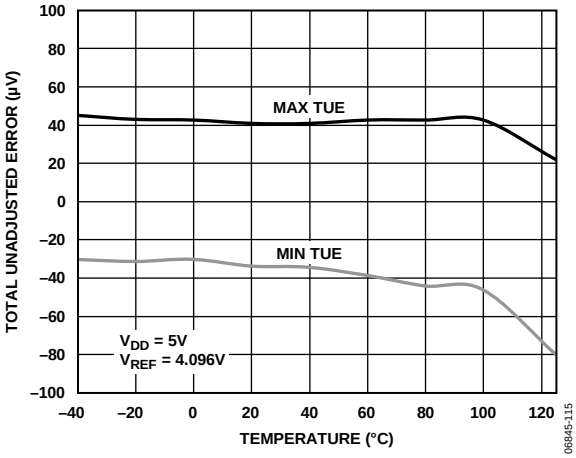

Figure 14. Total Unadjusted Error vs. Temperature

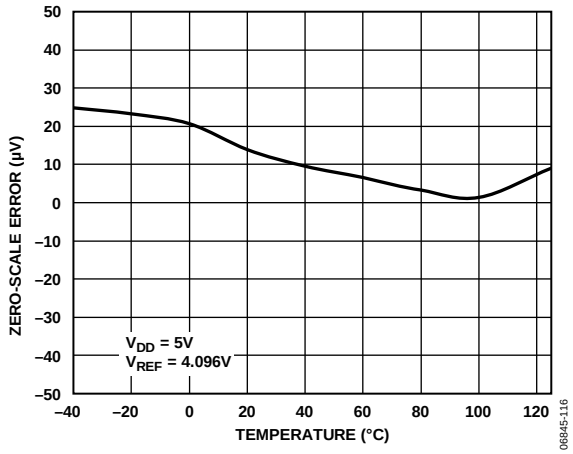

Figure 15. Zero-Code Error vs. Temperature

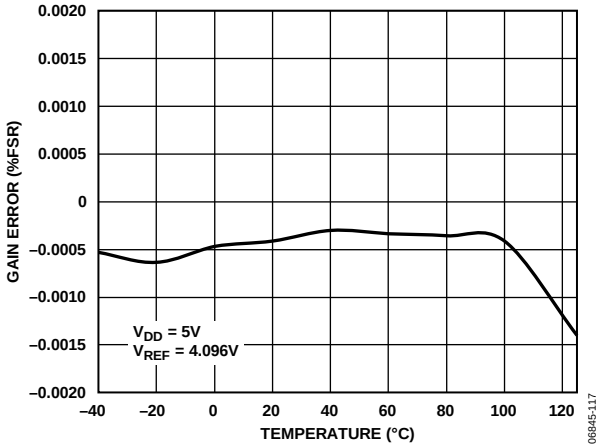

Figure 16. Gain Error vs. Temperature

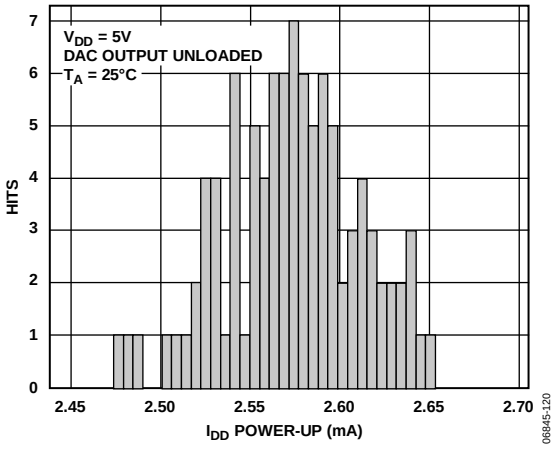

Figure 19. I_{DD} Histogram V_{DD} = 5.5 V

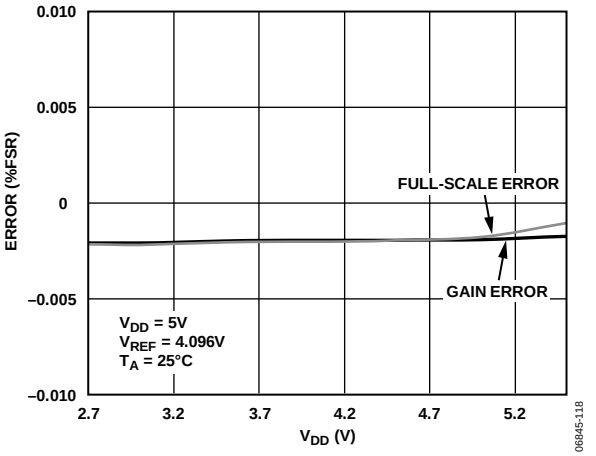

Figure 17. Gain Error and Full-Scale Error vs. Supply Voltage

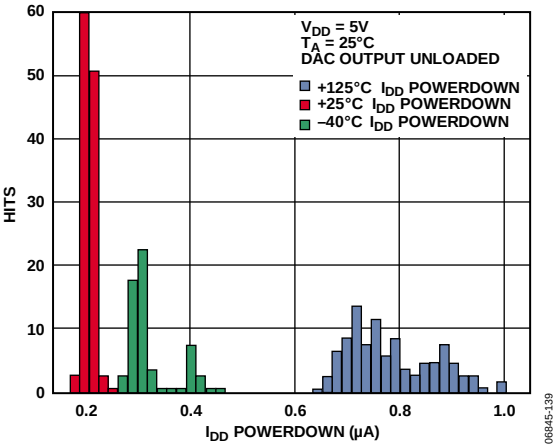

Figure 20. I_{DD} Power-Down Histogram

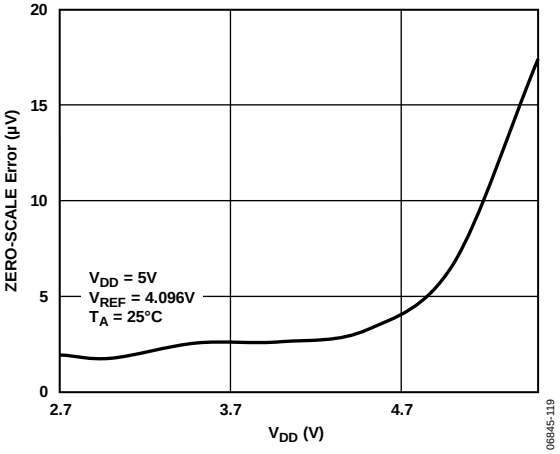

Figure 18. Zero-Code Error vs. Supply Voltage

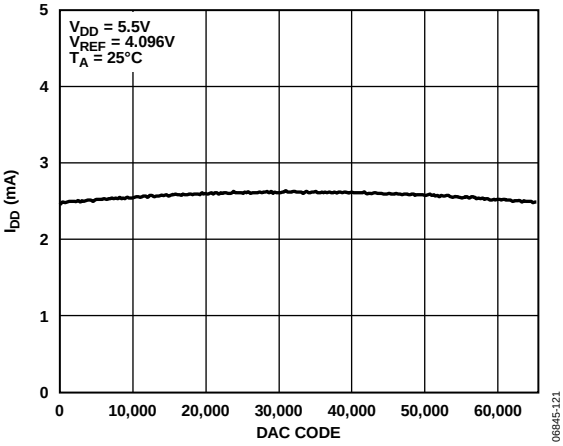

Figure 21. I_{DD} vs. Code

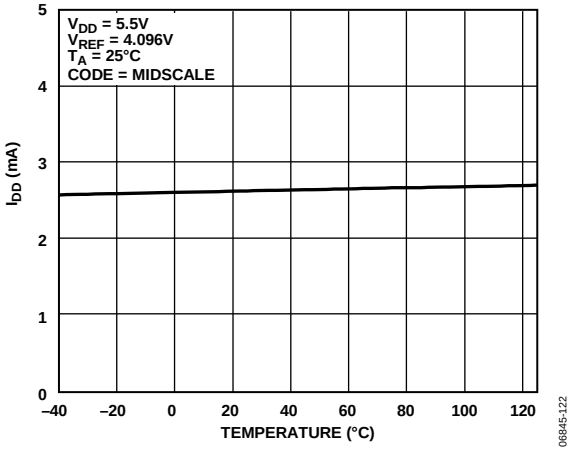

Figure 22. I_{DD} vs. Temperature

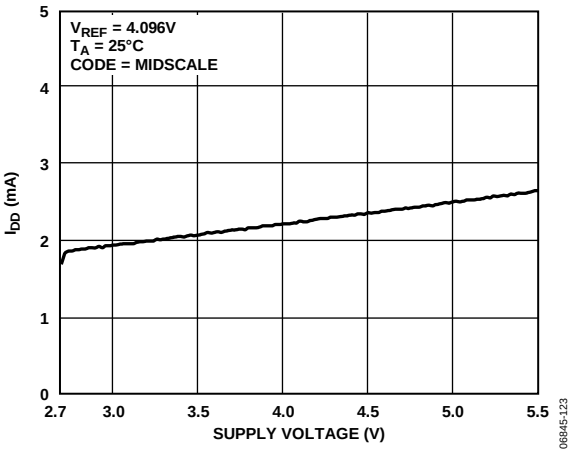

Figure 23. I_{DD} vs. Supply Voltage

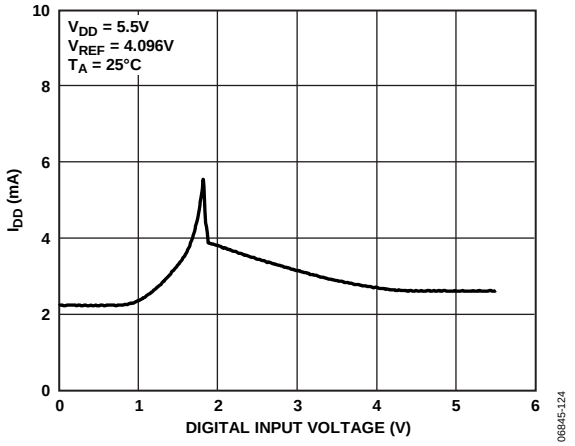

Figure 24. I_{DD} vs. Digital Input Voltage

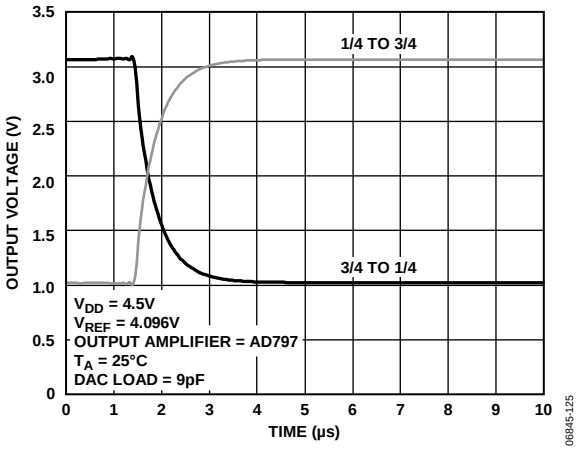

Figure 25. Settling Time

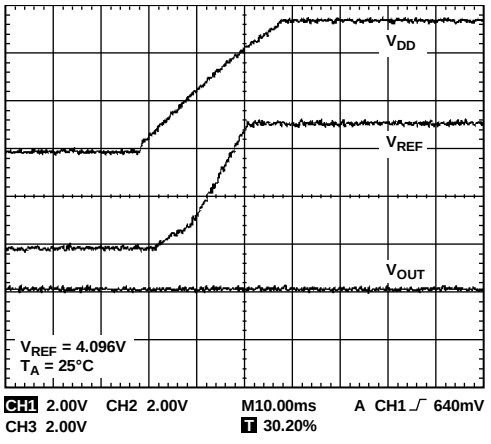

Figure 26. POR to 0 V

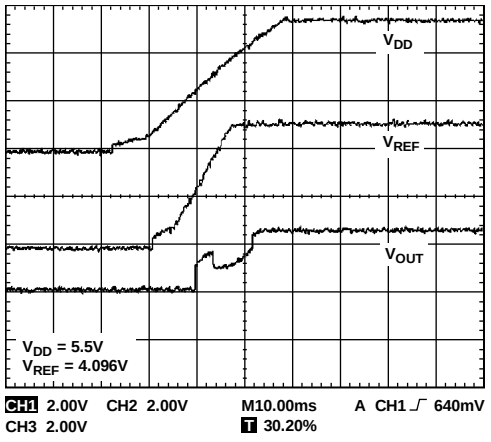

Figure 27. POR to MS

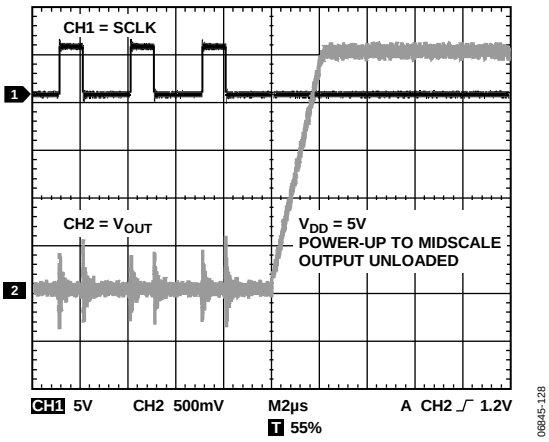

Figure 28. Exiting PD to MS

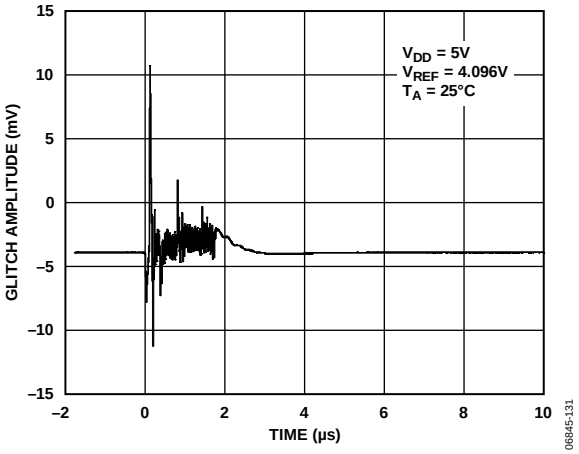

Figure 31. Digital Crosstalk

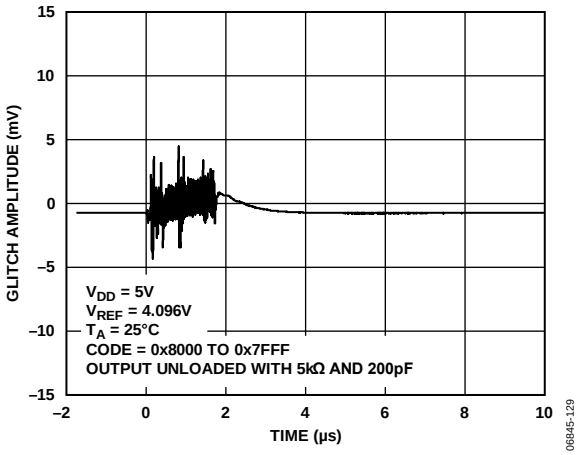

Figure 29. Glitch

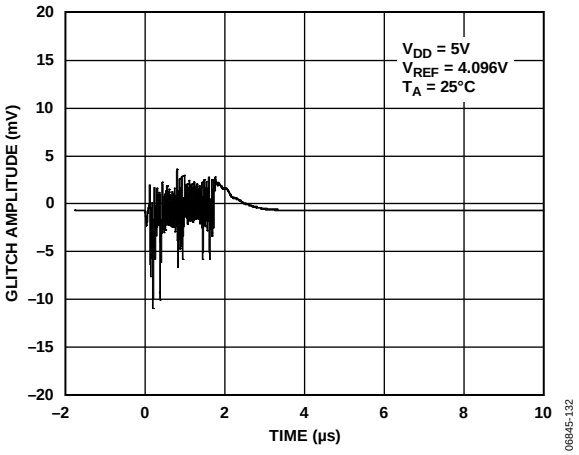

Figure 32. DAC-to-DAC Crosstalk

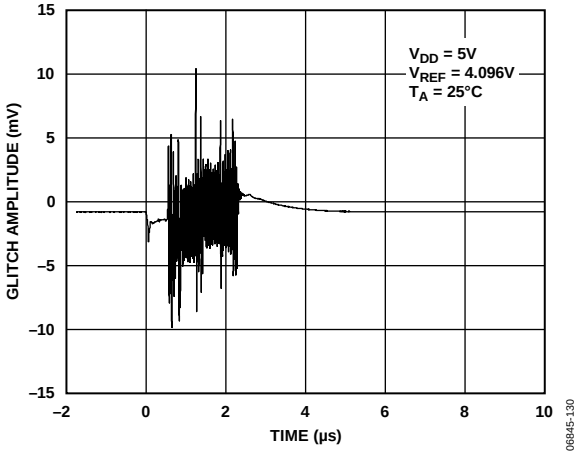

Figure 30. Analog Crosstalk

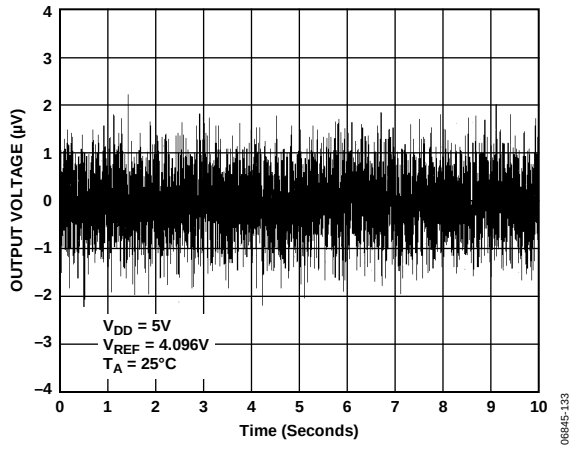

Figure 33. 1/f Noise

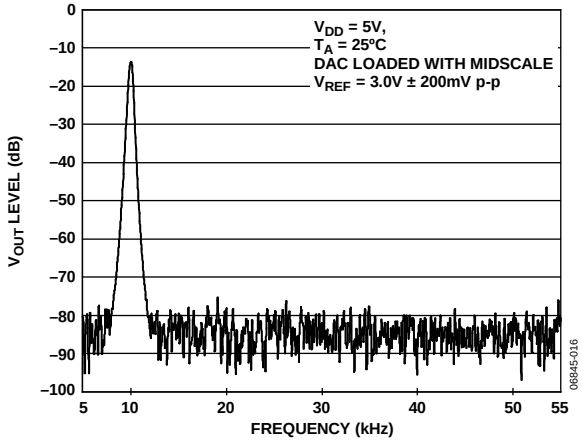

Figure 34. Total Harmonic Distortion

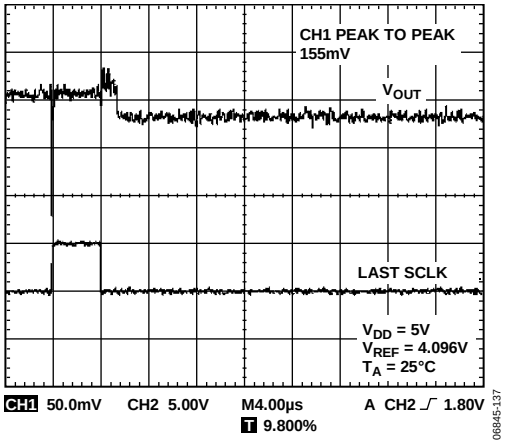

Figure 37. Glitch Upon Entering Power Down

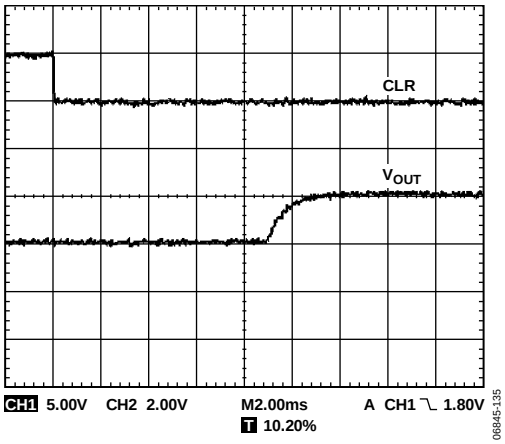

Figure 35. Hardware $\overline{CLR}$

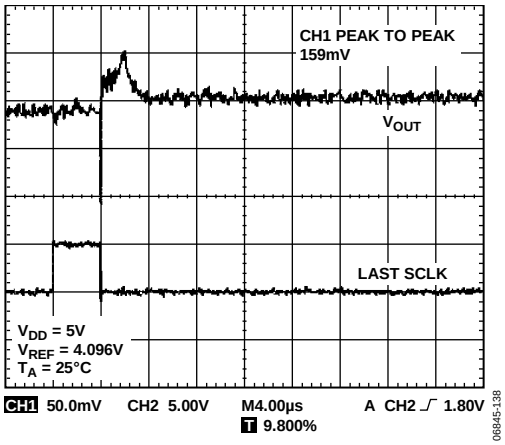

Figure 38. Glitch Upon Exiting Power Down

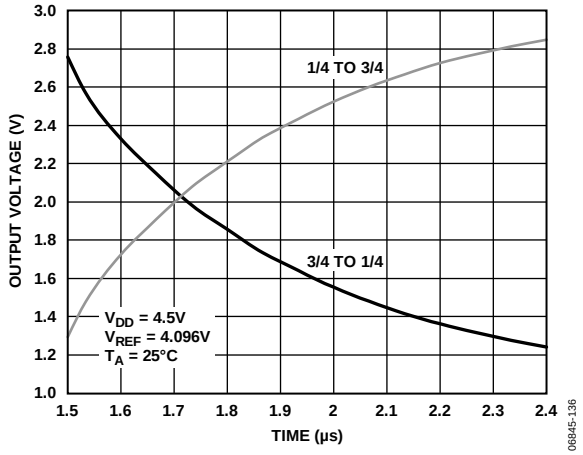

Figure 36. Slew Rate

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy or INL is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 4, Figure 5, and Figure 6 show typical INL vs. code plots.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Figure 7, Figure 8, and Figure 9 show typical DNL vs. code plots.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5066, because the output of the DAC cannot go below 0 V. Zero-code error is expressed in millivolts. Figure 17 shows a typical zero-code error vs. supply voltage plot.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in microvolts per degrees Celsius.

Full-Scale Error
Full-scale error is a measure of the output error when a full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{REF} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts per second and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 28.

DC Power Supply Rejection Ratio (PSRR)
DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. DC PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nanovolts per second and measured with one simultaneous DIN and SCLK pulse loaded to the DAC.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nanovolts per second.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nanovolts per second.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nanovolts per second.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5066 is a quad 16-bit, serial input, voltage output *nano*DAC. The part operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5066 in a 32-bit word format via a 3-wire serial interface. The AD5066 incorporates a power-on reset circuit to ensure the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to typically 400 nA.

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 65,535).
N is the DAC resolution.

DAC ARCHITECTURE

The DAC architecture of the AD5066 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 39. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either GND or the V_{REF} buffer output. The remaining 12 bits of the data word drive the S0 to S11 switches of a 12-bit voltage mode R-2R ladder network.

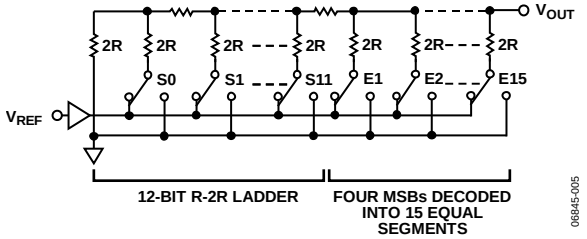

Figure 39. DAC Ladder Structure

REFERENCE BUFFER

The AD5066 operates with an external reference. Each of the four on-board DACs has a dedicated voltage reference pin that is buffered. The reference input pin has an input range of 2 V to V_{DD} − 0.4 V. This input voltage is then used to provide a buffered reference for the DAC core.

SERIAL INTERFACE

The AD5066 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, MICROWIRE, and most DSP interface standards. See Figure 2 for a timing diagram of a typical write sequence.

INPUT SHIFT REGISTER

The input shift register is 32 bits wide (see Figure 40). The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 7), followed by the 4-bit DAC address bits, A3 to A0 (see Table 8), and finally the bit data-word. The data-word comprises of a 16-bit input code followed by four don't care bits (see Figure 40). These data bits are transferred to the Input register on the 32nd falling edge of SCLK. Commands can be executed on individually selected DAC channels or on all DACs.

Table 7. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n
0	0	0	1	Transfer contents of Input Register n to DAC Register n
0	0	1	0	Write to Input Register n and update all DAC Registers
0	0	1	1	Write to Input Register n and update DAC Register n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Reserved
1	0	0	1	Reserved
1	1	1	1	Reserved

Table 8. DAC Input Register Address Bits

Address (n)				
A3	A2	A1	A0	Selected DAC Channel
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

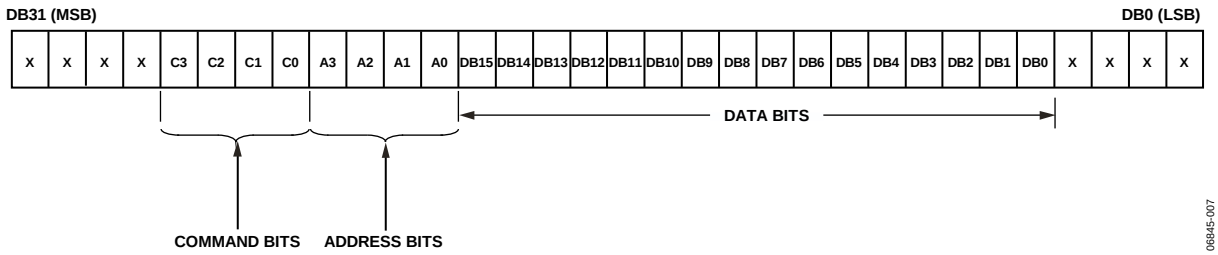

Figure 40. Input Shift Register Content

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Bringing the $\overline{\text{SYNC}}$ line low enables the DIN and SCLK input buffers. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5066 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in, and the programmed function is executed, that is, a change in the input register contents (see Table 8) and/or a change in the mode of operation. At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 2 µs (single-channel update, see the t_8 parameter in Table 4) before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Idle $\overline{\text{SYNC}}$ high between write sequences for even lower power operation of the part.

$\overline{\text{SYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The input shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 42).

Power-Down Modes

The AD5066 can be configured through software, in one of four different modes: normal mode (default) and three separate power-down modes (see Table 9). Any or all DACs can be powered down. Command 0100 is reserved for the power-down function (see Table 7). These power-down modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the input shift register. Table 9 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC A to DAC D) can be powered down to the selected mode by setting the corresponding four bits (DB3, DB2, DB1, DB0) to 1. See Table 10 for the contents of the input shift register during power-down/power-up operation.

When Bit DB9 and Bit DB8 in the control register are set to 0, the part is configured in normal mode with its normal power consumption of 2.5 mA at 5 V. However, for the three power-down modes, the supply current falls to 0.4 µA if all the channels are powered down. Not only does the supply current fall, but the output pin is also internally switched from the output of the DAC to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 41.

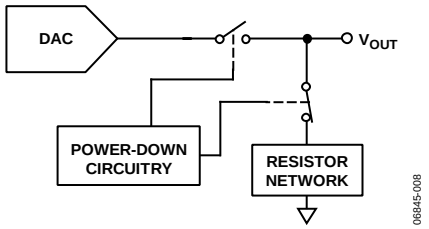

Figure 41. Output Stage During Power-Down Mode

The bias generator, DAC core, and other associated linear circuitry are shut down when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down mode. The time to exit power-down mode is typically 2.9 µs (see Figure 27).

Table 9. Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

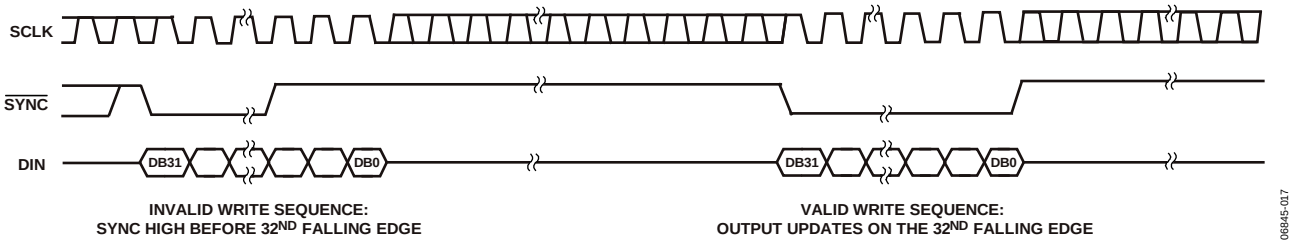

Figure 42. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-ON RESET

The AD5066 contains a power-on reset circuit that controls the output voltage during power-up. By connecting the POR pin low, the AD5066 output powers up to 0 V; by connecting the POR pin high, the AD5066 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 7). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

Table 10. 32-Bit Input Shift Register Contents for Power-Up/Power-Down Function

MSB **LSB**

DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23 to DB20**	**DB10 to DB19**	**DB9**	**DB8**	**DB4 to DB7**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	0	0	X	X	PD1	PD0	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C2 to C0)				Address bits (A3 to A0)—don't cares	Don't cares	Power-down mode		Don't cares	Power-down/power-up channel selection—set bit to 1 to select			

CLEAR CODE REGISTER

The AD5066 has a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly (see Table 11). This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the control register (see Table 11). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 7).

Table 11. Clear Code Register

DB1 (CR1)	DB0 (CR0)	Clears to Code
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time (the falling edge of $\overline{CLR}$ to when the output starts to change) is typically 10.6 µs. See Table 13 for contents of the input shift register during the loading clear code register operation.

$\overline{LDAC}$ FUNCTION

Hardware $\overline{LDAC}$ Pin

The outputs of all DACs can be updated simultaneously using the hardware LDAC pin, as shown in Figure 2. There are two methods of using the hardware LDAC pin: synchronously ($\overline{LDAC}$ permanently low) and asynchronously ($\overline{LDAC}$ pulsed).

Synchronous $\overline{LDAC}$: $\overline{LDAC}$ is held permanently low. After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse, provided $\overline{LDAC}$ is held low.

Asynchronous $\overline{LDAC}$: $\overline{LDAC}$ is held high then pulsed low to update. The outputs are not updated at the same time that the input registers are written to. When $\overline{LDAC}$ is pulsed low, the DAC registers are updated with the contents of the input registers.

Command 0001, 0010 and 0011 (see Table 7) update the DAC Register/Registers, regardless of the level of the $\overline{LDAC}$ pin

Software $\overline{LDAC}$ Function

Writing to the DAC using Command 0110 loads the 4-bit $\overline{LDAC}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{LDAC}$ pin works normally. Setting the bits to 1 updates the DAC channel regardless of the state of the hardware $\overline{LDAC}$ pin, so that it effectively sees the hardware $\overline{LDAC}$ pin as being tied low (see Table 12 for the LDAC register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the remainder of the channels are synchronously updating.

Table 12. Load $\overline{LDAC}$ Register

$\overline{LDAC}$ Bits (DB3 to DB0)	$\overline{LDAC}$ Pin	$\overline{LDAC}$ Operation
0	1/0	Determined by $\overline{LDAC}$ pin
1	X[1]	DAC channels update, overrides the $\overline{LDAC}$ pin; DAC channels see $\overline{LDAC}$ as 0

[1] X = don't care.

The $\overline{LDAC}$ register gives the user extra flexibility and control over the hardware $\overline{LDAC}$ pin (see Table 14). Setting the $\overline{LDAC}$ bits (DB0 to DB3) to 0 for a DAC channel means that this channel's update is controlled by the hardware $\overline{LDAC}$ pin.

Table 13. 32-Bit Input Shift Register Contents for Clear Code Function

MSB											LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB2 to DB19**	**DB1**	**DB0**
X	0	1	0	1	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	Clear code register (CR1 to CR0)	

Table 14. 32-Bit Input Shift Register Contents for $\overline{LDAC}$ Overwrite Function

MSB										LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23 to DB20**	**DB4 to DB19**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	1	0	X	X	DAC D	DAC C	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares	Don't cares	Setting $\overline{LDAC}$ bit to 1 override $\overline{LDAC}$ pin			

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5066 should have separate analog and digital sections. If the AD5066 is in a system where other devices require an AGND-to-DGND connection, make the connection at one point only and as close as possible to the AD5066.

Bypass the power supply to the AD5066 with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 μF capacitor, ideally, right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor has low effective series resistance and low effective series inductance, typical of common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield the clocks and other fast switching digital signals from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

MICROPROCESSOR INTERFACING

AD5066 to Blackfin® ADSP-BF53X Interface

Figure 43 shows a serial interface between the AD5066 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5066, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5066, TSCLK0 drives the SCLK of the parts, and TFS0 drives $\overline{\text{SYNC}}$.

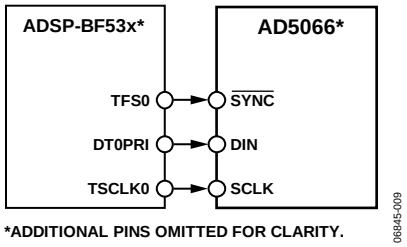

Figure 43. AD5066 to Blackfin ADSP-BF53X Interface

AD5066 to 68HC11/68L11 Interface

Figure 44 shows a serial interface between the AD5066 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5066, and the MOSI output drives DIN of the DAC. A port line (PC7) drives the $\overline{\text{SYNC}}$ signal.

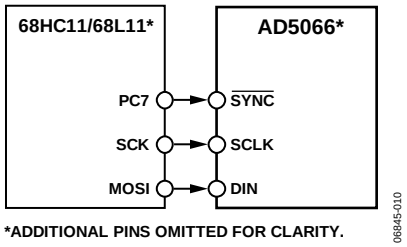

Figure 44. AD5066 to 68HC11/68L11 Interface

The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 is configured with its CPOL bit as 0, and the CPHA bit as 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as described previously, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5066, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

AD5066 to 80C51/80L51 Interface

Figure 45 shows a serial interface between the AD5066 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5066, RxD drives DIN on the AD5066, and a bit-programmable pin on the port (P3.3) drives the $\overline{\text{SYNC}}$ signal. When data is to be transmitted to the AD5066, P3.3 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second, third, and fourth write cycle is initiated to transmit the second, third, and fourth byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5066 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

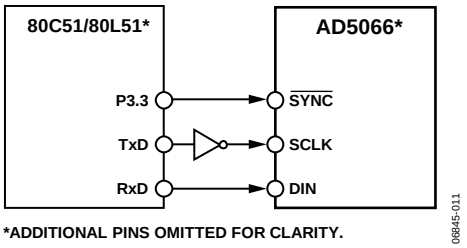

Figure 45. AD5066 to 80C512/80L51 Interface

AD5066 to MICROWIRE Interface

Figure 46 shows an interface between the AD5066 and any MICROWIRE-compatible device. Serial data is clocked into the AD5066 on the falling edge of the SCLK.

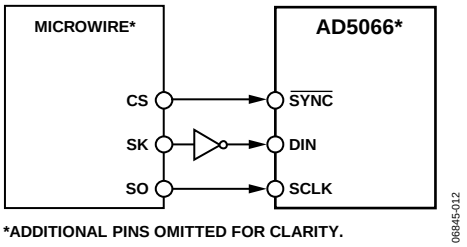

Figure 46. AD5066 to MICROWIRE Interface

APPLICATIONS INFORMATION

USING A REFERENCE AS A POWER SUPPLY

Because the supply current required by the AD5066 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the parts (see Figure 47). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5066. If the low dropout REF195 is used, it must supply 2.5 mA of current to the AD5066 with no load on the output of the DAC.

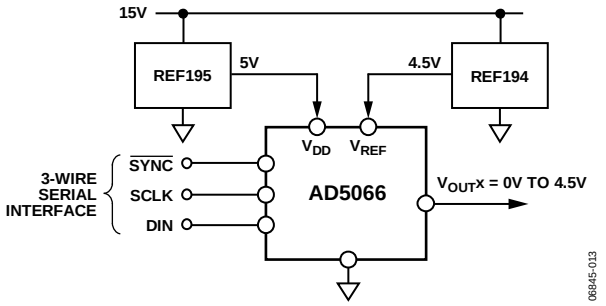

Figure 47. REF195 as a Power Supply to the AD5066

BIPOLAR OPERATION

The AD5066 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 48. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achieved using an AD8638 or AD8639 the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where:
D = the input code in decimal (0 to 65,535).
V_{DD} = 5 V.
$R1 = R2 = 10\ \text{k}\Omega$.

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5\ \text{V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

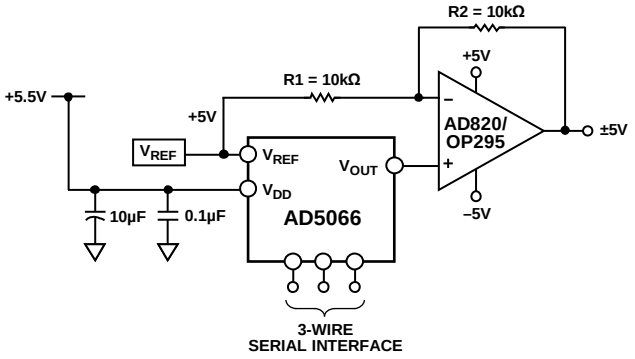

Figure 48. Bipolar Operation with the AD5066

USING THE AD5066 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. The AD5066 uses a 3-wire serial logic interface, so the ADuM1300 three-channel digital isolator provides the required isolation (see Figure 49). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5066.

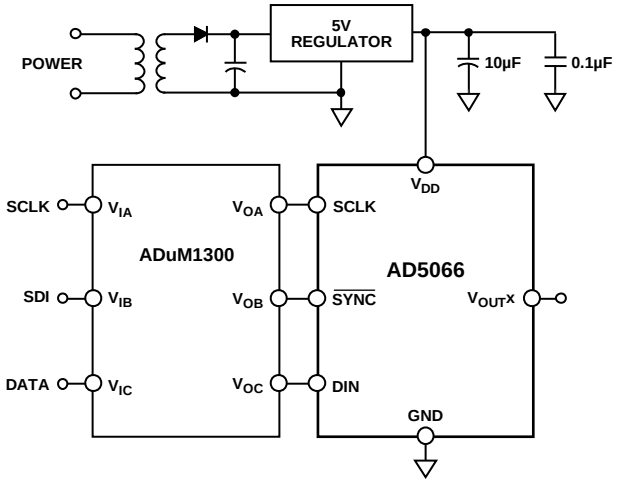

Figure 49. AD5066 with a Galvanically Isolated Interface

OUTLINE DIMENSIONS

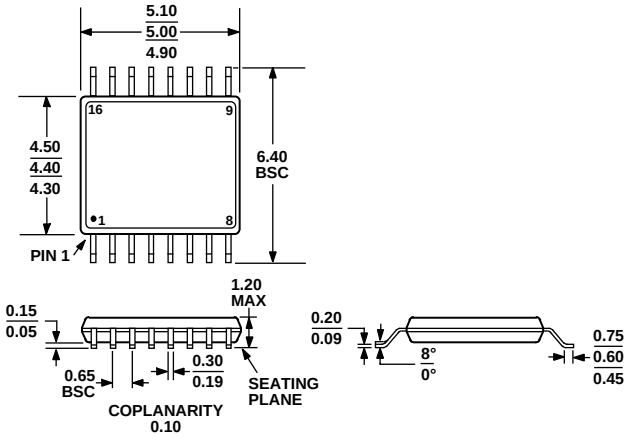

Figure 50. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeter

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Power-On Reset to Code	Accuracy	Resolution
AD5066BRUZ	−40°C to +125°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	16 bits
AD5066BRUZ-REEL7	−40°C to +125°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	16 bits
AD5066ARUZ	−40°C to +125°C	16-Lead TSSOP	RU-16	Zero	±4 LSB INL	16 bits
AD5066ARUZ-REEL7	−40°C to +125°C	16-Lead TSSOP	RU-16	Zero	±4 LSB INL	16 bits

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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