# N-channel 650 V, 0.85 Ω typ., 4.5 A MDmesh M2 Power MOSFET in a PowerFLAT 5x6 HV package
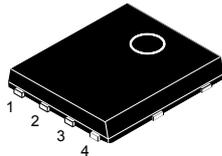
PowerFLAT 5x6 HV
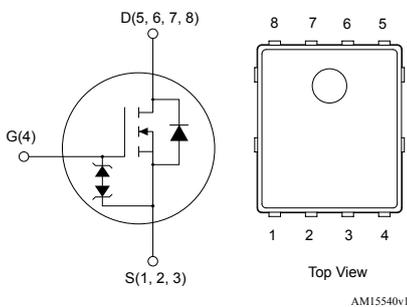
Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL10N65M2	650 V	1.00 Ω	4.5 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Product status link
STL10N65M2

Product summary	
Order code	STL10N65M2
Marking	10N65M2
Package	PowerFLAT 5x6 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	4.5	A
	Drain current (continuous) at T_C = 100 °C	2.8	A
I_{DM} [1]	Drain current pulsed	18	A
P_{TOT}	Total power dissipation at T_C = 25 °C	48	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	0.9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	95	mJ
dv/dt [2]	Peak diode recovery voltage slope	15	V/ns
dv/dt [3]	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD} \leq 4.5$ A, di/dt ≤ 400 A/µs, $V_{DS(peak)} \leq V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *$V_{DS} \leq 520$ V.*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.6	°C/W
$R_{thj\text{-}pcb}$ [1]	Thermal resistance junction-pcb	50	°C/W

1. *When mounted on 1 inch² FR-4 board, 2 oz Cu.*

2 Electrical characteristics

$T_C = 25$ °C unless otherwise specified

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V, $I_D = 1$ mA	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0$ V, $V_{DS} = 650$ V			1	µA
		$V_{GS} = 0$ V, $V_{DS} = 650$ V, $T_C = 125$ °C [1]			100	µA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0$ V, $V_{GS} = \pm 25$ V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10$ V, $I_D = 2.5$ A		0.85	1.00	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100$ V, f = 1 MHz, $V_{GS} = 0$ V	-	310	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	0.9	-	pF
$C_{oss\ eq.}$ [1]	Equivalent capacitance energy related	$V_{DS} = 0$ to 520 V, $V_{GS} = 0$ V	-	109	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	6.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520$ V, $I_D = 5$ A	-	10.3	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0$ to 10 V	-	2.4	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	4.8	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325$ V, $I_D = 2.5$ A,	-	7.5	-	ns
t_r	Rise time	$R_G = 4.7$ Ω, $V_{GS} = 10$ V	-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	22.5	-	ns
t_f	Fall time	Figure 18. Switching time waveform)	-	18	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
I_{SDM} [1]	Source-drain current (pulsed)		-		18	A
V_{SD} [2]	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	276		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	1.7		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	312		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	1.9		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12.4		A

1. *Pulse width is limited by safe operating area.*

2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1   Electrical characteristics (curves)

Figure 1. Safe operating area
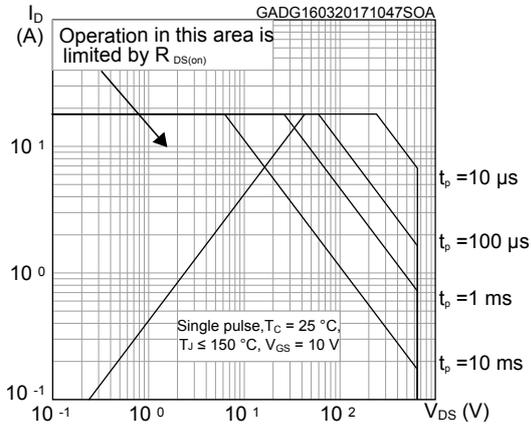
Figure 2. Thermal impedance

$$Z_{th} = k \; R_{thJ-c}$$
$$\delta = t_p / \tau$$
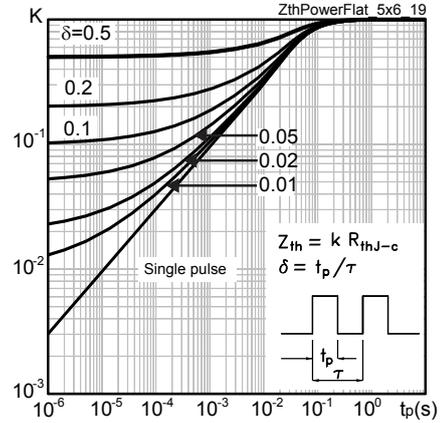
Figure 3. Output characteristics
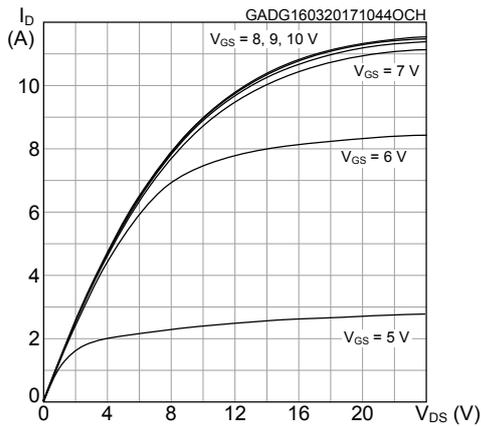
**Figure 4. Transfer characteristics**
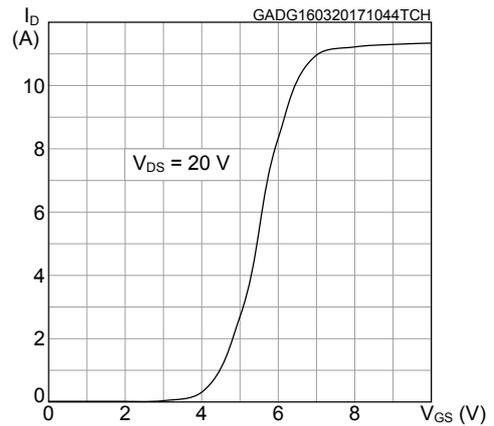
**Figure 5. Gate charge vs gate-source voltage**
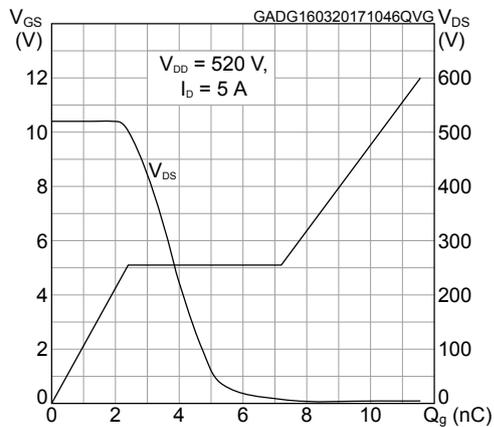
Figure 6. Static drain-source on-resistance
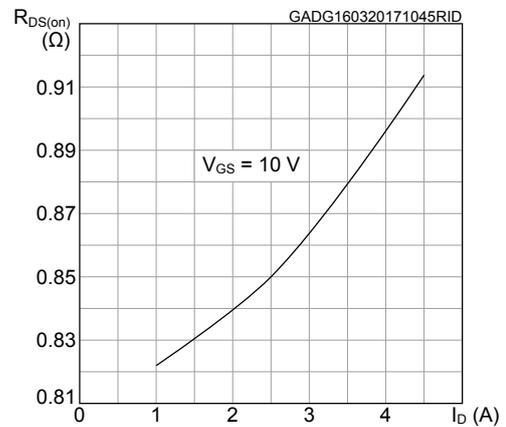
**Figure 7. Capacitance variations**
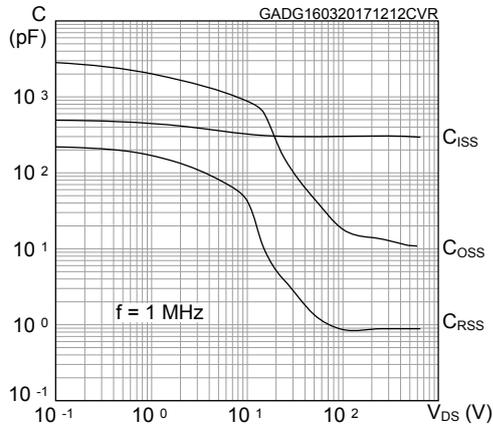
**Figure 8. Output capacitance stored energy**
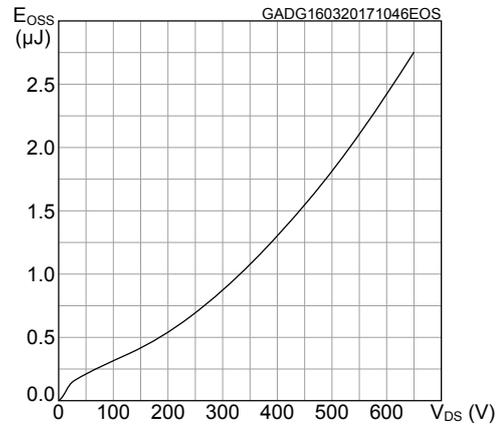
Figure 9. Normalized gate threshold voltage vs temperature
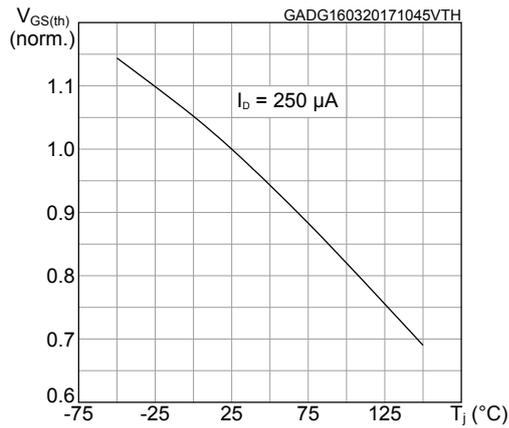
Figure 10. Normalized on-resistance vs temperature
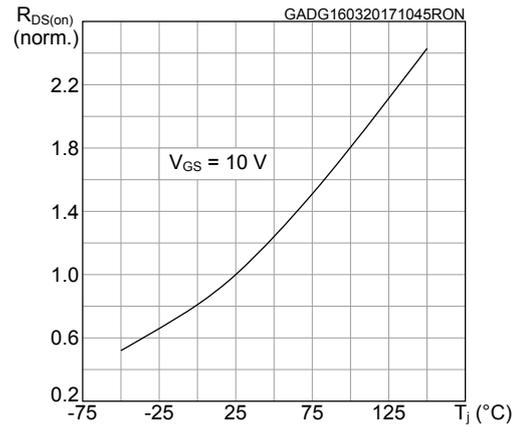

**Figure 11. Normalized $V_{(BR)DSS}$ vs temperature**
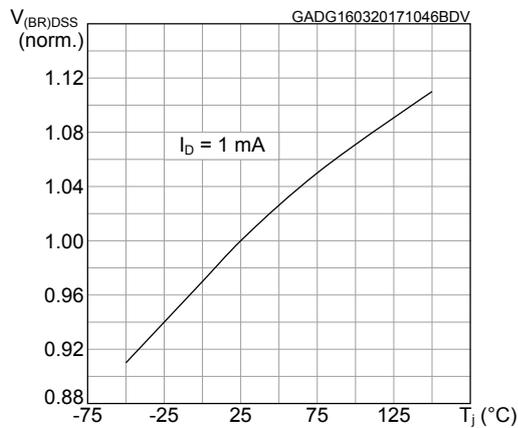
**Figure 12. Source-drain diode forward characteristics**
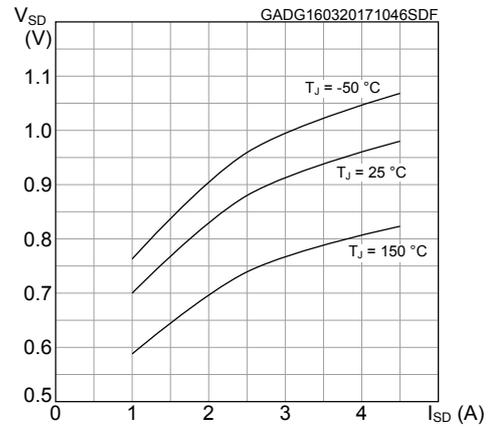
3 Test circuits

Figure 13. Test circuit for resistive load switching times
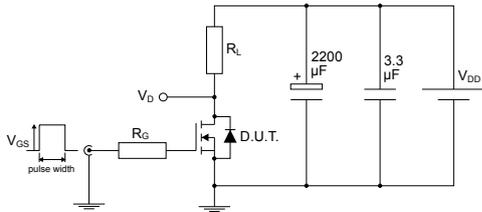

AM01468v1

**Figure 14. Test circuit for gate charge behavior**
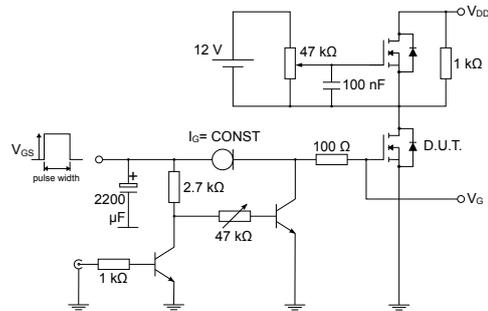
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Figure 15. Test circuit for inductive load switching and diode recovery times
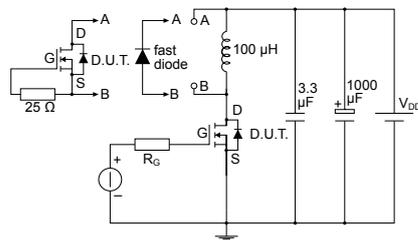
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Figure 16. Unclamped inductive load test circuit
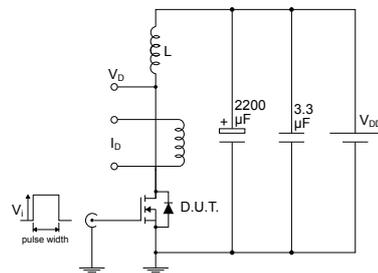
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Figure 17. Unclamped inductive waveform
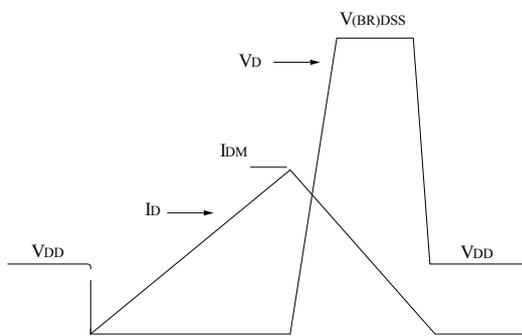
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**Figure 18. Switching time waveform**
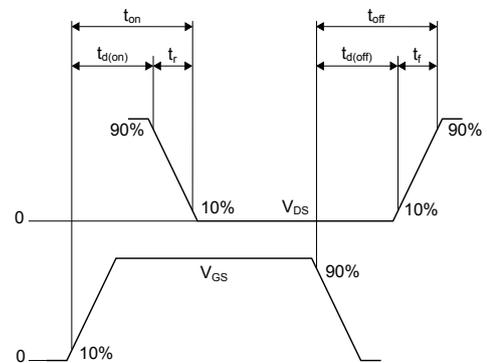
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 HV package information

Figure 19. PowerFLAT 5x6 HV package outline
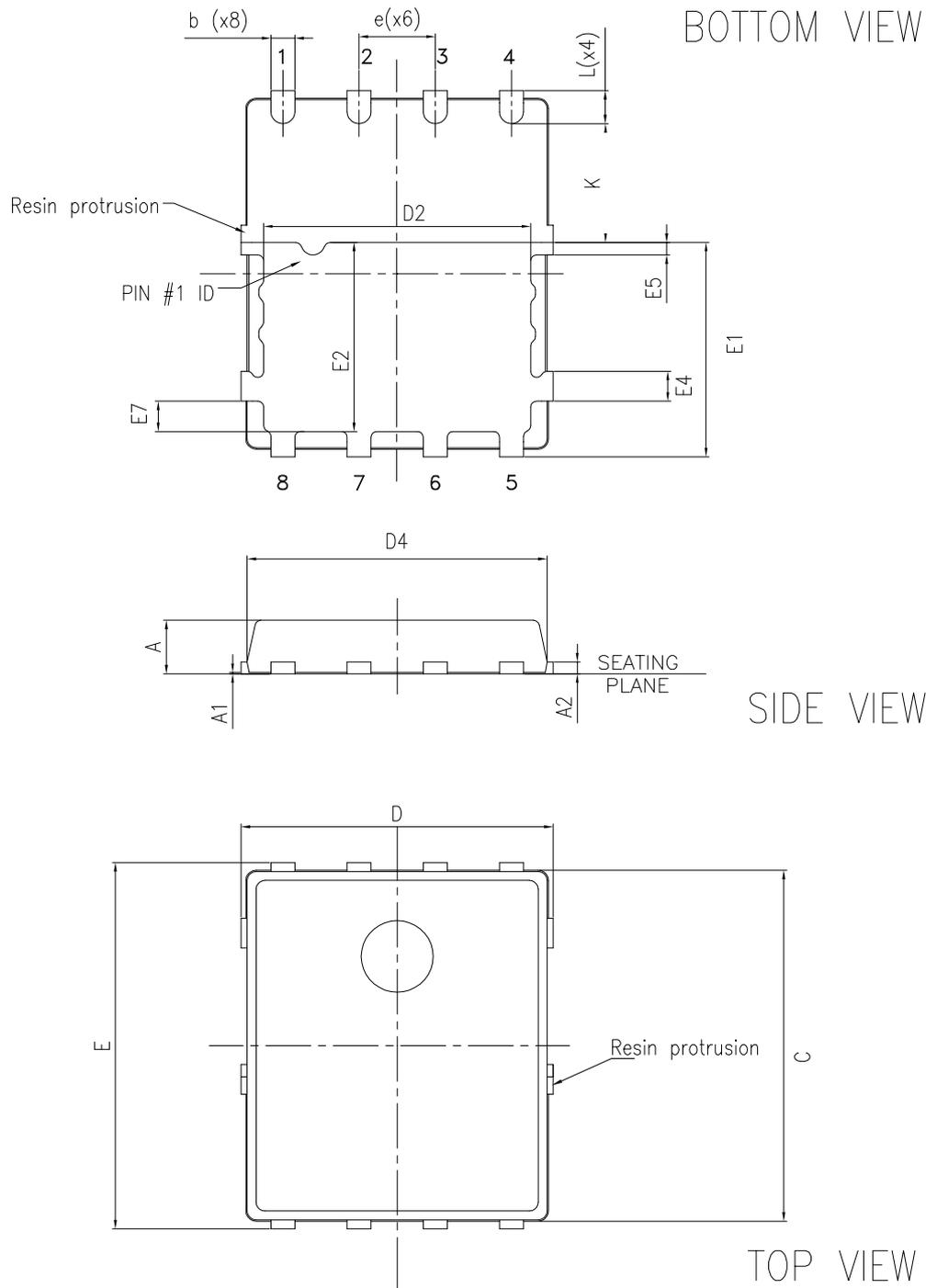
8368143_Rev_4

Table 7. PowerFLAT 5x6 HV mechanical data

| Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)
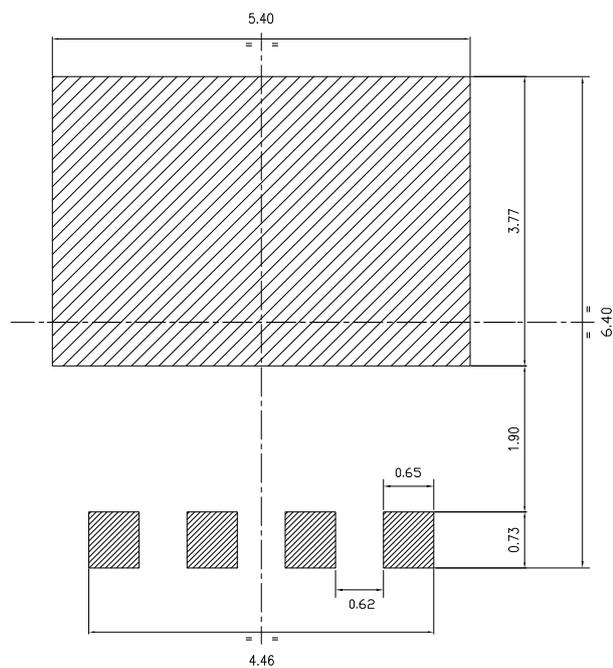
8368143_Rev_4_footprint

4.2　PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)
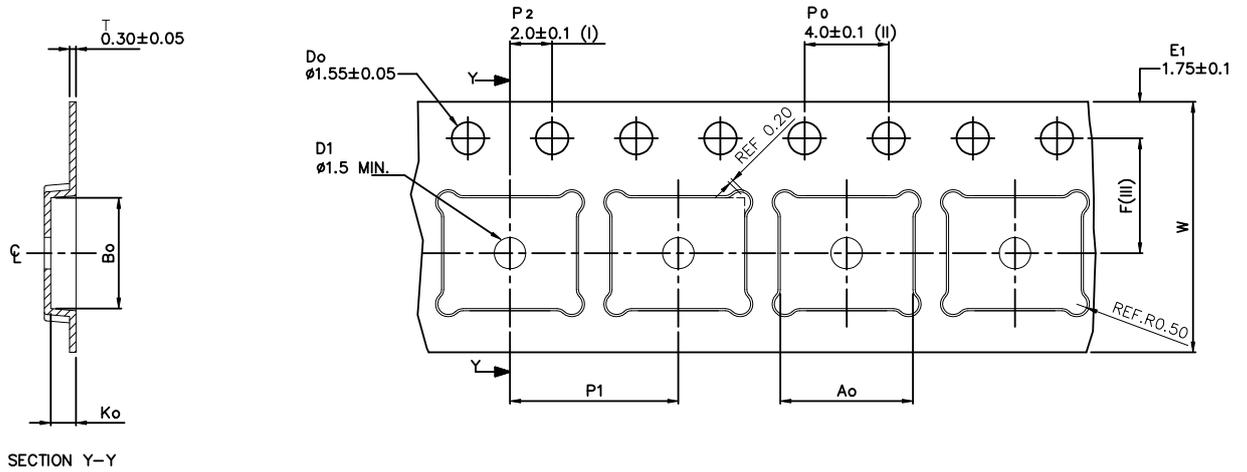
Ao	6.30 +/− 0.1
Bo	5.30 +/− 0.1
Ko	1.20 +/− 0.1
F	5.50 +/− 0.1
P₁	8.00 +/− 0.1
W	12.00 +/− 0.3

(I)　Measured from centreline of sprocket hole to centreline of pocket.

(II)　Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape
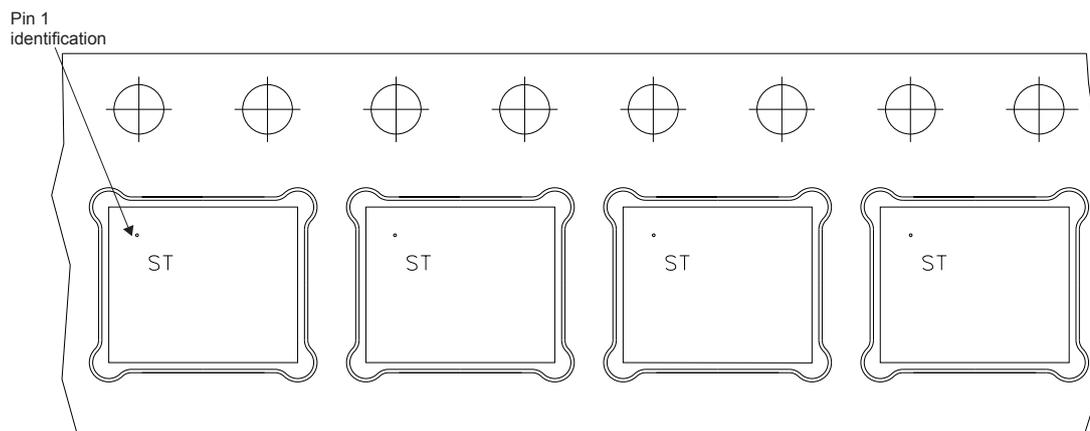
Figure 23. PowerFLAT 5x6 reel
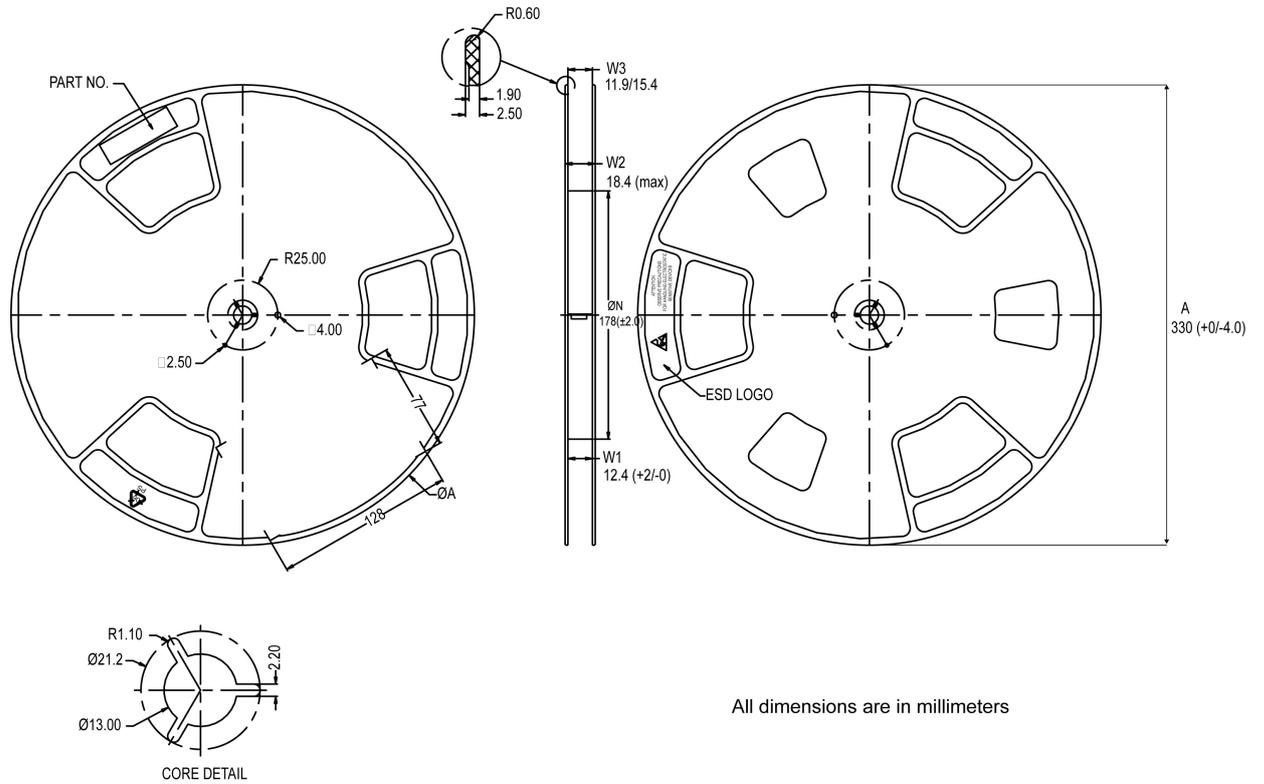
All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Mar-2017	1	First release
20-Jun-2019	2	Removed maturity status indication from cover page. The document status is production data. Updated Table 1. Absolute maximum ratings and Table 4. Dynamic. Minor text changes.

Contents

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