ATA6571

CAN FD Transceiver with High-Voltage WAKE Pin

Features

- CAN FD Transceiver Fully Compliant to ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAEJ 2962-2
- ISO 26262 Functional Safety Ready
- Wake-Up Pattern (WUP) Detection According to ISO 11898-2: 2016
- Communication Speed up to 5 Mbps
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- Functional Behavior Predictable Under All Supply Conditions
- VIO Input Allows for Direct Interfacing with 3V and 5V Microcontrollers
- Transceiver Disengages from the Bus when Not Powered-Up
- RXD Recessive Clamping Detection
- Silent Mode (Receive Only) for Node Diagnosis and Failure Containment
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-Out Function
- Undervoltage Detection on VS, VCC and VIO Pins
- CANH/CANL Short Circuit and Overtemperature Protected
- Power-Up Diagnosis
- INH Output to the Control External Voltage Regulator
- High-Voltage WAKE Input Pin
- Remote Wake-Up Capability through CAN Bus
- Wake-Up Source Recognition
- Fulfills the OEM Hardware Requirements for CAN in Automotive Applications, Rev. 1.3
- AEC Q100 and AEC Q006 Qualified
- Two Ambient Temperature Grades:
  - ATA6571-GNQW1 and ATA6571-GCQW1 up to T_{amb} = +125°C
  - ATA6571-GNQW0 and ATA6571-GCQW0 up to T_{amb} = +150°C
- Available Packages: SOIC14 and VDFN14 with Wettable Flanks (Moisture Sensitivity Level 1)

Description

The ATA6571 is a standalone high-speed CAN FD transceiver that interfaces a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 5 Mbit/s) CAN FD applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved Electromagnetic Compatibility (EMC) and ESD performance and very low power consumption, as well as features such as:

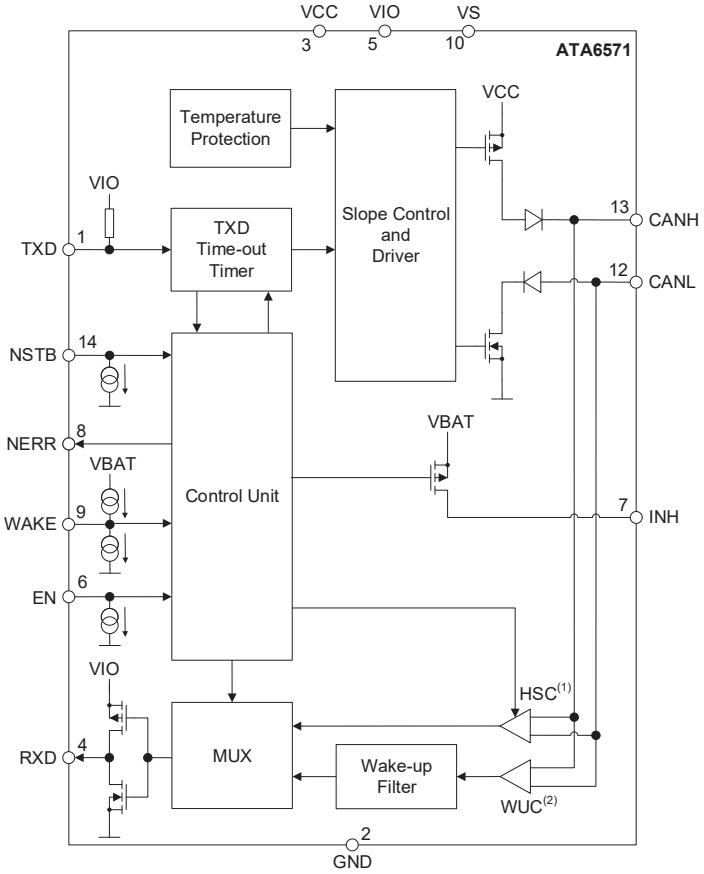
- Ideal passive behavior to the CAN bus when unpowered
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V
- Advanced low-power management with local and remote wake-up support, available at all times, even when the internal VIO and VCC supplies are switched off

- Protection and diagnostic functions including bus line short-circuit and battery connection detection

Table 1. ATA6571 Family Members

Device	Grade 0	Grade 1	SOIC14	VDFN14
ATA6571-GNQW1		x	x	
ATA6571-GNQW0	x		x	
ATA6571-GCQW1		x		x
ATA6571-GCQW0	x			x

Figure 1. Simplified Block Diagram



Notes:

1. High-Speed Comparator.
2. Wake-Up Comparator.

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1. Pin Configuration

Figure 1-1. Pin Configuration

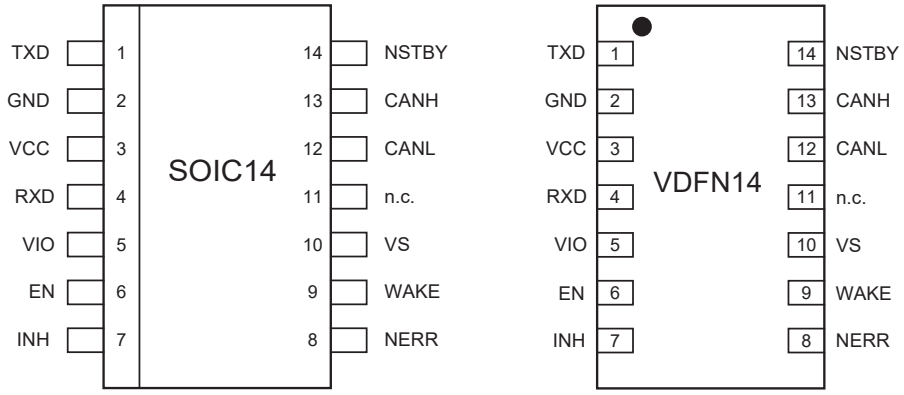


Table 1-1. Pin Description

ATA6571		Symbol	Function
SOIC14	VDFN14		
1		TXD	Transmit Data Input Pin
2		GND	Ground Pin
3		VCC	Transceiver Supply Voltage Pin
4		RXD	Receive Data Output Pin
5		VIO	Supply Voltage for the I/O Pins
6		EN	Enable Control Input Pin
7		INH	Inhibit Output for Switching External Voltage Regulators
8		NERR	Error and Power-on Indication Output (Active-Low)
9		WAKE	Local Wake-Up Input. Connect directly to the VS pin or the GND pin, if not used.
10		VS	Battery Supply Voltage Pin
11		NC	Not Connected
12		CANL	Low-Level CAN Bus Line
13		CANH	High-Level CAN Bus Line
14		NSTBY	Standby Mode Control Input (Active-Low)
—	15	EP	Heat Slug, Internally Connected to the GND Pin

1.1 Battery Supply Voltage Pin (VS)

This is the power supply pin. In an application, this pin is usually connected to the battery through a serial diode for reverse battery protection. This pin sustains standard automotive conditions, such as 40V during load dump. An undervoltage detection circuit is implemented to avoid a malfunction or false bus messages. After switching on the VS pin, the device starts in Standby mode and the INH output is switched on.

1.2 Ground Pin (GND)

The device does not affect the CAN bus in the event of a GND disconnection.

1.3 Transceiver Supply Voltage Pin (VCC)

This is the supply pin for the CANH and CANL bus drivers, the bus differential receiver and the bus biasing voltage circuitry. The device monitors the VCC pin for undervoltage conditions.

1.4 Supply Pin for I/O Level Adapter (VIO)

This is the supply pin for the digital input/output pins. This pin should be connected to the microcontroller's supply voltage to adjust the signal levels of pins TXD, RXD, NSTBY, EN and NERR to the I/O levels of the microcontroller. The device monitors the VIO pin for undervoltage conditions.

1.5 Bus Pins (CANH and CANL)

These are the CAN bus terminals.

The CANL pin is a low-side driver to GND, and the CANH pin is a high-side driver to VCC. In Normal mode and if TXD is high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is approximately 2.5V, provided by the internal bus biasing circuitry. This state is called recessive.

When TXD is low, CANL is pulled to GND and CANH to VCC, creating a differential voltage on the CAN bus. This state is called dominant.

In Standby mode, the CANH and CANL drivers are OFF. If the device is in unpowered mode or Sleep mode, CANH and CANL are highly resistive with extremely low leakage current to GND, making the device ideally passive.

The CANH and CANL pins have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. The CANH and CANL bus outputs are short-circuit protected against GND or a positive supply voltage and are also protected against overtemperature conditions.

1.6 Transmit Data Input Pin (TXD)

This is the device input pin used to control the CAN bus level. In the application, this pin is connected to the microcontroller transmit terminal. The TXD pin has an internal pull-up toward VIO to ensure a safe defined recessive driver state in case this pin is left floating.

In Normal mode, when TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus in the recessive state.

The TXD pin must be pulled to GND in order to activate the CANH and CANL drivers, and the bus is set to the dominant state. A TXD dominant time-out timer starts when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high.

The transmitter is also disabled, if the TXD pin is held low (for example, by a short circuit to GND) while the device is switched into Normal mode, the bus lines are in the recessive state. The transceiver remains in this state, until the TXD pin goes high.

1.7 Receive Data Output Pin (RXD)

In Normal and Silent mode, this pin reports the state of the CAN bus to the microcontroller. In the application, this pin is connected to the microcontroller receive terminal. RXD is high when the bus is recessive. When the bus is dominant, RXD is low.

The output is a push-pull structure; the high side is connected to VIO and the low side to GND.

In Standby mode, the RXD is switched to VIO. When a wake-up event is detected, the RXD will be forced to low.

A RXD recessive clamping function (see section 2.3.3 RXD Recessive Clamping) is implemented. This fail-safe feature prevents the controller from sending data on the bus if the RXD line is clamped to high (for example, recessive).

1.8 Inhibit Output Pin (INH)

The inhibit output pin provides an internal switch toward the VS pin and is used to control external voltage regulators. If the device is in Normal or Standby mode, the inhibit high-side switch is turned on. When the device is in Sleep mode, the inhibit switch is turned off, thus disabling the connected external voltage regulators or other connected external devices.

A wake-up event on the CAN bus or at the WAKE pin switches the INH pin to the VS level. After a system power-up (VS rises from zero), the INH pin switches to the VS level automatically.

1.9 Wake Pin (WAKE)

This pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If the WAKE pin is not needed in the application, it should be connected to VS or GND to ensure optimal EMI performance.

The WAKE pin has a special design structure and is triggered by a low-to-high or a high-to-low transition, allowing maximum flexibility when designing a local wake-up circuit.

An internal filter is implemented to avoid a false wake-up event due to parasitic pulses. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 10 kΩ. An external 10 nF capacitor is recommended for better EMC and ESD performances.

To reduce the battery current during Low-Power mode, the internal pull-up/pull-down circuit follows the logic level at the WAKE pin:

- a high level on the pin is followed by an internal pull-up toward VS
- a low level is followed by an internal pull-down towards GND.

1.10 Enable Pin (EN)

The enable input pin together with the NSTBY pin controls the operating mode of the device.

The internal pull-down on the EN pin forces the transceiver into Recessive mode if EN is disconnected.

1.11 Error Indication Pin (NERR)

The NERR pin signals the status of the device. The ATA6571 supports system diagnosis using seven internal flags. Five of these flags can be polled by the controller through NERR pin. The signaled flag on the pin NERR depends on the active operating mode and on a number of other conditions. Switching between modes gives access to the different diagnostic flags through the NERR pin.

1.12 Standby Mode Control Pin (NSTBY)

The NSTBY input pin together with the EN pin control the operating mode of the device. The NSTBY pin provides a pull-down current to force the transceiver into Standby mode, if STBY is disconnected.

2. Functional Description

The ATA6571 high-speed CAN transceiver offers a number of operating modes, diagnostic features and fail-safe features that enable enhanced system reliability and advanced power management.

2.1 Device Operation Modes

The control pins NSTBY and EN are used to select one of the five operating modes supported by the ATA6571. Switching between modes allows access to a number of diagnostic flags through the NERR pin. Table 2-1 describes how to switch between modes and Figure 2-1 illustrates the different mode transitions.

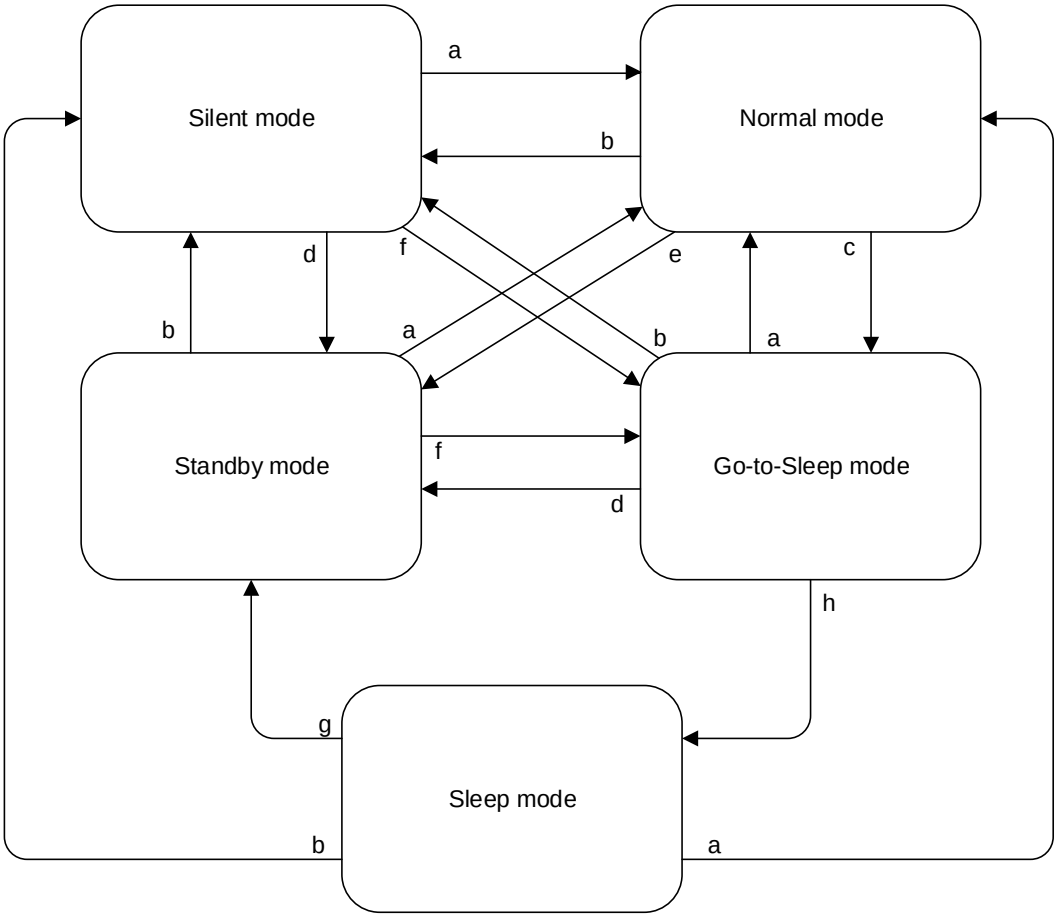
Table 2-1. Operating Modes

Mode	Diagnostic Flags			NSTBY(3)	EN	INH
	$UV_{VCC/VIO}$(1)	UV_{VS}	Wake(2)			
From Normal, Silent, Standby and Go-to-Sleep modes						
Sleep mode	Set	X	X	X	X	Floating
Standby mode	Cleared	Set	X	High	X	High
Standby mode	Cleared	X	Set	Low	X	High
Standby mode	Cleared	X	Cleared	Low	Low	High
Go-to-Sleep mode	Cleared	X	Cleared	Low	High	High
Silent mode	Cleared	Cleared	X	High	Low	High
Normal mode	Cleared	Cleared	X	High	High	High
From Sleep mode						
Sleep mode	Set	X	X	X	X	Floating
Standby mode	Cleared	Set	X	High	X	High
Standby mode	Cleared	X	Set	Low	X	High
Sleep mode	Cleared	X	Cleared	Low	X	Floating
Silent mode	Cleared	Cleared	X	High	Low	High
Normal mode	Cleared	Cleared	X	High	High	High

Notes:

1. Setting the $UV_{VCC/VIO}$ flag clears the Wake flag.
2. Setting the Wake flag clears the $UV_{VCC/VIO}$ flag.
3. A low-to-high transition on pin NSTBY clears the $UV_{VCC/VIO}$ flag.

Figure 2-1. Operating Modes



Where:

- a = NSTBY = 1, EN = 1
- b = NSTBY = 1, EN = 0
- c = NSTBY = 0, EN = 1
- d = NSTBY = 0, EN = 0 (wake flag set)
- e = NSTBY = 0, EN = 0
- f = NSTBY = 0, EN = 1 (wake flag cleared)
- g = NSTBY = 0 (wake flag set)
- h = wake flag cleared, $t > t_{hold(min)}$

2.1.1 Normal Mode

In Normal mode, the transceiver can transmit and receive data through the bus lines CANH and CANL. The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to the RXD pin. The bus biasing is set to $V_{VCC/2}$ and the undervoltage monitoring of VCC is active. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME). The INH pin is active, so voltage regulators controlled by the INH pin are active too.

2.1.2 Silent Mode

This Receive-Only mode can be used to test the connection of the bus medium. In Silent mode, the ATA6571 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state ($V_{VCC/2}$). All other IC functions, including the HSC, continue to operate as they do in Normal mode. The Silent mode can be used to prevent a faulty CAN controller from disrupting network communication.

2.1.3 Standby Mode

The Standby mode is the first level of power-saving mode for the ATA6571, offering reduced current consumption. In this mode, the transceiver is not able to transmit or correctly receive data through the bus lines. The transmitter and the HSC are switched off to reduce current consumption and only the low-power Wake-Up Comparator (WUC) monitors the bus lines for a valid wake-up signal. The bus pins are biased at ground level.

Pin INH is still active, so voltage regulators controlled by this pin are also active.

Pins RXD and NERR reflect any active wake-up requests (provided that VIO and VS are present).

2.1.4 Go-to-Sleep Mode

The Go-to-Sleep mode is the controlled route for entering Sleep mode. In Go-to-Sleep mode, the transceiver behaves as in Standby mode, with the addition that a Go-to-Sleep command is issued to the transceiver. The transceiver remains in Go-to-Sleep mode for the minimum hold time (t_{hold}) before entering Sleep mode. The transceiver does not enter Sleep mode if the state of pin NSTBY or pin EN is changed or if the Wake flag is set before t_{hold} has elapsed.

2.1.5 Sleep Mode

The Sleep mode is the highest power-saving mode of the device. In this mode, the INH output is switched off. Therefore the external voltage regulator(s) controlled by this pin is also switched off. This is the only difference between Sleep mode and Standby mode.

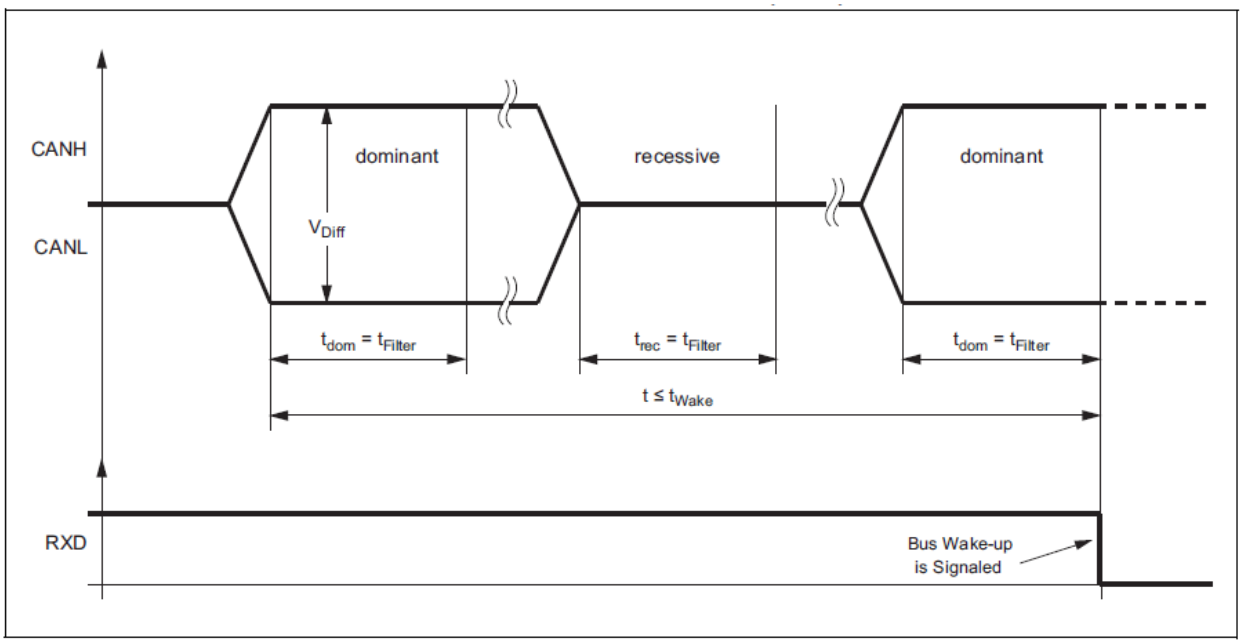
The Sleep mode is entered through Go-to-Sleep mode, and also when the undervoltage detection time on either VCC or VIO elapses before the relevant voltage level has recovered. Pins NSTBY, EN, and the Wake flag can be used to wake up a node from Sleep mode.

2.1.6 Remote Wake-Up through the CAN Bus

In Standby and Sleep mode, the bus lines are biased to ground to reduce current consumption to a minimum. The ATA6571 monitors the bus lines for a valid WUP as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events, which can be triggered by scenarios such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI.

The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern must be received within the bus wake-up time-out time t_{wake}, to be recognized as a valid wake-up pattern, as shown in Figure 2-2. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. Pin RXD remains at high level until a valid wake-up event is detected. During Normal mode, at a VCC or VIO undervoltage condition or when the complete wake-up pattern is not received within t_{wake}, no wake-up is signalled at the RXD pin.

Figure 2-2. Timing of the Bus WUP in Standby Mode



When a valid CAN WUP is detected on the bus, the RXD pin switches to low to signal a wake-up request.

2.2 Internal Flags

For Fail-Safe Fallback mode control and system diagnosis, the ATA6571 has seven internal flags. Five of these flags can be polled by the controller through pin NERR. Depending on the current operating mode and on a number of other conditions, a different flag is available on the NERR pin. Table 2-2 describes how to access and control these flags.

Table 2-2. Internal Flags Accessed through Pin NERR

Internal flag	Available flag on pin NERR (1)	Flag is cleared
$UV_{VCC/VIO}$	No	By setting the Pwon or Wake flags, by a low-to-high transition on NSTBY or when both VIO and VCC have recovered.
UV_{VS}	No	When VS has recovered.
Pwon	In Silent mode (coming from Standby mode, Go-to-Sleep mode, or Sleep mode).	When entering Normal mode.
Wake	In Standby mode, Go-to-Sleep, and Sleep mode (provided that VIO and VS are present).	When entering Normal mode or by setting the $UV_{VCC/VIO}$ flag.
Wake-up source	In Normal mode (before the fourth dominant-to-recessive edge on pin TXD (2).	When leaving Normal mode.
Bus failure	In Normal mode (after the fourth dominant-to-recessive edge on pin TXD (2).	When re-entering Normal mode or by setting the Pwon flag.

Notes:
1. Pin NERR is an active-low output, so a low level indicates a set flag and a high level indicates a cleared flag. Allow pin NERR to stabilize for at least 8 µs after changing operating modes.
2. Allow a TXD dominant time of at least 4 µs per dominant-recessive cycle.

.....continued		
Internal flag	**Available flag on pin NERR (1)**	**Flag is cleared**
Local failure	In Silent mode (coming from Normal mode).	When entering Normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved) or by setting the Pwon flag.

Notes:
1. Pin NERR is an active-low output, so a low level indicates a set flag and a high level indicates a cleared flag. Allow pin NERR to stabilize for at least 8 µs after changing operating modes.
2. Allow a TXD dominant time of at least 4 µs per dominant-recessive cycle.

2.2.1 $UV_{VCC/VIO}$ Flag

$UV_{VCC/VIO}$ is the VCC and/or VIO undervoltage detection flag. The flag is set when the voltage on pin VCC drops below the VCC undervoltage detection voltage, V_{VCC_UV}, for longer than the undervoltage detection time, $t_{VSUP\_UV\_set}$, or when the voltage on pin VIO drops below V_{VIO_UV} for longer than $t_{VSUP\_UV\_set}$. When the $UV_{VCC/VIO}$ flag is set, the transceiver enters Sleep mode to save power and to ensure the bus is not disturbed. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding any extra power consumption that might be caused by a short-circuit condition.

Any wake-up request, setting the Pwon flag or a low-to-high transition on NSTBY will clear $UV_{VCC/VIO}$ and the timers, allowing the voltage regulators to be reactivated (at least until $UV_{VCC/VIO}$ is set again). $UV_{VCC/VIO}$ is also cleared if both VCC and VIO recover for longer than the undervoltage recovery time, $t_{VSUP\_UV\_clear}$. The transceiver will then switch to the operating mode indicated by the logic levels on pins NSTBY and EN (see section 2.1 Device Operation Modes).

2.2.2 UV_{VS} Flag

The UV_{VS} is the VS undervoltage detection flag. This flag is set when the voltage on pin VS drops below $V_{VS\_UV\_CAN\_Set}$. When UV_{VS} is set, the transceiver enters Standby mode to save power and disengages from the bus (zero load). UV_{VS} is cleared when the voltage on pin VS recovers. The transceiver then switches to the operating mode indicated by the logic levels on pins NSTBY and EN (see section 2.1 Device Operation Modes).

2.2.3 Pwon Flag

The Pwon is the VS power-on flag. This flag is set when the voltage on pin VS recovers after previously dropping below V_{VS_PWROFF} (usually because the battery was disconnected). Setting the Pwon flag clears the $UV_{VCC/VIO}$ flag and timers. The Wake and Wake-Up Source flags are set to ensure consistent system power-up under all supply conditions. In Silent mode, the Pwon flag can be polled through pin NERR (see Table 2-2). The flag is cleared when the transceiver enters Normal mode.

2.2.4 Wake Flag

The Wake flag is set when the transceiver detects a local or remote wake-up request. A local wake-up request is detected when the logic level on pin WAKE changes and the new level remains stable for at least t_{wake}. A remote wake-up request is triggered by two bus dominant states of at least $t_{wake(busdom)}$, with the first dominant state followed by a recessive state of at least $t_{wake(busrec)}$ (provided the dominant-recessive-dominant pattern is completed within $t_{to(wake)bus}$). The Wake flag can be set in Standby mode, Go-to-Sleep mode or Sleep mode. Setting the Wake flag clears the $UV_{VCC/VIO}$ flag and timers. Once set, the Wake flag status is immediately available on pins NERR and RXD (if VIO and VS are present). This flag is also set at power-on and cleared when the $UV_{VCC/VIO}$ flag is set or the transceiver enters Normal mode.

2.2.5 Wake-Up Source Flag

The wake-up source recognition is provided through the Wake-Up Source flag, which is set when the Wake flag is set by a local wake-up request through the WAKE pin. The Wake-Up Source flag can be polled through the NERR pin in Normal mode (see Table 2-2). This flag is also set at power-on and cleared when the transceiver leaves the Normal mode.

2.2.6 Bus Failure Flag

The Bus Failure flag is set if the transceiver detects a bus line short-circuit condition to VS, VCC or GND during four consecutive dominant-recessive cycles on pin TXD, while trying to drive the dominant bus lines. The Bus Failure flag can be polled through the NERR pin in Normal mode (see Table 2-2). This flag is cleared at power-on or when the transceiver re-enters Normal mode.

2.2.7 Local Failure Flag

In Normal and Silent modes, the transceiver can detect five different local failure events, any of which will cause the Local Failure flag to be set. The five local failure events are: TXD dominant clamping, TXD-to-RXD short circuit, bus dominant clamping, an overtemperature event, and an RXD recessive clamping event (see section 2.3 Fail-Safe Features). The Local Failure flag can be polled through the NERR pin in Silent mode (see Table 2-2). This flag is cleared at power-on, when entering Normal mode or when RXD is dominant while TXD is recessive, provided that all local failures have been resolved.

2.3 Fail-Safe Features

The ATA6571 can detect a number of different local failure conditions. Any of these failures sets the Local Failure flag and in most cases the transmitter of the transceiver is disabled.

2.3.1 TXD Dominant Time-Out Function

A permanent low level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communication. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter. The TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to a recessive state. The $t_{to(dom)}$ dominant time-out timer defines a minimum possible bit rate of 40 kbit/s. The transmitter remains disabled until the Local Failure flag is cleared.

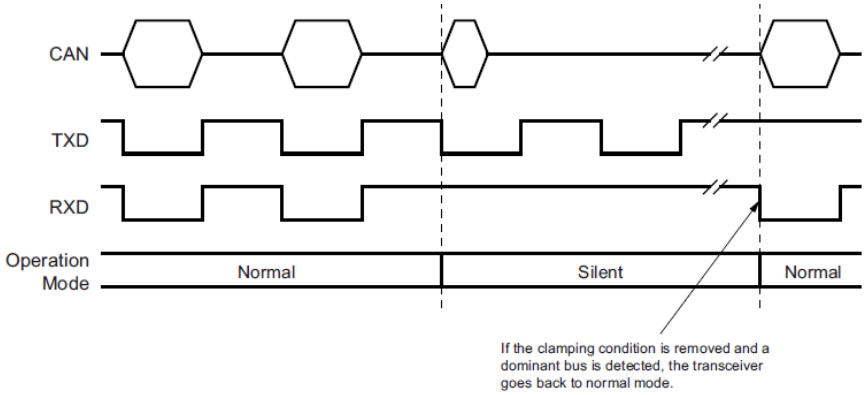
2.3.2 TXD-to-RXD Short-Circuit Detection

A short circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it has been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. The TXD-to-RXD short-circuit detection prevents this network lock-up by disabling the transmitter. The transmitter remains disabled until the Local Failure flag is cleared.

2.3.3 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data to the bus if its RXD line is clamped to high (for example, recessive). That is, if the RXD pin cannot signal a dominant bus state because it is shorted to VCC, the transmitter within the ATA6571 is disabled to avoid possible data collisions on the bus. In Normal and Silent mode, the device permanently compares the state of the the HSC with the state of the RXD pin. If the HSC indicates a dominant bus state for more than $t_{RXD\_rec\_clmp}$, without the RXD pin indicating the same, a recessive clamping situation is detected. The RXD recessive clamping detection is reset (LOCFAIL flag removed) by either entering Normal or unpowered mode or if the RXD pin is showing a dominant (for example, LOW) level again.

Figure 2-3. RXD Recessive Clamping Detection



2.3.4 Bus Dominant Clamping Detection

A CAN bus short circuit (to VS, VCC or GND) or a failure in one of the other network nodes can result in a differential voltage on the bus, high enough to represent a bus dominant state. Because a node does not start transmission if the bus is dominant, the normal bus failure detection does not detect this failure, but the bus dominant clamping detection will. The Local Failure flag is set if the dominant state on the bus persists for longer than t_{BUS_dom}. By checking this flag, the controller can determine if a clamped bus is blocking network communication. There is no need to disable the transmitter. RXD is low as long as the bus is still dominant and goes high when the bus is released to high.

Note: The Local Failure flag does not retain a bus dominant clamping failure and is released as soon as the bus returns to the recessive state.

2.3.5 Overtemperature Detection

The transceiver is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the transmitter is disabled until the Local Failure flag is cleared.

2.3.6 Bus Wake-Up only at Dedicated Wake-Up Pattern

Due to the implementation of the wake-up filtering, the ATA6571 does not wake up when the bus is in a long dominant phase, it only wakes up due to the wake-up pattern specified in the ISO 11898-2: 2016. This means that for a valid wake-up at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter} must be received from the bus. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern (as shown in Figure 2-2) must be received within the bus wake-up time-out time t_{wake} to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients and reduces therefore the risk of an unwanted bus wake-up significantly.

2.3.7 Undervoltage Detection on Pins VS, VCC and VIO

If V_{VS}, V_{VCC} or V_{VIO} drop below their respective undervoltage detection levels ($V_{VS\_UV\_CAN\_Set}$, V_{VCC_UV} and V_{VIO_UV} (see section 5. Electrical Characteristics), the transceiver switches off and disengages from the bus until V_{VS}, V_{VCC} and V_{VIO} recover. The low-power wake-up comparator and local wake-up are switched off during a VS undervoltage.

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Sym.	Min.	Max.	Unit
CANH, CANL DC Voltage	V_{CANH}, V_{CANL}	–27	+42	V
Transient Voltage, according to ISO 7637 part 2		–150	+100	V
Maximum Differential Bus Voltage	V_{Diff}	–25	+25	V
DC Voltage on Pins TXD, RXD, NSTBY, EN, NERR, VCC, VIO	V_x	–0.3	+5.5	V
DC Voltage on Pins VS, WAKE, INH	V_{VS}, V_{WAKE}, V_{INH}	–0.3	+40	V
ESD according to IBEE CAN EMC Test Specification following IEC 62228, IEC 61000-4-2: Pins VS, CANH, CANL, WAKE to GND	—	+/–8	—	kV
HBM JESD22-A114/AEC-Q100-002: • CANH, CANL • VS, WAKE to GND	— —	+/–8 +/–6	— —	kV kV
HBM JESD22-A114/AEC-Q100-002: All Pins	—	+/–4	—	kV
Charge Device Model ESD AEC-Q100-011	—	+/–750	—	V
Machine Model ESD AEC-Q100-003	—	+/–100	—	V
Storage Temperature	T_{stg}	–55	+150	°C
Virtual Junction Temperature	T_{vJ}	–40	+175	°C

4. Thermal Characteristics

Table 4-1. Thermal Characteristics SOIC14

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Ambient, where IC is soldered to PCB according to JEDEC	R_{thvJA}	—	110	—	K/W
Thermal Shutdown of the Bus Drivers for the ATA6571-GNQW1 (Grade 1)	T_{Jsd}	150	—	200	°C
Thermal Shutdown of the Bus Drivers for the ATA6571-GNQW0 (Grade 0)	T_{Jsd}	170	—	200	°C
Thermal Shutdown Hysteresis	T_{Jsd_hys}	—	15	—	°C

Table 4-2. Thermal Characteristics VDFN14

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	45	—	K/W
Thermal Shutdown of the Bus Drivers for the ATA6571-GCQW1 (Grade 1)	T_{Jsd}	150	—	200	°C
Thermal Shutdown of the Bus Drivers for the ATA6571-GCQW0 (Grade 0)	T_{Jsd}	170	—	200	°C
Thermal Shutdown Hysteresis	T_{Jsd_hys}	—	30	—	°C

5. Electrical Characteristics

All parameters valid for Grade 1: T_{amb} = –40°C to +125°C, Grade 0: T_{amb} = –40°C to +150°C; $T_{vJ} \leq 170°C$; $4.5V \leq V_{VS} \leq 28V$; $4.5V \leq V_{VCC} \leq 5.5V$; $2.8V \leq V_{VIO} \leq 5.5V$; all voltages are defined with respect to ground; $R_{(CANH-CANL)}$ = 60Ω; C_L = 100 pF; typical values are given at V_{VS} = 13V, T_{amb} = +25°C; unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
VS									
0.10	Supply Voltage Threshold for Power-On Detection	V_{VS} rising	VS	V_{VS_PWRON}	—	—	4.8	V	B
0.20	Supply Voltage Threshold for Power-Off Detection	V_{VS} falling	VS	V_{VS_PWROFF}	2.8	—	3.1	V	A
0.30	Supply Voltage Threshold for CAN TRX Undervoltage Detection Release	V_{VS} rising	VS	$V_{VS\_UV\_CAN\_Clear}$	4.3	—	4.6	V	A
0.40	Supply Voltage Threshold for CAN TRX Undervoltage Detection	V_{VS} falling	VS	$V_{VS\_UV\_CAN\_Set}$	4.2	—	4.5	V	A
0.50	VS Supply Current	Standby mode; $V_{INH} = V_{WAKE} = V_{VS}$, $V_{VS} < 18V$	VS	I_{VS_Stby}	—	—	32	µA	A
0.51		Normal or Silent mode; $V_{VS} < 18V$	VS	I_{VS_Norm}	—	—	350	µA	A
0.52		Sleep mode; $V_{INH} = V_{VCC} = V_{VIO} = 0V$; $V_{WAKE} = V_{VS}$; $V_{VS} < 18V$	VS	I_{VS_Sleep}	—	18	30	µA	A
VCC									
1.10	VCC Undervoltage Detection Threshold		VCC	V_{VCC_UV}	4	—	4.5	V	A
1.20	VCC Supply Current	Normal mode (dominant)	VCC	I_{VCC_dom}	20	—	65	mA	A
1.31		Normal mode (recessive)	VCC	I_{VCC_rec}	2	—	6.2	mA	A
1.310		Silent mode	VCC	I_{VCC_sil}	0.2	—	1.8	mA	A
1.32		Normal mode short between CANH and CANL	VCC	I_{VCC_short}	—	—	80	mA	B
1.33		Sleep mode or Standby mode	VCC	I_{VCC_sleep}	—	—	4	µA	A
VIO									
2.10	VIO Undervoltage Detection Threshold		VIO	V_{VIO_UV}	2.4	—	2.8	V	A
2.20	VIO Supply Current	Normal (V_{TXD} = 0V)	VIO	I_{VIO_norm}	—	—	130	µA	A
2.21		Normal mode or Silent mode (recessive)	VIO	I_{VIO_rec}	—	—	4.5	µA	A
2.22		Standby mode or Sleep mode	VIO	I_{VIO_Sleep}	—	—	4.5	µA	A
NSTBY and EN									
3.10	High-Level Input Voltage		NSTBY/EN	V_{NSTBY/EN_H}	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V	A
3.20	Low-Level Input Voltage		NSTBY/EN	V_{NSTBY/EN_L}	−0.3	—	0.3 × V_{VIO}	V	A
3.30	High-Level Input Current	V_{NSTBY}, V_{EN} > 0.7*VIO	NSTBY/EN	I_{NSTBY/EN_H}	1	4	10	µA	A
3.40	Low-Level Input Current	V_{NSTBY}, V_{EN} = 0V	NSTBY/EN	I_{NSTBY/EN_L}	−1	0	+1	µA	B
NERR, RXD									
4.10	High-Level Output Current	$V_{NERR/RXD}$ = V_{VIO} - 0.4V	NERR, RXD	$I_{NERR\_H, IRXD\_H}$	−3	—	—	mA	A
4.20	Low-Level Output Current	V_{NERR} = 0.4V	NERR, RXD	$I_{NERR\_L, IRXD\_L}$	—	—	3	mA	A
TXD									
5.10	High-Level Input Voltage		TXD	V_{TXD_H}	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V	A
5.20	Low-Level Input Voltage		TXD	V_{TXD_L}	−0.3	—	0.3 × V_{VIO}	V	A

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No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
5.30	Pull-Up Resistor		TXD	R_{PU_TXD}	40	60	80	kΩ	A
5.40	Input Capacitance		TXD	C_{TXD}	—	5	10	pF	D
WAKE									
6.10	High-Level Input Current	$V_{WAKE} = V_{VS}$ - 1.9V	WAKE	I_{WAKE_H}	−10	−5	−1	µA	A
6.20	Low-Level Input Current	$V_{WAKE} = V_{VS}$ - 3.9V	WAKE	I_{WAKE_L}	1	5	10	µA	A
6.30	Threshold Voltage		WAKE	V_{WAKE_TH}	V_{VS} - 3.8	—	V_{VS} - 2	V	A
INH									
7.10	High-Level Voltage	Normal mode or Standby mode, I_{INH} = −180 µA	INH	V_{INH_H}	V_{VS} - 0.8	—	V_{VS}	V	A
7.20	Off Mode Leakage Current	Off mode leakage current, INH pin grounded	INH	I_{INH_Off}	−2	—	2	µA	A
CANH, CANL (see Figure 6-3 for the definition of R_L and the test circuit)									
8.10	Single-Ended Dominant Output Voltage	R_L = 50Ω to 65Ω	CANH	V_{CANH}	2.75	3.5	4.5	V	A
8.11			CANL	V_{CANL}	0.5	1.5	2.25	V	A
8.30	Transmitter Voltage Symmetry	$V_{Sym} = (V_{CANH} + V_{CANL})/VCC$, R_L = 60Ω, C_1 = 4.7 nF, f_{TXD} = 1 MHz	—	V_{SYM}	0.9	—	1.1	V	D
8.40	Dominant Differential Output Voltage	Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, t < $t_{to(dom)}$ R_L = 50Ω to 65Ω	—	V_{Diff}	1.5	—	3	V	B
8.41		Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, t < $t_{to(dom)}$ R_L = 45Ω to 70Ω	—	V_{Diff}	1.4	—	3.2	V	B
8.42		Normal mode, V_{TXD} = 0V, V_{VCC} = 4.7V to 5.5V, t < $t_{to(dom)}$ R_L = 2240Ω	—	V_{Diff}	1.5	—	5	V	D
8.50	Recessive Output Voltage	Single-Ended output voltage on CANH/CANL, Normal mode/Silent mode, $V_{TXD} = V_{VIO}$, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	0.5 x V_{VCC}	3	V	A
8.51		Single-Ended output voltage on CANH/CANL, Standby mode, $V_{TXD} = V_{VIO}$, no load	CANH, CANL	V_{CANH}, V_{CANL}	−0.1	—	0.1	V	A
8.53		Differential output voltage (bus biasing active), no load	CANH, CANL	V_{Diff}	−50	—	50	mV	A
8.54		Differential output voltage (bus biasing inactive), no load	CANH, CANL	V_{Diff}	−200	—	200	mV	A
8.60	Differential Receiver Threshold Voltage	Normal/Silent mode; $V_{CANL} = V_{CANH}$ = −12V to +12V	—	$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	A
8.61		Standby/Sleep mode; $V_{CANL} = V_{CANH}$ = −12V to +12V	—	$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	A
8.70	Differential Receiver Hysteresis Voltage	Normal/Silent mode; $V_{CANL} = V_{CANH}$ = −12V to +12V	—	V_{hys_rx}	50	120	200	mV	B
8.80	Input Leakage Current	$V_{VS} = V_{VCC} = V_{VIO}$ = 0V, $V_{CANH} = V_{CANL}$ = 5V	—	I_{leak_in} (I_{CANH}, I_{CANL})	−5	—	+5	µA	A
		$V_{VS} = V_{VCC} = V_{VIO}$ shorted to ground through 47 kΩ, $V_{CANH} = V_{CANL}$ = 5V	—	I_{leak_in} (I_{CANH}, I_{CANL})	−5	—	+5	µA	D

.....continued

No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
8.90	Maximum Driver Output Current	Normal mode, CAN dominant, V_{TXD} = 0, t < $t_{to(dom)}$, V_{VCC} = 5V, V_{CANH} = −5V (short circuit)	—	I_{CANH_max}	−100	—	−35	mA	A
8.91		Normal mode, CAN dominant; V_{TXD} = 0, t < t_{dom}, V_{VCC} = 5V, V_{CANL} = 18V (short circuit)	—	I_{CANL_max}	35	—	100	mA	A
8.92		Normal mode, CAN dominant; V_{TXD} = 0, t < t_{dom}, V_{VCC} = 5V, V_{CANL} = 27V (short circuit)	—	I_{CANL_max}	35	—	115	mA	D
8.100	Single-Ended Input Resistance	V_{CANH} = V_{CANL} = 4V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	A
		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	D
8.110	Matching of Internal Resistance Between CANH and CANL	V_{CANH} = V_{CANL} = 4V, mR = 2 × (R_{CANH} - CANL)/ (R_{CANH} + R_{CANL})	—	mR	−1	—	1	%	A
		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V mR = 2 × (R_{CANH} - R_{CANL})/ (R_{CANH} + R_{CANL})	—	mR	−1	—	1	%	D
8.120	Differential Internal Resistance	V_{CANH} = V_{CANL} = 4V	—	R_{Diff}	18	30	56	kΩ	A
		−2V ≤ V_{CANH} ≤ 7V, −2V ≤ V_{CANL} ≤ 7V	—	R_{Diff}	18	30	56	kΩ	D
8.130	Common-Mode Input Capacitance	f=500kHz, CANH and CANL referring to ground	—	$C_{i(cm)}$	—	—	20	pF	D
8.140	Differential Input Capacitance	f=500kHz, between CANH and CANL	—	C_{Diff}	—	—	10	pF	D
8.141	Differential Bus Voltage Range for Recessive State Detection	Bus biasing active /inactive -12,0V ≤ V_{CANL} ≤ +12,0V -12,0V ≤ V_{CANH} ≤ +12,0V	—	$V_{Diff\_rec\_a}$ $V_{Diff\_rec\_i}$	−3 −3	— —	+0.5 +0.4	V	D
8.142	Differential Bus Voltage Range for Dominant State Detection	Bus biasing active /inactive -12,0 V ≤ V_{CANL} ≤ +12,0 V -12,0 V ≤ V_{CANH} ≤ +12,0 V	—	$V_{DIFF\_dom\_a}$ $V_{DIFF\_dom\_i}$	0.9 1.15	— —	8 8	V	D
Transceiver Timing, Pins WAKE, INH, CANH, CANL, TXD and RXD. See Figure 5-1, Figure 5-2 and Figure 6-3 for the definition of the timing parameters and the test circuit.									
9.10	Delay Time from TXD to Bus Dominant	R_L = 60Ω, C_2 = 100 pF	CANH, CANL, TXD	t_{TXDBUS_dom}	—	65	—	ns	C
9.20	Delay Time from TXD to Bus Recessive	R_L = 60Ω, C_2 = 100 pF	CANH, CANL, TXD	t_{TXDBUS_rec}	—	90	—	ns	C
9.30	Delay Time from bus Dominant to RXD	R_L = 60Ω, C_2 = 100 pF	CANH, CANL, RXD	t_{BUSRXD_dom}	—	60	—	ns	C
9.40	Delay Time from Bus Recessive to RXD	R_L = 60Ω, C_2 = 100 pF	CANH, CANL, RXD	t_{BUSRXD_rec}	—	65	—	ns	C
9.50	Propagation Delay from TXD to RXD	R_L = 60Ω, C_2 = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	100	—	255	ns	A
9.51		R_L = 150Ω, C_2 = 100 pF, C_{RXD} = 15 pF, f_{TXD} = 250 KHz	TXD, RXD	t_{Loop}	—	—	300	ns	C
9.60	Recessive Bit Time on Pin RXD	t_{B_TXD} = 500 ns, R_L = 60Ω, C_2 = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	400	—	550	ns	C
9.61		t_{B_TXD} = 200 ns, R_L = 60Ω, C_2 = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	120	—	220	ns	A

.....continued

No.	Parameters	Test Conditions	Pin	Sym.	Min.	Typ.	Max.	Unit	Type*
9.70	Receiver Timing Symmetry	$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$, t_{B_TXD} = 500 ns (see no. 9.100 for $t_{Bit(Bus)}$) RL = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	—	Δt_{Rec}	−65	—	+40	ns	C
9.71		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$, t_{B_TXD} = 200 ns RL = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	—	Δt_{Rec}	−45	—	+15	ns	B
9.80	TXD Dominant Time-Out Time	V_{TXD} = 0V, Normal mode	TXD	$t_{to(dom)}$	2.7	—	3.3	ms	B
9.90	Bus Dominant Time-Out Time	$V_{CANH-CANL}$ 0.9V	—	t_{BUS_dom}	2.7	—	3.3	ms	B
9.100	Transmitted Recessive Bit Width on the Bus	t_{B_TXD} = 500 ns RL = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	—	$t_{Bit(Bus)}$	435	—	530	ns	C
9.110		t_{B_TXD} = 200 ns RL = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	—	$t_{Bit(Bus)}$	155	—	210	ns	A
9.120	CAN Activity Filter Time for Standard Remote Wake-Up Pattern (WUP)	First pulse (after first recessive) and second pulse for wake-up on pins CANH and CANL, Sleep mode	CANH, CANL	t_{Filter}	0.5	—	1.8	µs	A
9.170	Go-to-Sleep Hold Time	From issuing the Go-to-Sleep command to enter Sleep mode	—	t_{hold}	20	—	50	µs	B
9.180	Undervoltage Detection Time		VCC, VIO	$t_{VSUP\_UV\_set}$	100	—	350	ms	B
9.190	Undervoltage Recovery Time		VCC, VIO	$t_{VSUP\_UV\_clear}$	1	—	5	ms	B
9.200	Start-Up Time after Power-On	From V_{VS} rises above the power-on detection threshold, V_{VS_PWRON} until pin INH high	VS	$t_{startup}$	—	0.5	1	ms	A
9.220	Debouncing Time for Recessive Clamping State Detection	$V_{CANH + CANL}$ > 900 mV, RXD = HIGH	RXD	$t_{RXD\_rec\_clmp}$	60	90	175	ns	D
9.230	Local Wake-Up Filter Time	In response to a falling or rising edge on pin WAKE; Standby or Sleep mode	WAKE	t_{local_wu}	5	—	50	µs	A
9.240	Transmitter Resume Time	From TXD, it goes high to TX and it operates after the TXD dominant timeout event is detected	—	$t_{TX\_resume\_TXDOUT}$	—	—	4	µs	D
9.250	Bus Wake-Up Time-Out Time	Between the first and second dominant pulses, CAN TRX Standby mode	—	t_{wake}	0.9	—	1.2	ms	B
9.260	Delay Time for Standby to Normal Mode Transition	Rising edge at pin NSTBY, EN = HIGH	—	$t_{del(stby-norm)}$	—	—	47	µs	D
9.270	Delay Time for Normal Mode to Standby Mode Transition	Falling edge at pin NSTBY, EN = LOW	—	$t_{del(norm-stby)}$	—	—	5	µs	D
9.280	Delay Time for Normal Mode to Silent Mode Transition	Falling edge at pin EN, NSTBY = HIGH	—	$t_{del(norm-silent)}$	—	—	10	µs	D
9.290	Delay Time for Silent Mode to Normal Mode Transition	Rising edge at pin EN, NSTBY = HIGH	—	$t_{del(silent-norm)}$	—	—	10	µs	D
9.300	Delay Time for Silent Mode to Standby Mode Transition	Falling edge at pin EN, NSTBY = LOW	—	$t_{del(silent-stby)}$	—	—	5	µs	D
9.310	Delay Time for Standby Mode to Silent Mode Transition	Rising edge at pin NSTBY, EN = LOW	—	$t_{del(stby-silent)}$	—	—	47	µs	D
9.320	Delay Time for Sleep Mode to Standby Mode Transition	Wake event detected	—	$t_{del(sleep-stby)}$	—	—	5	µs	D

* Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter.

Figure 5-1. CAN Transceiver Timing Diagram 1

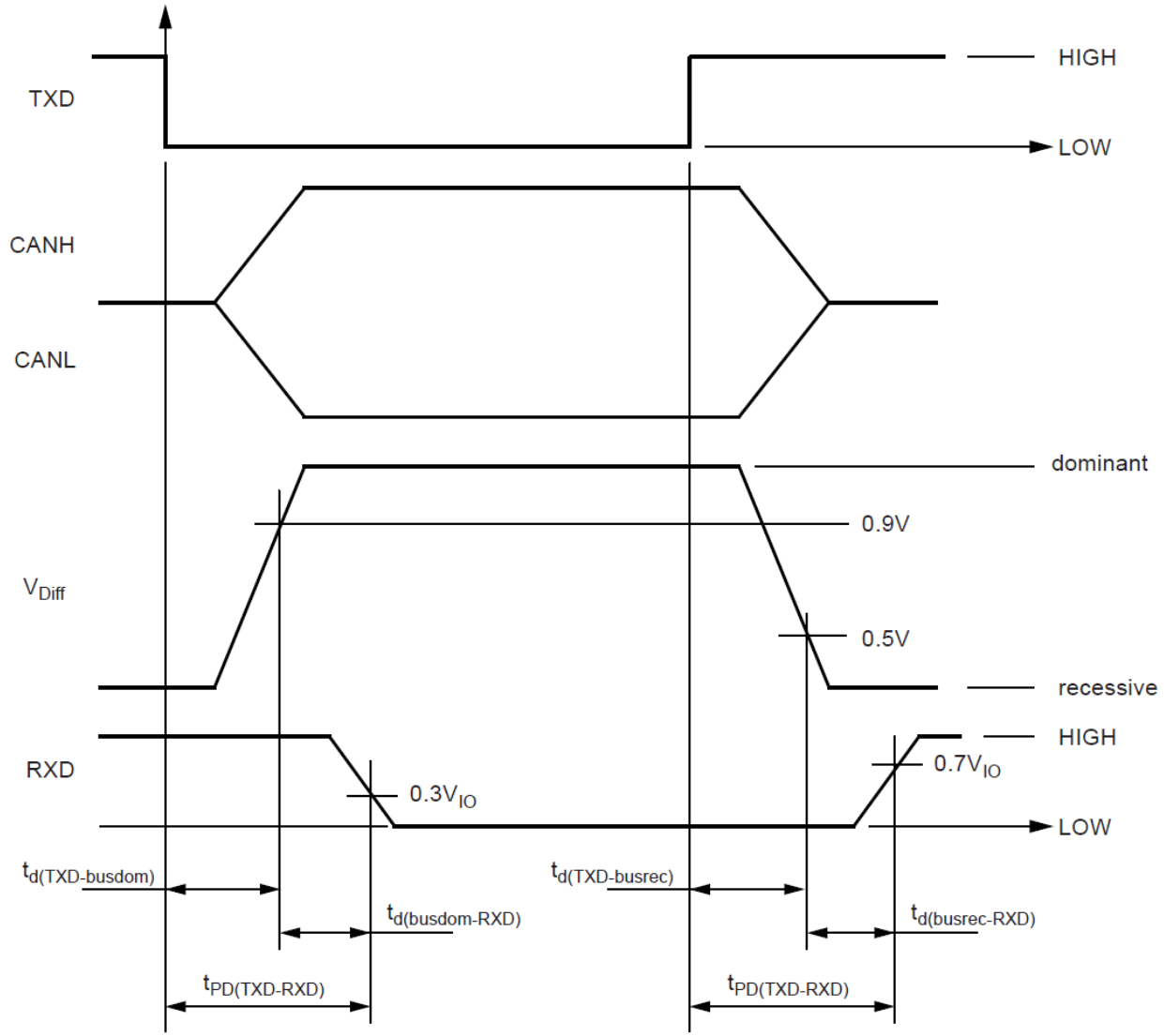
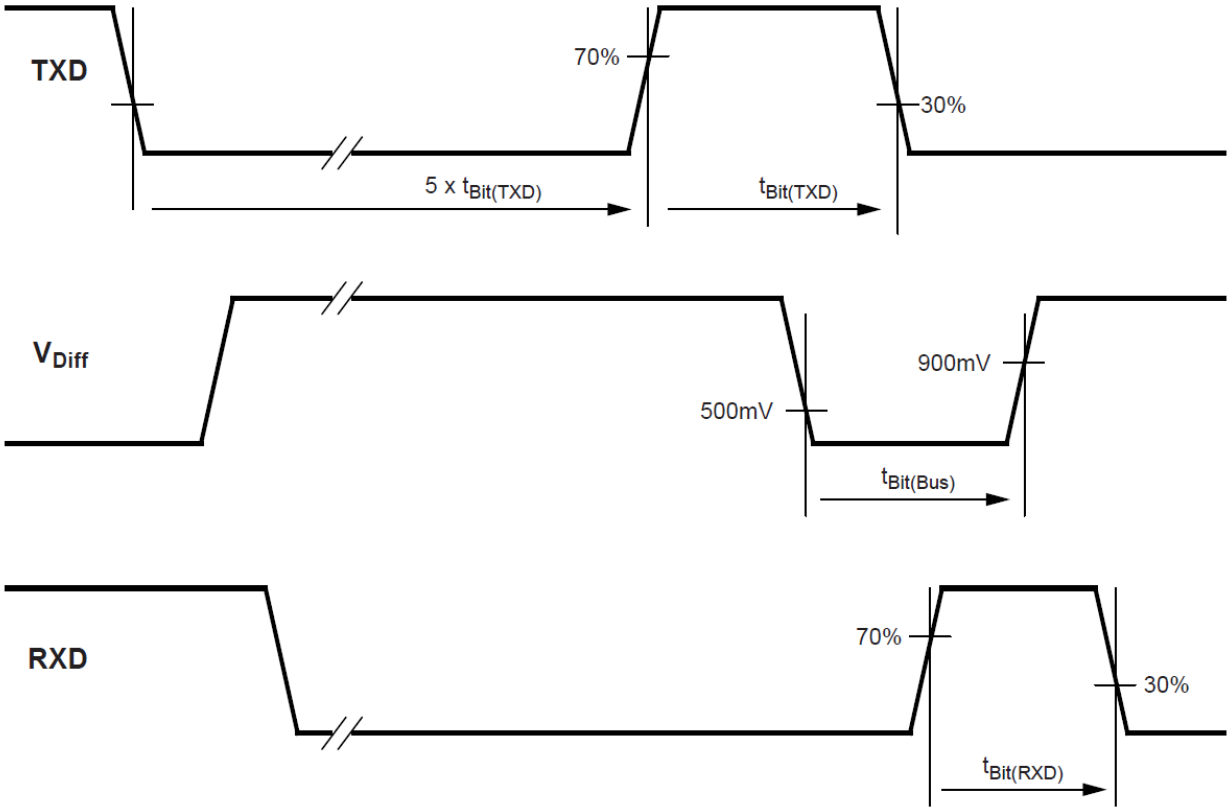
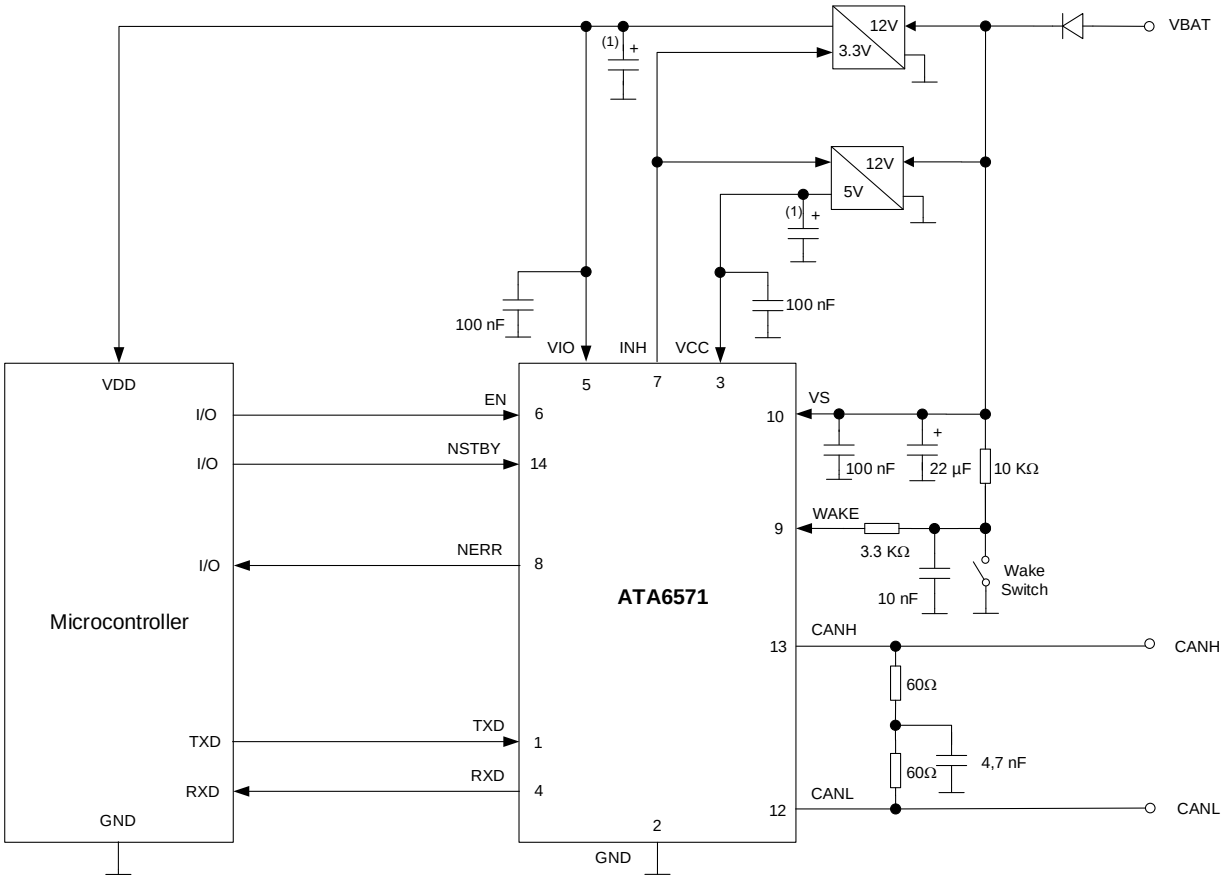


Figure 5-2. CAN Transceiver Timing Diagram 2



6. Application Circuits

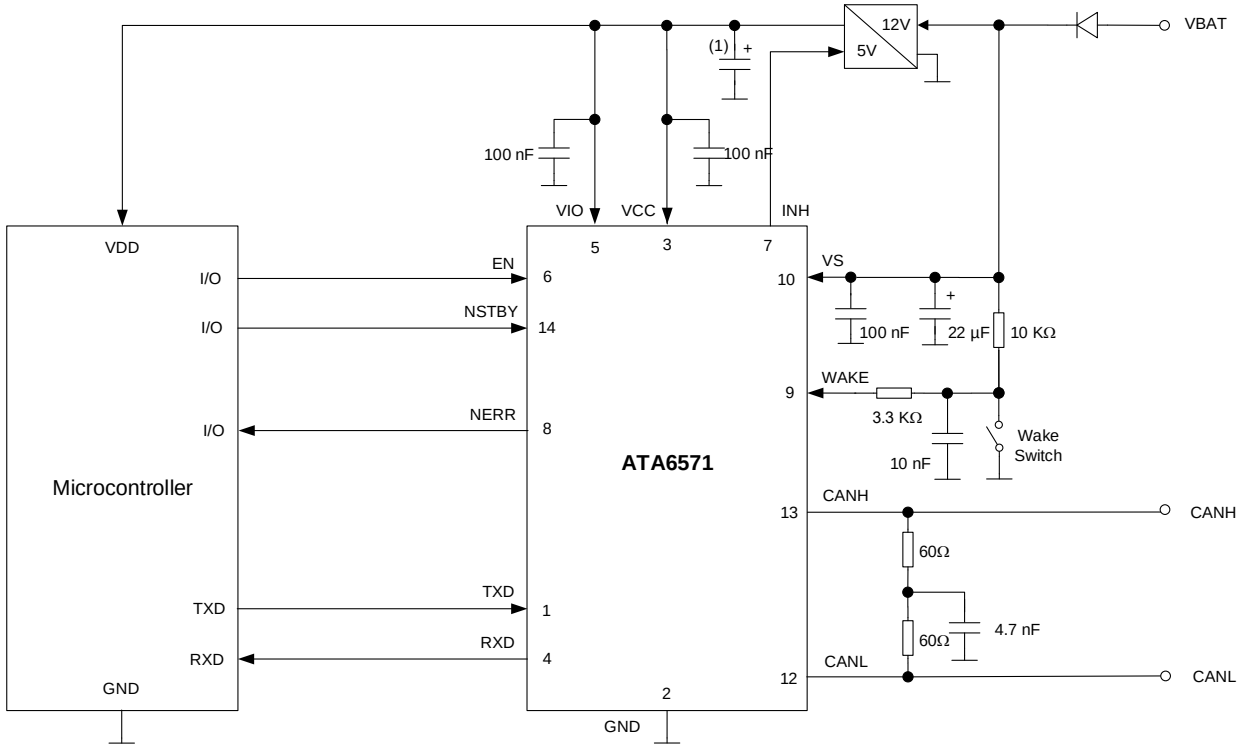
Figure 6-1. Typical Application Circuit



Notes:

1. The value of these capacitors depends on the used external voltage regulators.
2. For the VDFN14 package, the exposed thermal pad must be always connected to GND.

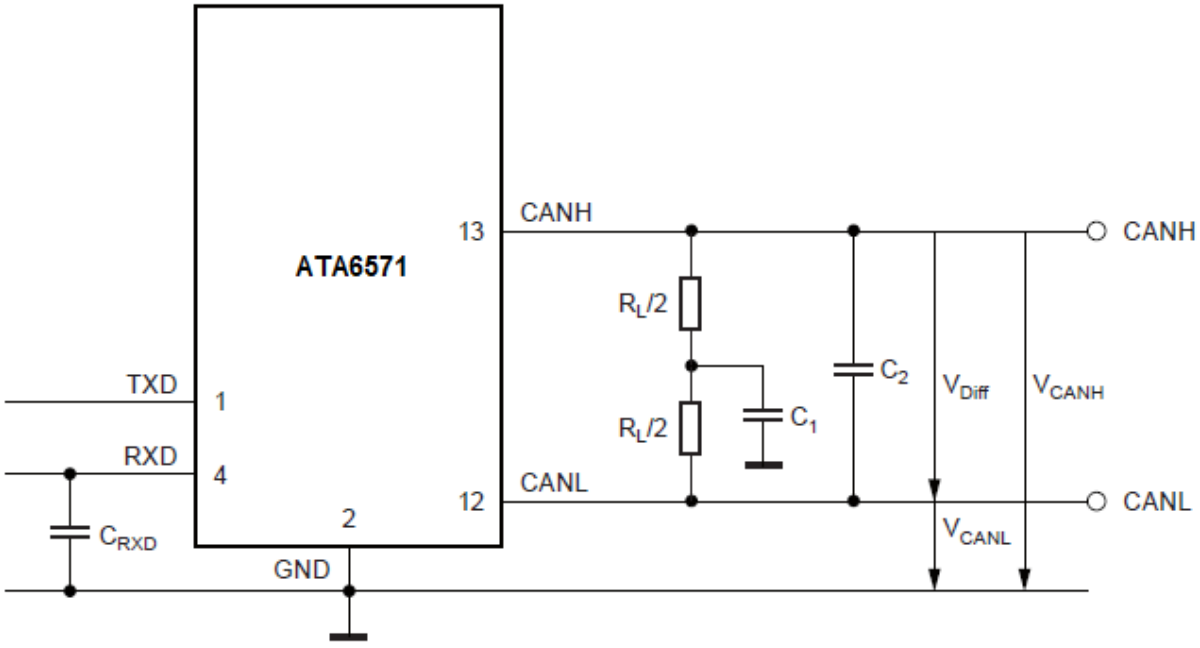
Figure 6-2. Typical Application Circuit 5V Only



Notes:

1. The value of this capacitor depends on the used external voltage regulator.
2. For the VDFN14 package, the exposed thermal pad must be always connected to GND.

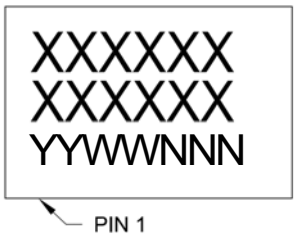
Figure 6-3. Test Circuit



7. Package Information

7.1 Package Marking Information

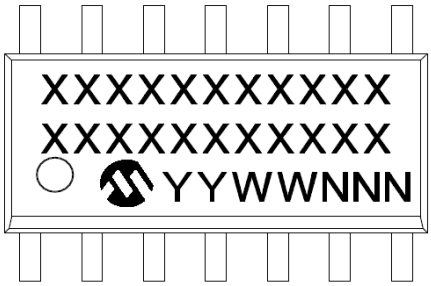
14-Lead 4.5 x 3 mm VDFN



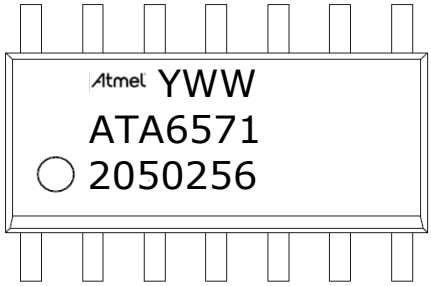
Example Grade 1

Example Grade 0

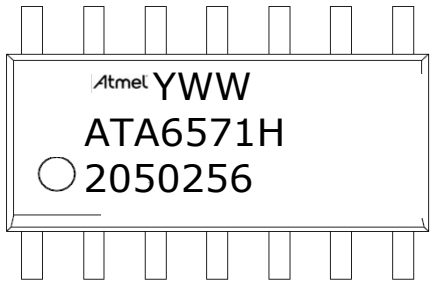
14-Lead 3.90 mm SOIC



Example Grade 1



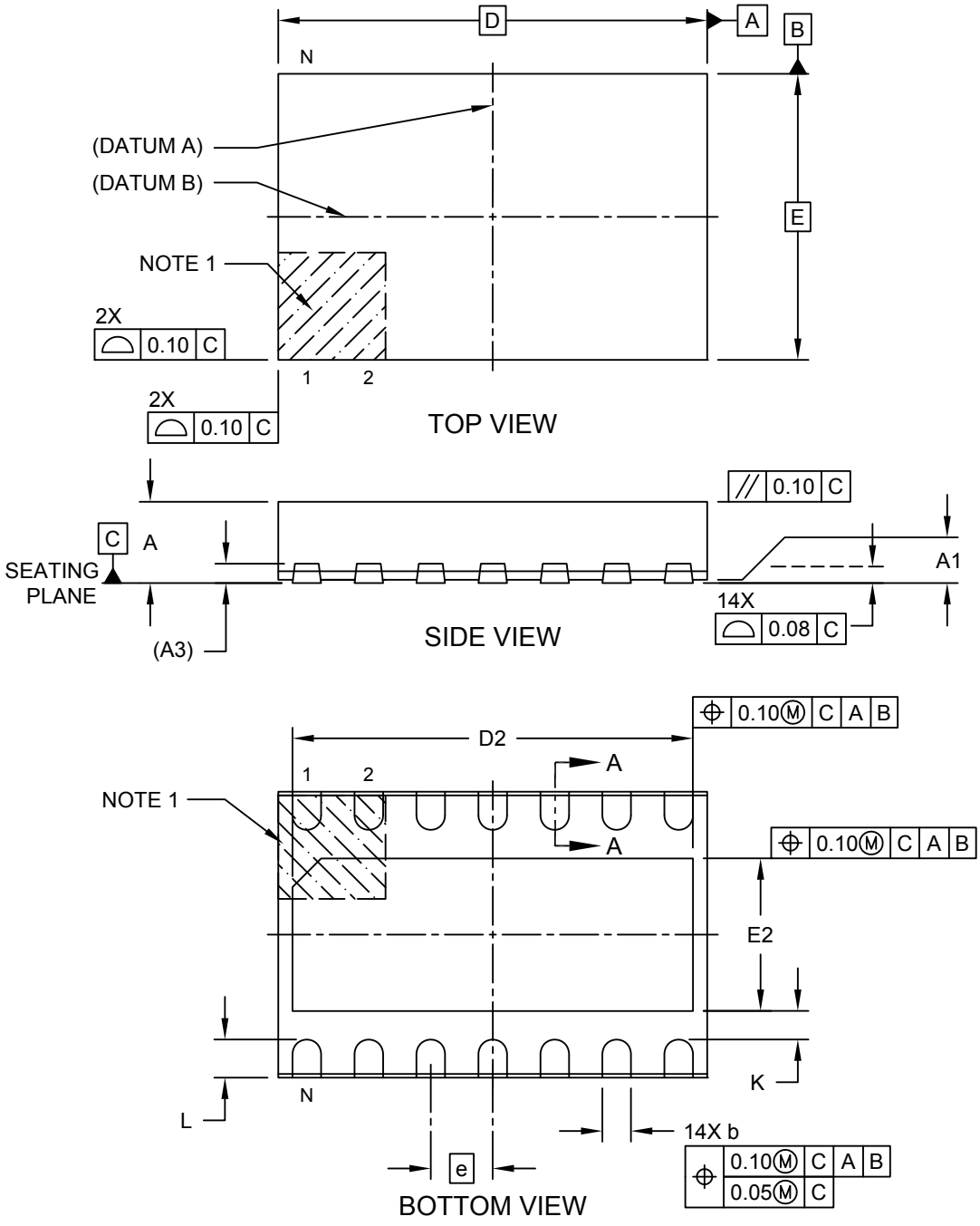
Example Grade 0



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

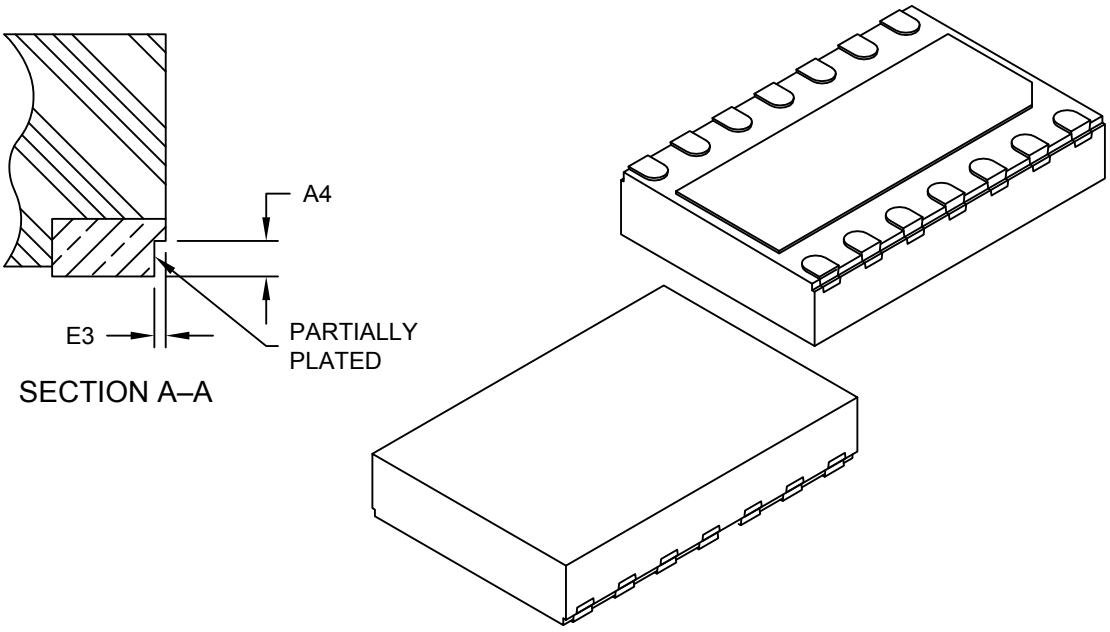
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21361 Rev C Sheet 1 of 2

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.50 BSC	
Exposed Pad Length	D2	4.15	4.20	4.25
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.27	0.32	0.37
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	-	0.19
Wettable Flank Step Cut Width	E3	-	-	0.085

Notes:

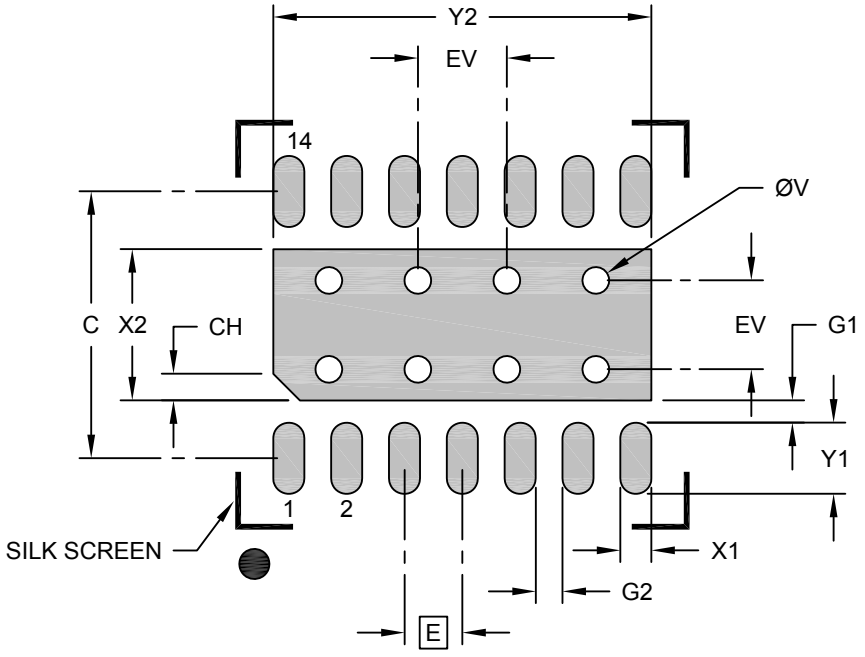
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21361 Rev C Sheet 2 of 2

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C		3.00	
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.80
Pin 1 Index Chamfer	CH		0.30	
Contact Pad to Center Pad (X14)	G1	0.20		
Contact Pad to Center Pad (X12)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

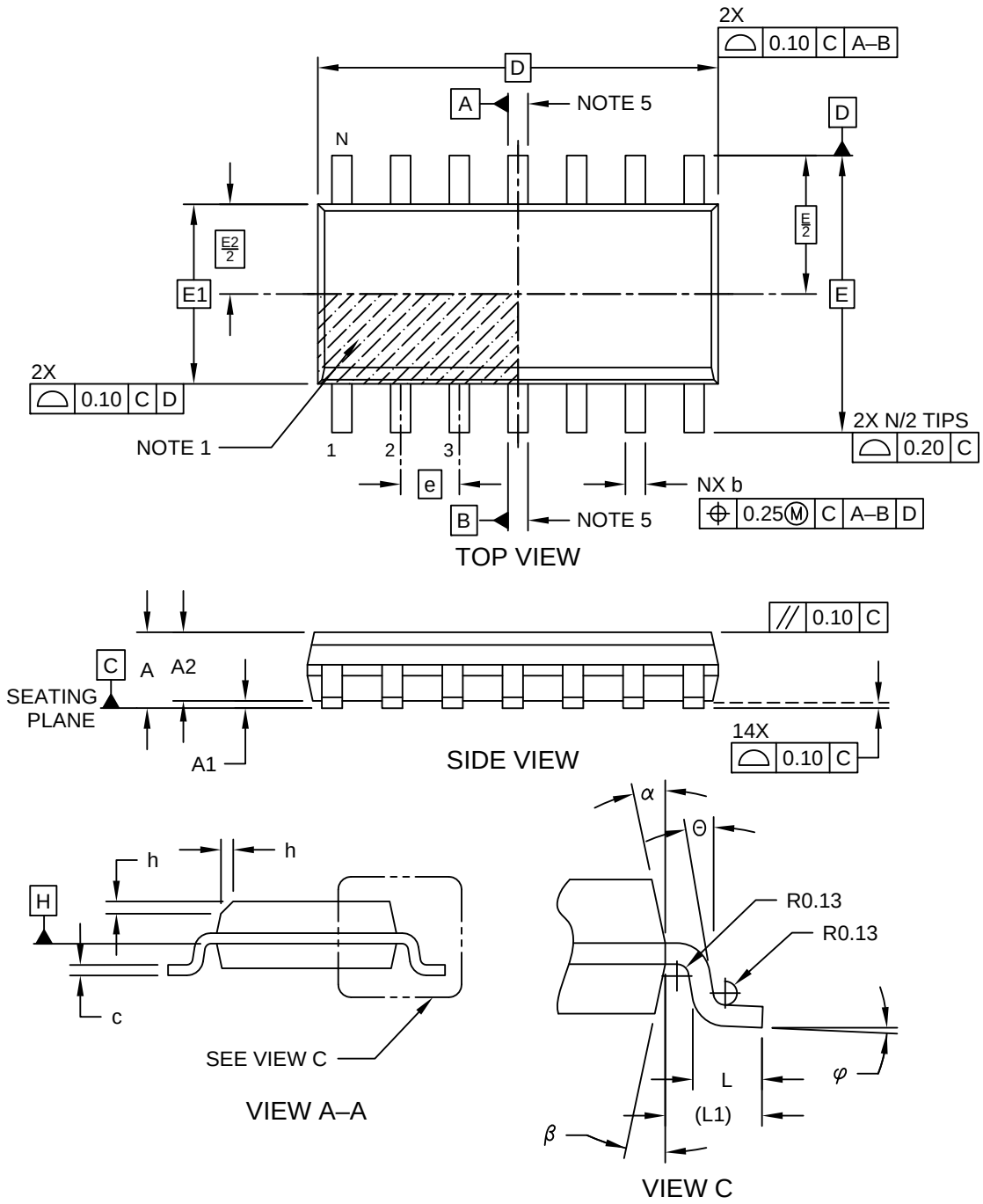
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23361 Rev C

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

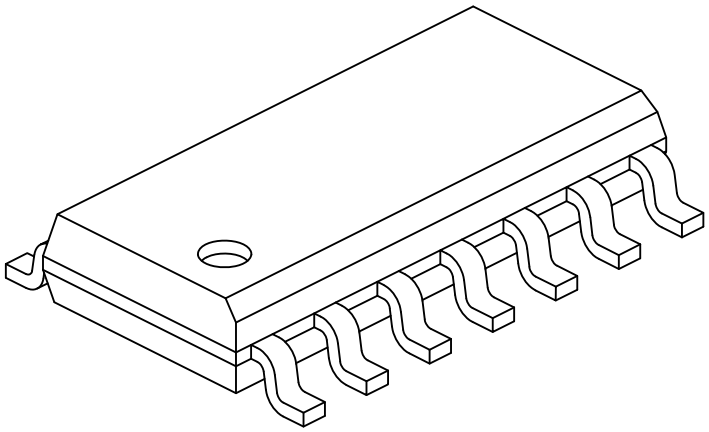
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

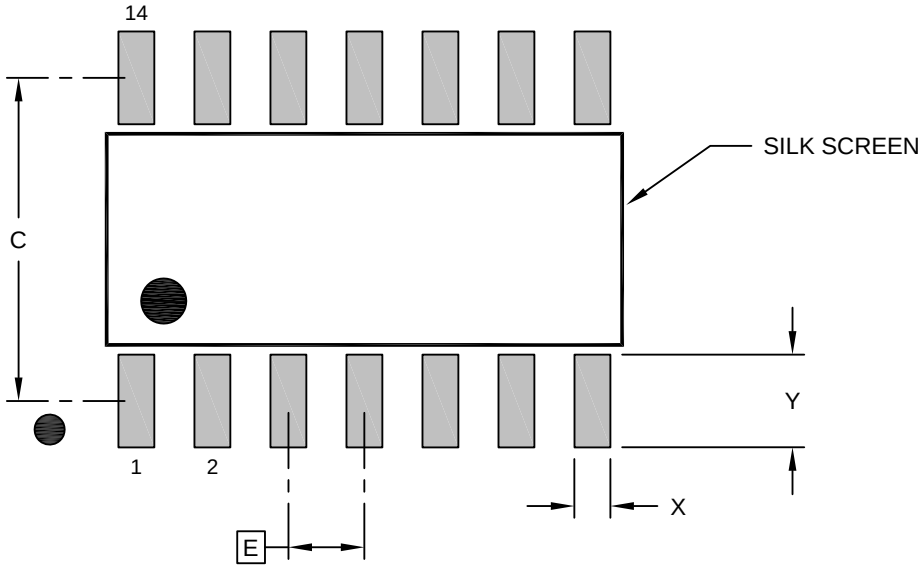
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

8. Revision History

Revision B (January 2021)
The following is the list of modifications:

- Added the VDFN14 package.
- Updated Section Features.
- Updated Section Description.
- Updated Section 1. Pin Configuration.
- Updated Section 6. Application Circuits.
- Updated Section 7.1 Package Marking Information.
- Updated Section Product Identification System.

Revision A (November 2020)
Original Release of this Document.

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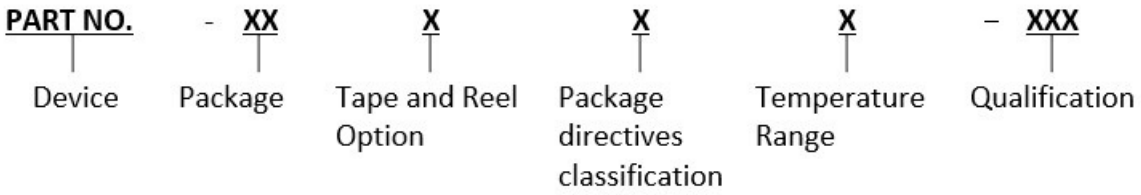

Device:	ATA6571: High-Speed CAN FD Transceiver	
Package	GN	14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body SOIC, Copper Bonds
	GC	14-Lead VDFN with Wettable Flanks (Moisture Sensitivity Level 1)
Tape and Reel Option	Q	330 mm diameter Tape and Reel(1)
Package Directives Classification	W	Package according to RoHS(3)
Temperature Range	0	Temperature Grade 0 (-40ºC to +150ºC)
	1	Temperature Grade 1 (-40ºC to +125ºC)
Qualification	VAO	Automotive

- ATA6571-GNQW0-VAO – High-Speed CAN FD Transceiver, SOIC14 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6571-GNQW1-VAO – High-Speed CAN FD Transceiver, SOIC14 package, Tape and Reel, Grade 1, Automotive qualified
- ATA6571-GCQW0-VAO – High-Speed CAN FD Transceiver, VDFN14 package, Tape and Reel, Grade 0, Automotive qualified
- ATA6571-GCQW1-VAO – High-Speed CAN FD Transceiver, VDFN14 package, Tape and Reel, Grade 1, Automotive qualified

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (CI) and less than 0.15% (1500) total Bromine (Br) and Chlorine (CI) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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