

CD4001B, CD4002B, CD4025B Types

CMOS NOR Gates

High-Voltage Types (20-Volt Rating)

Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

■ CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

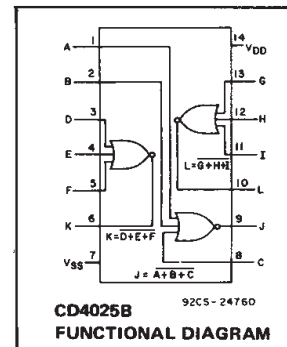
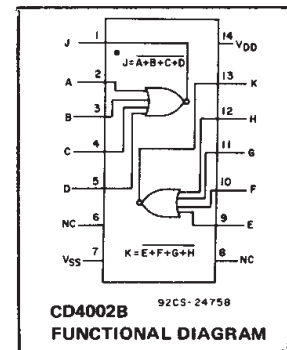
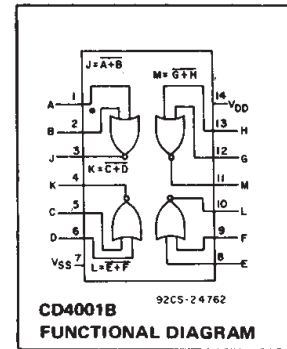
The CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Propagation delay time = 60 ns (typ.) at $C_L = 50 \text{ pF}$, $V_{DD} = 10 \text{ V}$
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of $1 \mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5 \text{ V}$
 - 2 V at $V_{DD} = 10 \text{ V}$
 - 2.5 V at $V_{DD} = 15 \text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD} \text{ Max.}$	–	0,5	5	0,25	0,25	7,5	7,5	–	0,01	0,25	μA
	–	0,10	10	0,5	0,5	15	15	–	0,01	0,5	
	–	0,15	15	1	1	30	30	–	0,01	1	
	–	0,20	20	5	5	150	150	–	0,02	5	
Output Low (Sink) Current $I_{OL} \text{ Min.}$	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	–	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	–	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	–	
	–	–	–	–	–	–	–	–	–	–	
Output High (Source) Current, $I_{OH} \text{ Min.}$	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	–	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	–	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	–	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	–	
Output Voltage: Low-Level, $V_{OL} \text{ Max.}$	–	0,5	5	0,05				–	0	0,05	V
	–	0,10	10	0,05				–	0	0,05	
	–	0,15	15	0,05				–	0	0,05	
Output Voltage: High-Level, $V_{OH} \text{ Min.}$	–	0,5	5	4,95				4,95	5	–	V
	–	0,10	10	9,95				9,95	10	–	
	–	0,15	15	14,95				14,95	15	–	
Input Low Voltage, $V_{IL} \text{ Max.}$	0,5,4,5	–	5	1,5				–	–	1,5	V
	1,9	–	10	3				–	–	3	
	1,5,13,5	–	15	4				–	–	4	
Input High Voltage, $V_{IH} \text{ Min.}$	0,5	–	5	3,5				3,5	–	–	V
	1	–	10	7				7	–	–	
	1,5	–	15	11				11	–	–	
Input Current $I_{IN} \text{ Max.}$		0,18	18	$\pm 0,1$	$\pm 0,1$	± 1	± 1	–	$\pm 10^{-5}$	$\pm 0,1$	μA



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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4001B, CD4002B, CD4025B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} + 0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	
		V_{DD} VOLTS	TYP.		MAX.
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

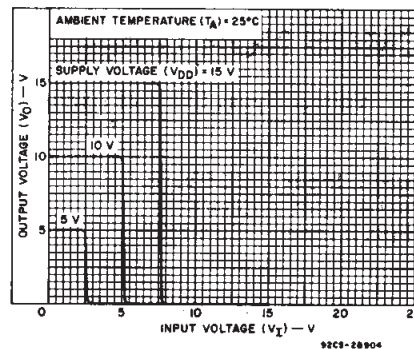


Fig. 1 - Typical voltage transfer characteristics.

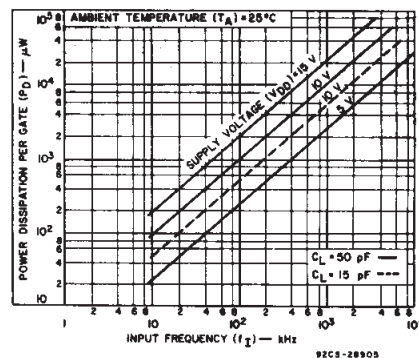


Fig. 2 - Typical power dissipation vs. frequency.

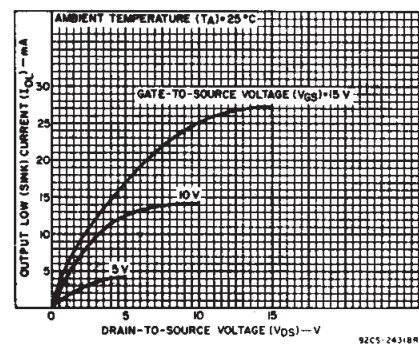


Fig. 3 - Typical output low (sink) current characteristics.

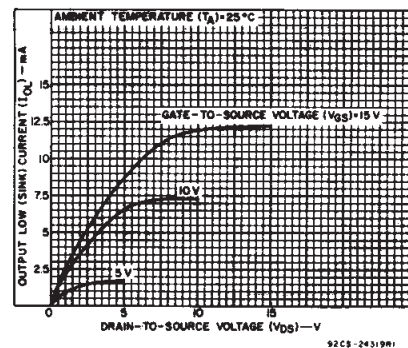


Fig. 4 - Minimum output low (sink) current characteristics.

CD4001B, CD4002B, CD4025B Types



Fig.5 - Schematic and logic diagrams for CD4001B.



Fig.6 - Schematic and logic diagrams for CD4002B.



Fig.7 - Schematic and logic diagrams for CD4025B.

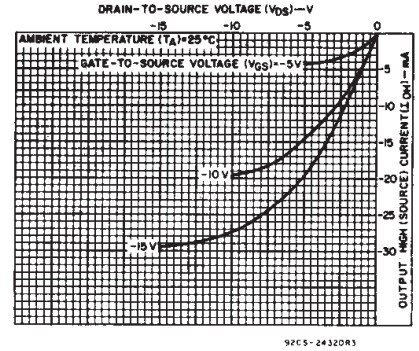


Fig.8 - Typical output high (source) current characteristics.

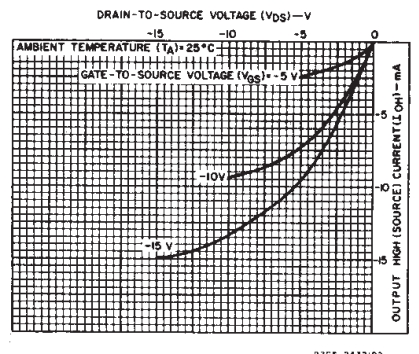


Fig.9 - Minimum output high (source) current characteristics.

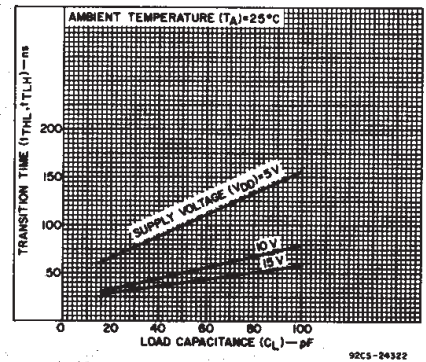


Fig.10 - Typical transition time vs. load capacitance.

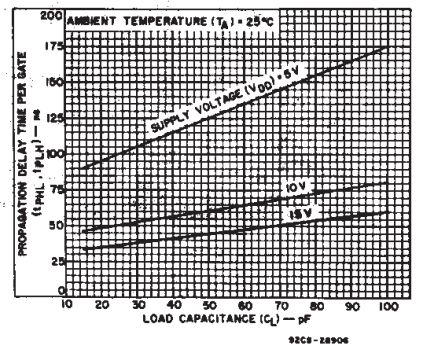


Fig.11 - Typical propagation delay time vs. load capacitance.

COMMERCIAL CMOS HIGH VOLTAGE ICs

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Fig. 13 - Input leakage current test circuit.



Fig. 14 - Input-voltage test circuit.

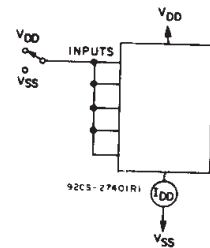
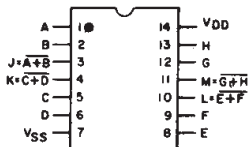


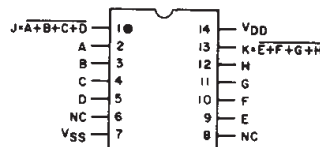
Fig. 15 - Quiescent-device current test circuit.

TERMINAL ASSIGNMENTS (TOP VIEW)



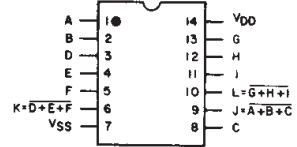
NC = NO CONNECTION

CD4001B



NC = NO CONNECTION

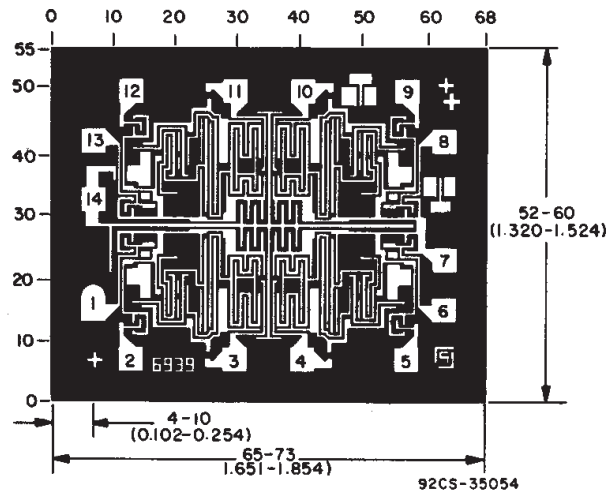
CD4002B



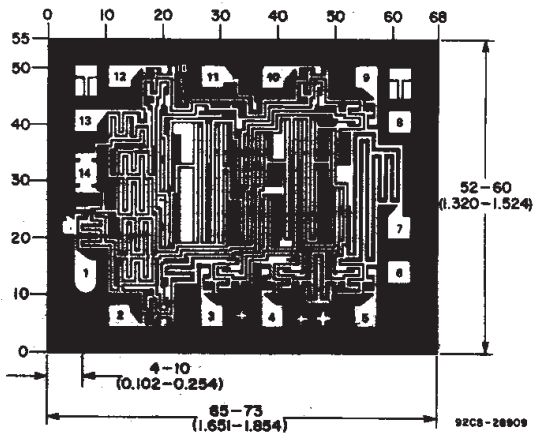
NC = NO CONNECTION

CD4025B

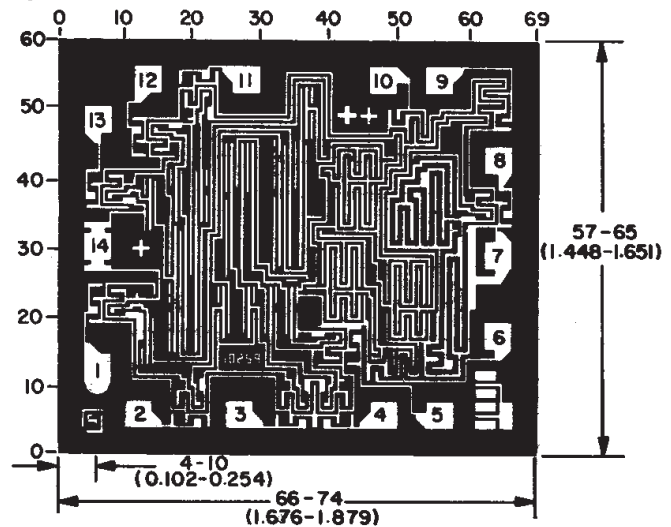
Chip Dimensions and Pad Layouts



CD4001B



CD4002B



CD4025B

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



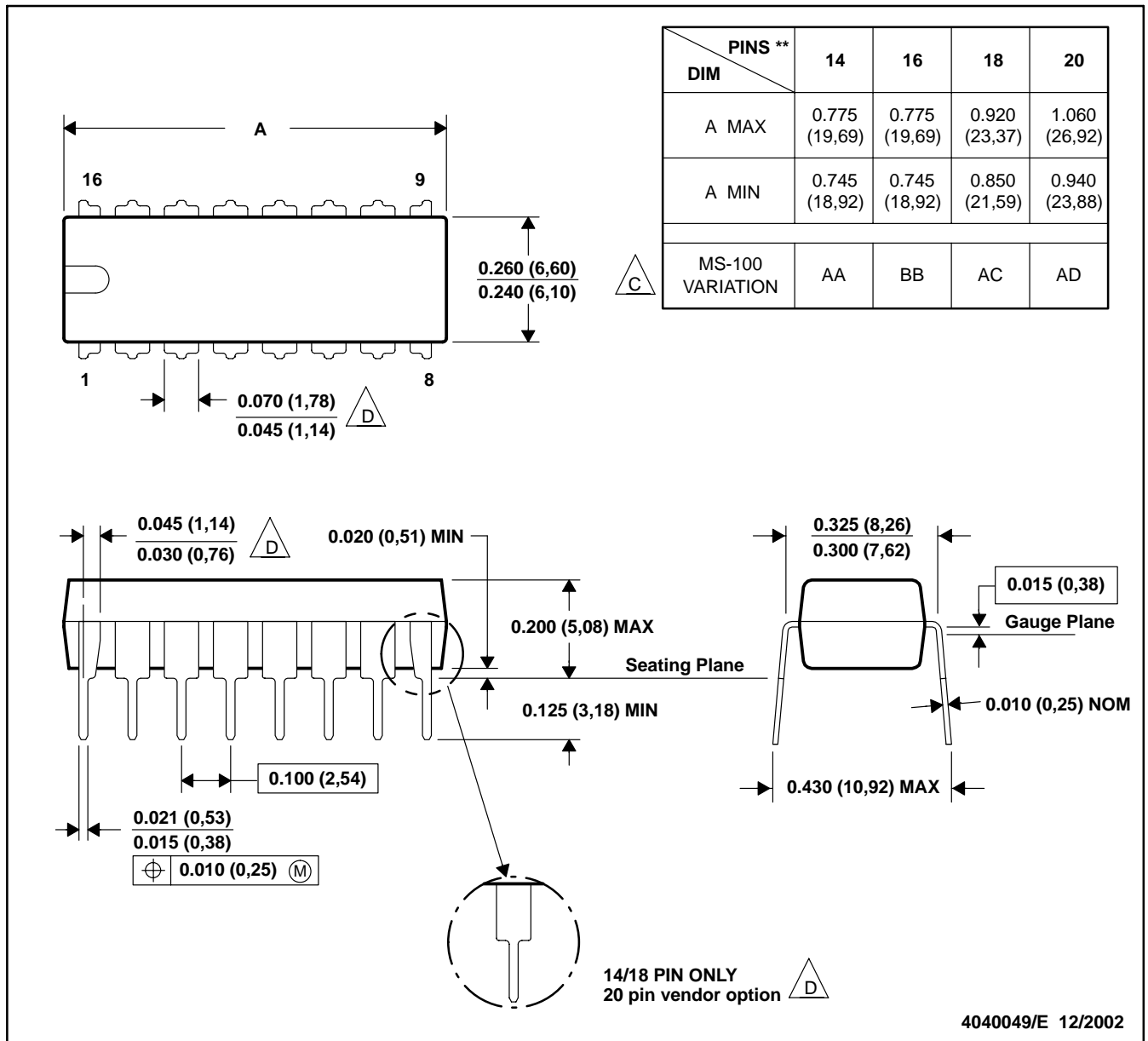
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

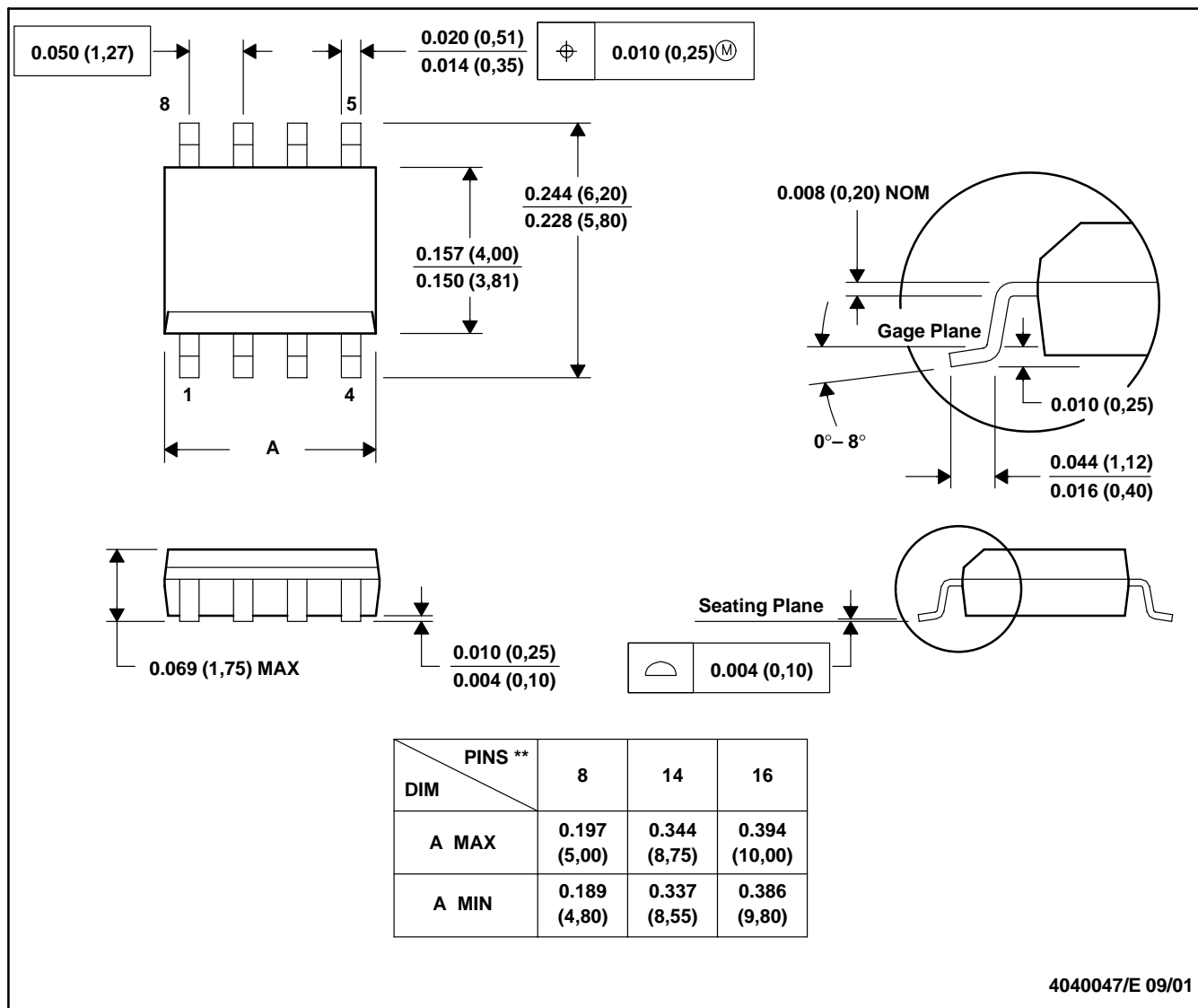


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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