

# CM1248-08DE

## ESD Protection Diode

### Low Capacitance

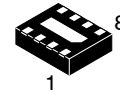
#### Features

- Low I/O Capacitance at 10 pF at 0 V
- In-System ESD Protection to  $\pm 15$  kV Contact Discharge, per the IEC 61000-4-2 International Standard
- Compact SMT Package Saves Board Space and Facilitates Layout in Space-Critical Applications
- Each I/O Pin Can Withstand over 1000 ESD Strikes
- These Devices are Pb-Free and are RoHS Compliant



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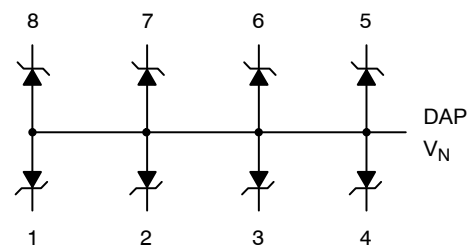
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UDFN-8  
DE SUFFIX  
CASE 517BC

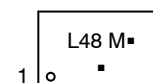
#### BLOCK DIAGRAM

CM1248-08DE



Note: DAP (Die Attach Pad) is on back-side of chip.

#### MARKING DIAGRAM



L48 = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

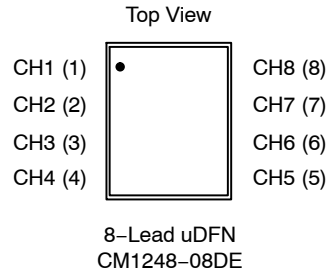
#### ORDERING INFORMATION

Device	Package	Shipping†
CM1248-08DE	uDFN-8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# CM1248-08DE

## PACKAGE / PINOUT DIAGRAMS



**Table 1. PIN DESCRIPTIONS**

Pins	Name	Description
(Refer to package / pinout diagrams)	CHx	The cathode of the respective surge protection diode, which should be connected to the node requiring transient voltage protection.
(Refer to package / pinout diagrams)	V <sub>N</sub>	The anode of the surge protection diodes.

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Storage Temperature Range	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. STANDARD OPERATING CONDITIONS**

Parameter	Rating	Units
Operating Temperature	-40 to +85	°C

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C <sub>IN</sub>	Channel Input Capacitance	T <sub>A</sub> = 25°C, 0 VDC, 1 MHz		10		pF
		0 VDC, 1 MHz	7		15	pF
ΔC <sub>IN</sub>	Differential Channel I/O to GND Capacitance	T <sub>A</sub> = 25°C, 2.5 VDC, 1 MHz		0.19		pF
V <sub>RSO</sub>	Reverse Stand-off Voltage	I <sub>R</sub> = 10 μA, T <sub>A</sub> = 25°C	5.5			V
		I <sub>R</sub> = 1 mA, T <sub>A</sub> = 25°C	6.1			V
I <sub>LEAK</sub>	Leakage Current	V <sub>IN</sub> = 5.0 VDC, T <sub>A</sub> = 25°C			0.25	μA
		V <sub>IN</sub> = 5.0 VDC			0.75	μA
V <sub>SIG</sub>	Small Signal Clamp Voltage Positive Clamp Negative Clamp	I = 10 mA, T <sub>A</sub> = 25°C I = -10 mA, T <sub>A</sub> = 25°C		6.8 -0.89		V
V <sub>ESD</sub>	ESD Withstand Voltage Contact Discharge per IEC 61000-4-2 standard	T <sub>A</sub> = 25°C (Notes 2 and 3)	±15			kV
R <sub>D</sub>	Diode Dynamic Resistance Forward Conduction Reverse Conduction	T <sub>A</sub> = 25°C, I <sub>PP</sub> = 1 A, t <sub>p</sub> = 8/20 μs		0.57 1.36		Ω

- All parameters specified at T<sub>A</sub> = -40°C to +85°C unless otherwise noted.
- Standard IEC 61000-4-2 with C<sub>Discharge</sub> = 150 pF, R<sub>Discharge</sub> = 330 Ω, V<sub>N</sub> grounded.
- These measurements performed with no external capacitor on CH<sub>x</sub>.

PERFORMANCE INFORMATION

**Diode Capacitance**

Typical diode capacitance with respect to positive cathode voltage (reverse voltage across the diode) is given in Diode Capacitance vs. Reverse Voltage.

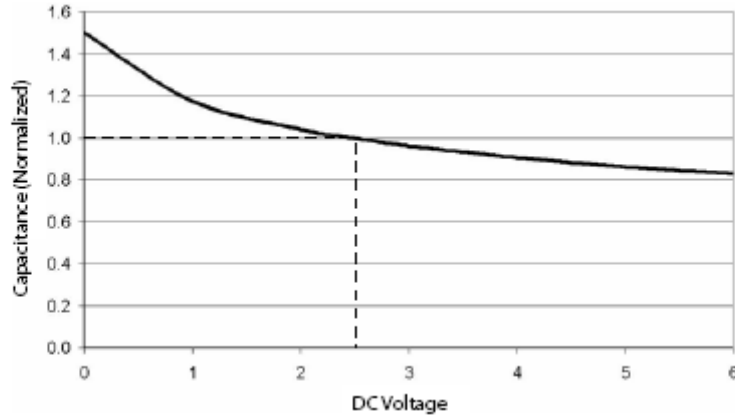


Figure 1. Diode Capacitance vs. Reverse Voltage

**Typical High Current Diode Characteristics**

Measurements are made in pulsed mode with a nominal pulse width of 0.7 ms.

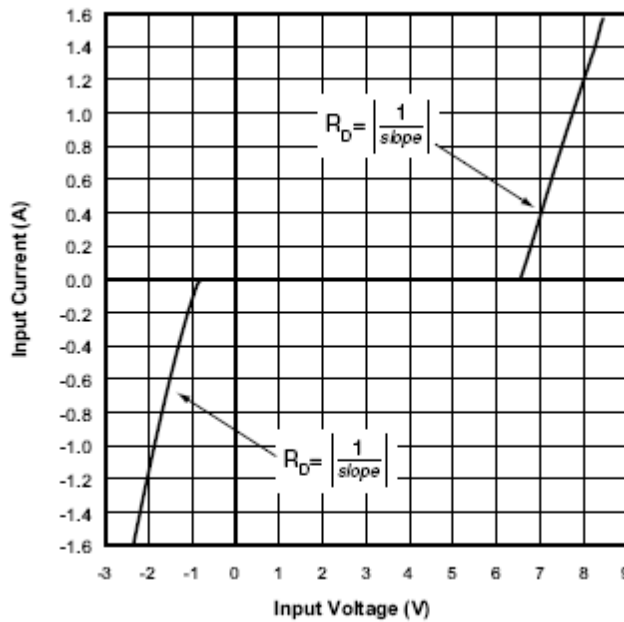
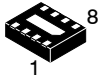


Figure 2. Typical Input VI Characteristics  
(Pulse-mode Measurements, Pulse Width = 0.7 ms nominal)

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

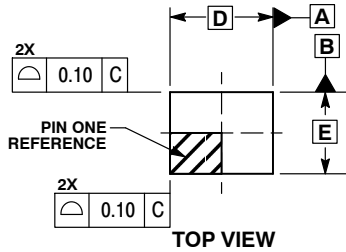
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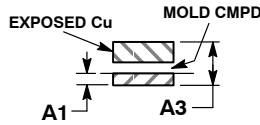
SCALE 4:1

UDFN8, 1.7x1.35, 0.4P  
CASE 517BC-01  
ISSUE O

DATE 17 NOV 2009



TOP VIEW

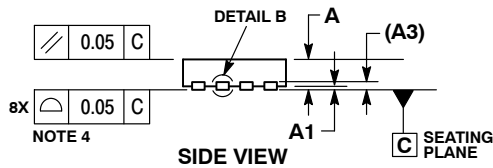


DETAIL B  
ALTERNATE  
CONSTRUCTIONS

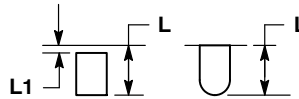
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

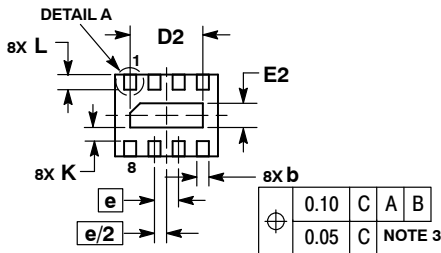
MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.70	BSC
D2	1.10	1.30
E	1.35	BSC
E2	0.30	0.50
e	0.40	BSC
K	0.15	---
L	0.20	0.30
L1	---	0.05



SIDE VIEW

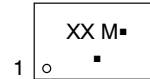


DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*

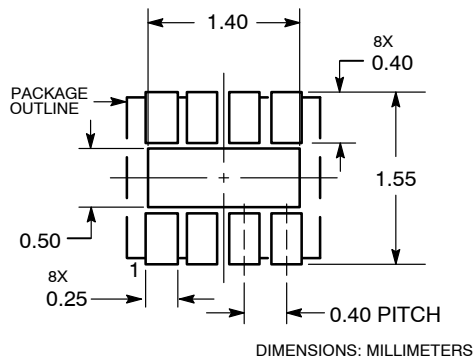


- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	8 PIN UDFN, 1.7X1.35, 0.4P	PAGE 1 OF 1

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