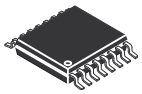
Document Number: MPC17533
Rev. 3.0, 12/2013

0.7 A 6.8 V Dual H-Bridge Motor Driver

17533

H-BRIDGE MOTOR DRIVER



EV SUFFIX (Pb-FREE)
98ASA10614D
16-PIN VMFP

The 17533 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar stepper motors and/or brush DC-motors (e.g., cameras and disk drive head positioners).

The 17533 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible logic). The device features built-in shoot-through current protection and an undervoltage shutdown function.

The 17533 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The 17533 has a low total $R_{DS(ON)}$ of 1.2 Ω (max at 25 °C).

The 17533's low output resistance and high slew rate provides efficient drive for many types of micromotors.

Features

- Low total $R_{DS(ON)}$ 0.8 Ω (typ), 1.2 Ω (max) at 25 °C
- Output current 0.7 A (DC), 1.4 A (peak)
- Shoot-through current protection circuit
- 3.0 V/5.0 V CMOS-compatible inputs
- PWM control Input frequency up to 200 kHz
- Built-in 2-channel H-Bridge driver
- Low power consumption
- Undervoltage detection and shutdown circuit

ORDERING INFORMATION		
Device (For Tape and Reel, add an R2 Suffix)	**Temperature Range (T_A)**	**Package**
MPC17533EV/EL	-20 °C to 65 °C	16 VMFP

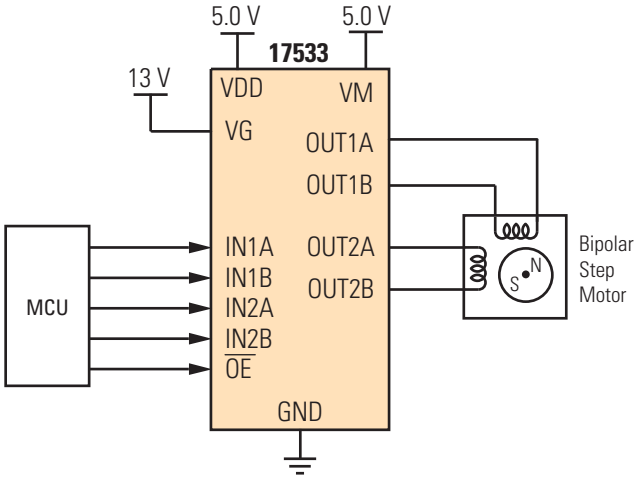


Figure 1. 17533 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

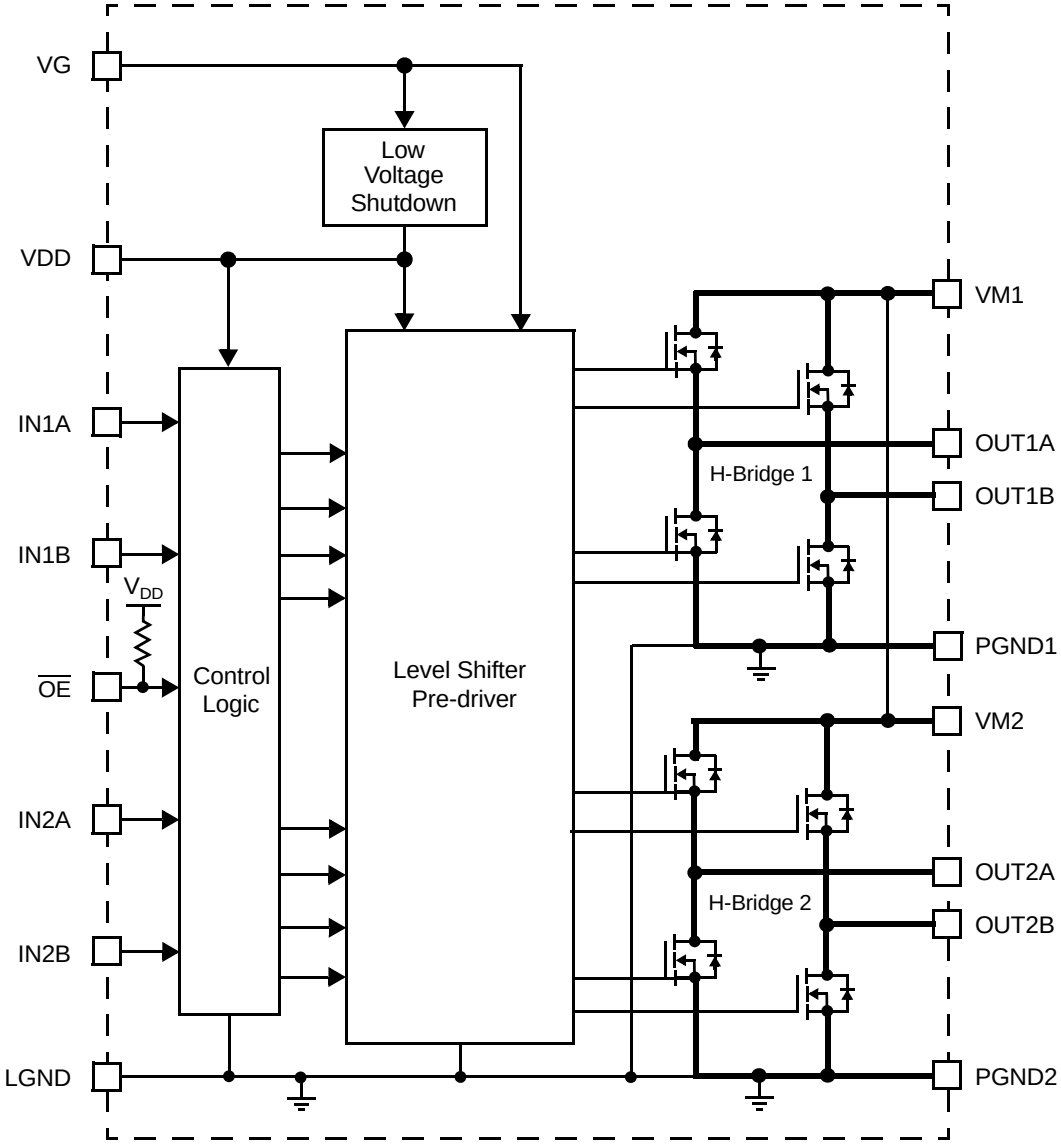


Figure 2. 17533 Simplified Internal Block Diagram

PIN CONNECTIONS

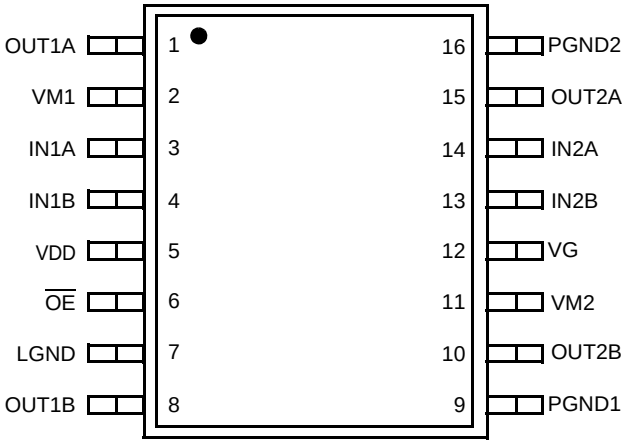


Figure 3. 17533 Pin Connections

Table 1. PIN Function Description

Pin	Pin Name	Formal Name	Definition
1	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
2	VM1	Motor Drive Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).
3	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 5, Truth Table, page 7).
4	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 5, Truth Table, page 7).
5	VDD	Logic Supply	Control circuit power supply pin.
6	$\overline{OE}$	Output Enable	Logic output Enable control of H-Bridges (Low = True).
7	LGND	Logic Ground	Low-current logic signal ground.
8	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
9	PGND1	Power Ground 1	High-current power ground 1.
10	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
11	VM2	Motor Drive Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).
12	VG	Gate Driver Circuit Voltage Input	Input pin for the gate drive voltage.
13	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 5, Truth Table, page 7).
14	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 5, Truth Table, page 7).
15	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
16	PGND2	Power Ground 2	High-current power ground 2.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Gate Driver Circuit Power Supply Voltage	V_G	-0.5 to 14	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (1)	 I_O I_{OPK}	 0.7 1.4	A
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±1500 ±200	V
Operating Junction Temperature	T_J	-55 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C
Thermal Resistance (3)	$R_{\theta JA}$	150	°C/W
Power Dissipation (4)	P_D	830	mW
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C

Notes

1. T_A = 25°C. 10 ms pulse at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Mounted on 37 mm x 50 mm x 1.6 mm glass epoxy board mount.
4. T_A = 25 °C.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = V_M = 5.0 V, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.7	V
Quiescent Power Supply Current					µA
Driver Circuit Power Supply Current	I_{QM}	–	–	1.0	
Logic Supply Current (7)	I_{QVDD}	–	–	20	
Gate Driver Circuit Power Supply Current	I_{QVG}	–	–	150	
Operating Power Supply Current					mA
Logic Supply Current (8)	I_{VDD}	–	–	3.0	
Gate Driver Circuit Power Supply Current (9)	I_{VG}	–	–	0.7	
Low V_{DD} Detection Voltage (10)	V_{DDDET}	1.5	2.0	2.5	V
Driver Output ON Resistance					Ω
Source+Sink at I_O = 0.7 A (11)	$R_{DS(ON)}$	–	0.8	1.2	
V_G = 9.5 V, V_M = 5.0 V, T_A = 25 °C (12)	$R_{DS(ON)2}$	–	–	1.5	
GATE DRIVE					
Gate Drive Circuit Power Supply Voltage	V_G	12	13	13.5	V
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Inputs (2.7 V < V_{DD} < 5.7 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	µA
Low-Level Input Current	I_{IL}	-1.0	–	–	µA
$\overline{OE}$ Pin Input Current Low	I_{IL}-$\overline{OE}$	–	50	100	µA

Notes

7. IQ_{VDD} includes the current to pre-driver circuit.
8. $I_{V_{DD}}$ includes the current to pre-driver circuit at f_{IN} = 100 kHz.
9. At f_{IN} = 20 kHz.
10. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When gate voltage V_G is applied from an external source, V_G = 7.5 V.
11. The total H-Bridge ON resistance when VG is 13 V.
12. Increased $R_{DS(ON)}$ value as the result of a reduced VG value of 9.5 V.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = V_M = 5.0 V, GND = 0 V, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (13)	t_R	–	–	1.0 (14)	µs
Input Pulse Fall Time (15)	t_F	–	–	1.0 (14)	µs
OUTPUT					
Propagation Delay Time (16)					µs
Turn-ON Time	t_{PLH}	–	0.1	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Low Voltage Detection Time(17)	t_{VDDDET}	–	–	10	ms

Notes

13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. Load of Output is 8.0 Ω resistance. see Figure 4
17. See Figure 5

TIMING DIAGRAMS

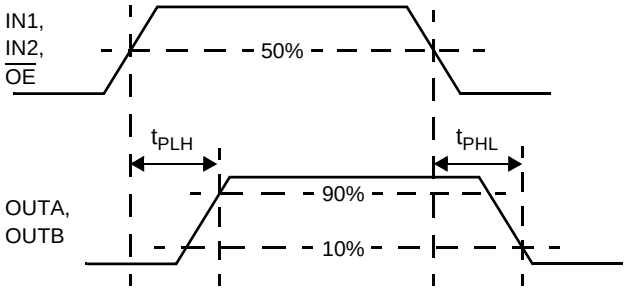


Figure 4. t_{PLH}, t_{PHL}, and t_{PZH} Timing

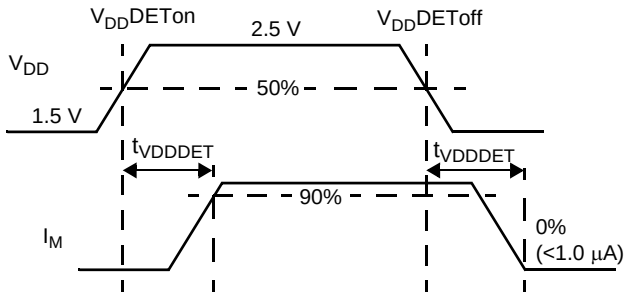


Figure 5. Low-Voltage Detection Timing Diagram

Table 5. Truth Table

INPUT			OUTPUT	
$\overline{OE}$	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B
L	L	L	L	L
L	H	L	H	L
L	L	H	L	H
L	H	H	Z	Z
H	X	X	Z	Z

H = High.
L = Low.
Z = High-impedance.
X = Don't care.
$\overline{OE}$ pin is pulled up to V_{DD} with internal resistance.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17533 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar stepper motors and brush DC motors, such as those found in camera len assemblies, camera shutters, optical disk drives, etc.

The 17533 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible I/O). The device features built-in shoot-through current protection and undervoltage shutdown.

The 17533 has four operating modes: forward, reverse, brake, and tri-Stated (high-impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2\ \Omega$.

The 17533 can simultaneously drive two brush DC motors or, as shown in Figure 1, 17533 Simplified Application Diagram on page 1, one bipolar stepper motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

FUNCTIONAL PIN DESCRIPTION

LOGIC SUPPLY (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input control pins.

LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output (e.g., IN1A logic HIGH = OUT1A HIGH, etc.). However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 5, Truth Table, page 7).

OUTPUT ENABLE ($\overline{OE}$)

The $\overline{OE}$ pin is a LOW = TRUE enable input. When $\overline{OE}$ = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (high-impedance), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states.

OUTPUT A AND B OF H-BRIDGE CHANNEL 1 AND 2 (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see Figure 2, 17533 Simplified Internal Block Diagram, page 2).

MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output pins. All VM pins must be connected together on the printed circuit board.

GATE DRIVER CIRCUIT VOLTAGE INPUT (VG)

The VG pin is the input pin for the gate drive voltage.

POWER GROUND (PGND)

Power ground pins. They must be tied together on the PCB.

LOGIC GROUND (LGND)

Logic ground pin.

TYPICAL APPLICATIONS

INTRODUCTION

Figure 6 shows a typical application for the 17533. When applying the gate voltage to the VG pin from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = V_G/0.02\ \Omega$.

Care must be taken to provide sufficient gate-source voltage for the high-side MOSFETs when $V_M >> V_{DD}$ (e.g., $V_M = 5.0$ V, $V_{DD} = 3.0$ V), in order to ensure full enhancement of the high-side MOSFET channels.

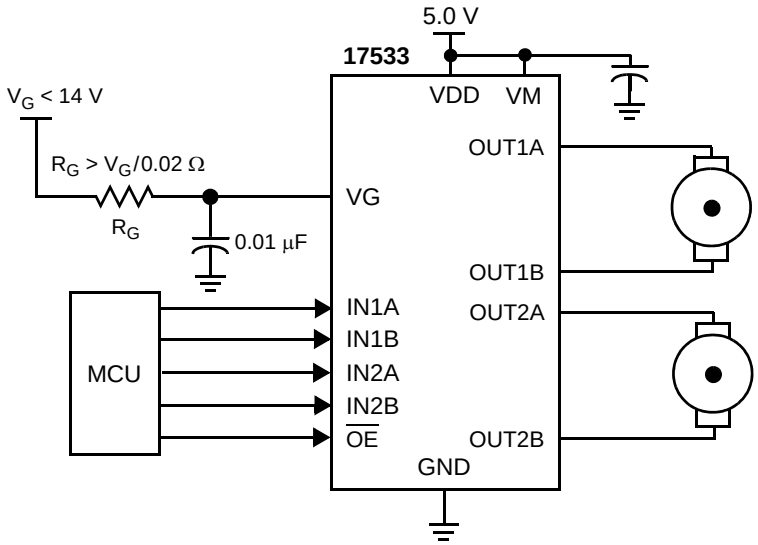


Figure 6. 17533 Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commuting currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a zener or a capacitor at the supply pin (VM) (see Figure 7).

PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

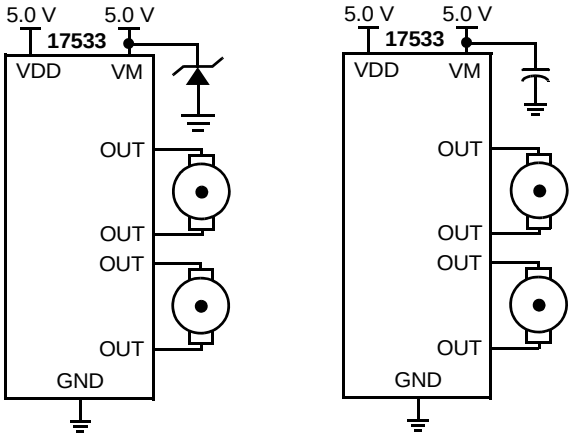


Figure 7. CEMF Snubbing Techniques

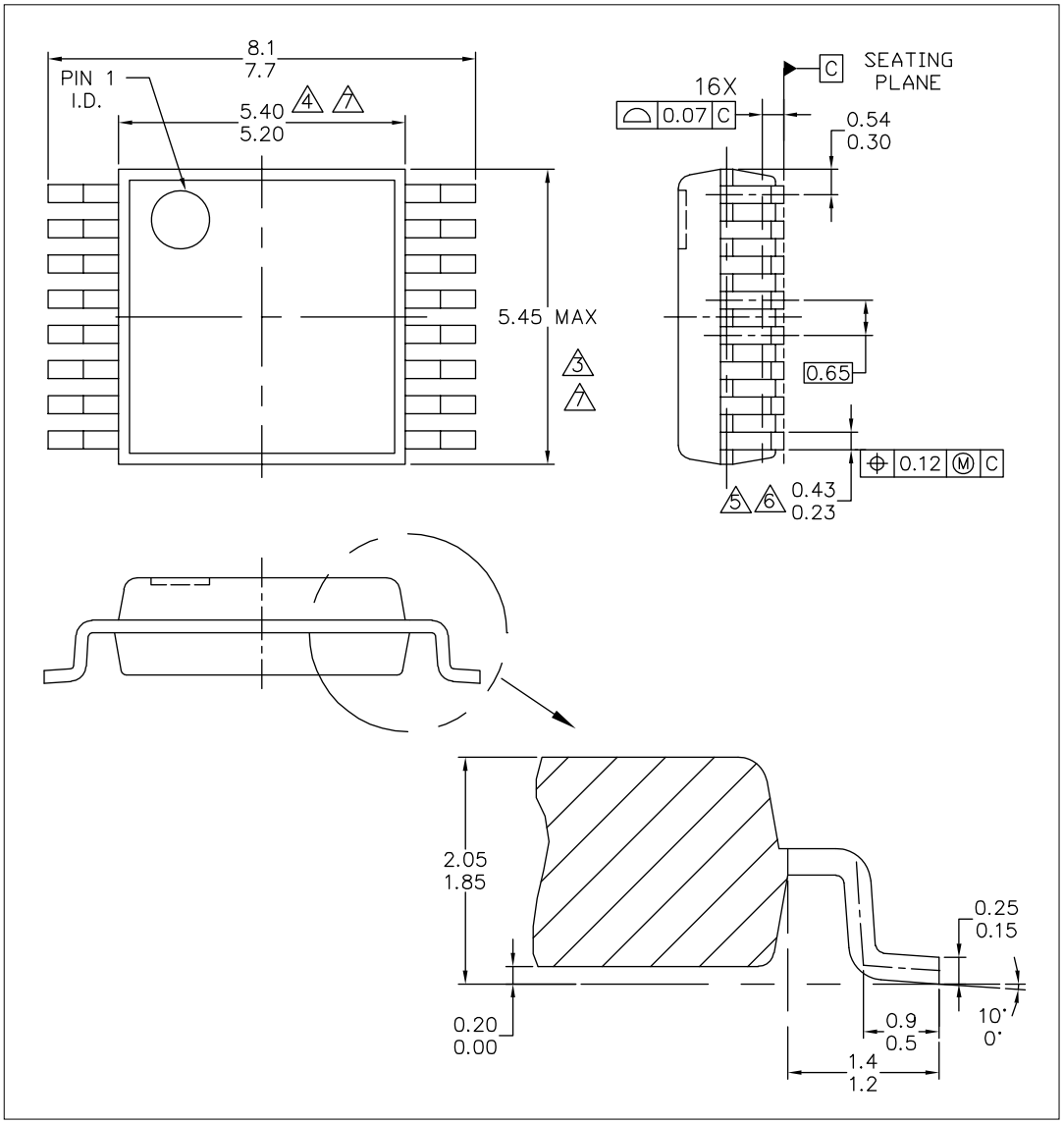
PACKAGING

PACKAGE DIMENSIONS

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 6.

Package	Suffix	Package Outline Drawing Number
16-PIN VMFP	EV	98ASA10614D



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TITLE: 16LD VMFP, 5.30 X 5.45 PKG 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ASA10614D	REV: B
	CASE NUMBER: 1563-02	07 NOV 2007
	STANDARD: NON-JEDEC	

EV (Pb-FREE) SUFFIX
16-LEAD VMFP
98ASA10614D
ISSUE B

17533

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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TITLE: 16LD VMFP, 5.30 X 5.45 PKG 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ASA10614D	REV: B
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	STANDARD: NON-JEDEC	

EV (Pb-FREE) SUFFIX
16-LEAD VMFP
98ASA10614D
ISSUE B

17533

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	5/2006	• Converted to Freescale format • Added Revision History page
3.0	7/2006	• Updated to the prevailing form and style • Corrected device isometric drawing on page 1 • Added RoHS compliance
	12/2013	• No technical changes • Revised back page • Updated document properties

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