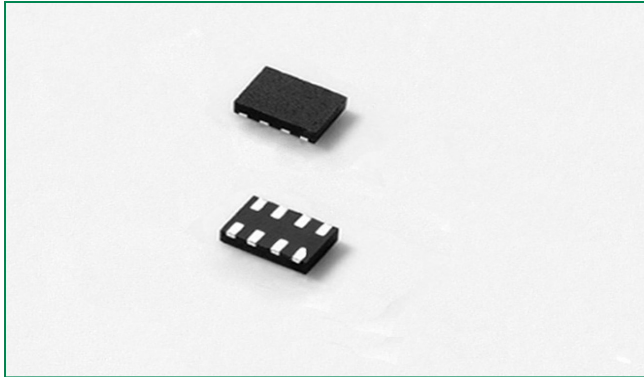
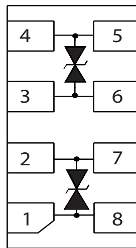
# SP3312T Series 3.3V 15A Diode Array



## Description

The SP3312T integrates 4 channels (2 differential pair) of low capacitance diodes to protect sensitive I/O pins against lightning induced surge events and ESD. This robust device can safely absorb up to 15A per IEC61000-4-5 ($t_p$=8/20μs) without performance degradation and a minimum ±30kV ESD per IEC61000-4-2 international standard. The low loading capacitance makes the SP3312T ideal for protecting high-speed signal pins.

## Pinout




## Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A ($t_p$=5/50ns)
- Lightning, IEC61000-4-5, 15A ($t_p$=8/20μs)
- Low capacitance of 1.3pF (TYP) per I/O
- Low leakage current of 0.01μA (TYP) at 3.3V
- Low variation in capacitance vs. bias voltage: 0.3pF Typical($V_R$=0 to 2.5V)
- AEC-Q101 qualified

## Functional Block Diagram

## Applications

- 10/100/1000 Ethernet
- Integrated magnetics/ RJ45 connectors
- LAN/WAN Equipment
- Security Cameras
- Industrial Controls
- Notebook & Desktop Computers

Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

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## Absolute Maximum Ratings

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $I_{PP}$ | Peak Current ($t_p$=8/20μs) | 15.0 | A |
| $P_{PK}$ | Peak Pulse Power ($t_p$=8/20μs) | 250 | W |
| $T_{OP}$ | Operating Temperature | -40 to 125 | °C |
| $T_{STOR}$ | Storage Temperature | -55 to 150 | °C |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Thermal Information

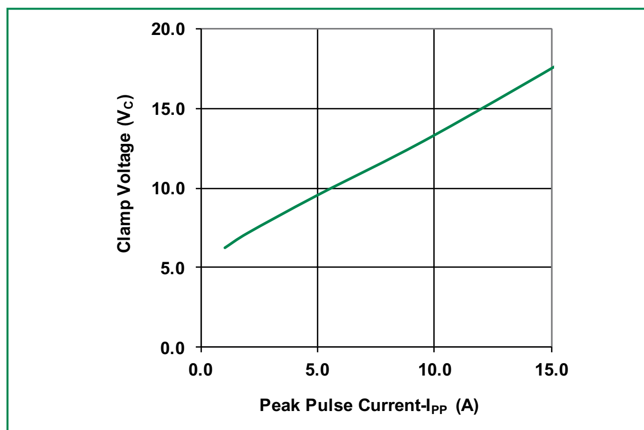
| Parameter | Rating | Units |
|---|---|---|
| Storage Temperature Range | -55 to 150 | °C |
| Maximum Junction Temperature | 150 | °C |
| Maximum Lead Temperature (Soldering 20-40s) | 260 | °C |

## Electrical Characteristics ($T_{OP}$=25°C)

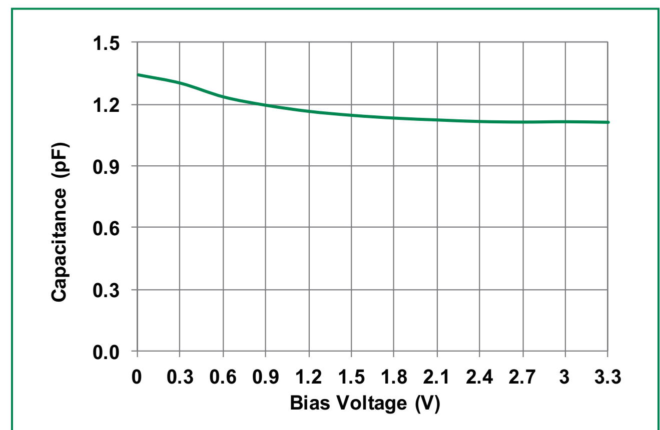
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Reverse Standoff Voltage | $V_{RWM}$ | | | | 3.3 | V |
| Snap Back Voltage | $V_{SB}$ | $I_{SB}$=50mA | 2.8 | | | V |
| Reverse Leakage Current | $I_{LEAK}$ | $V_R$=3.3V, I/O to GND | | 0.01 | 0.05 | μA |
| Clamp Voltage[1] | $V_C$ | $I_{PP}$=1A, $t_p$=8/20μs, Fwd | | 6.0 | | V |
| | | $I_{PP}$=2A, $t_p$=8/20μs, Fwd | | 7.0 | | V |
| | | $I_{PP}$=10A, $t_p$=8/20μs, Fwd | | 13.0 | | V |
| Dynamic Resistance[2] | $R_{DYN}$ | TLP, $t_p$=100ns, I/O to GND | | 0.40 | | Ω |
| ESD Withstand Voltage[1] | $V_{ESD}$ | IEC61000-4-2 (Contact) | ±30 | | | kV |
| | | IEC61000-4-2 (Air) | ±30 | | | kV |
| Variation in Capacitance with Reverse Bias | | Pins 1, 8 to 2, 7 and pins 3, 6 to 4, 5 $V_R$= 0 to 2.5V, f= 1MHz | | 0.3 | | pF |
| Diode Capacitance[1] | $C_{I/O-GND}$ | Reverse Bias=0V | | 1.3 | | pF |

Note:
[1] Parameter is guaranteed by design and/or device characterization.
[2] Transmission Line Pulse (TLP) with 100ns width and 200ps rise time.

## Clamping Voltage vs $I_{PP}$




## Capacitance vs. Reverse Bias

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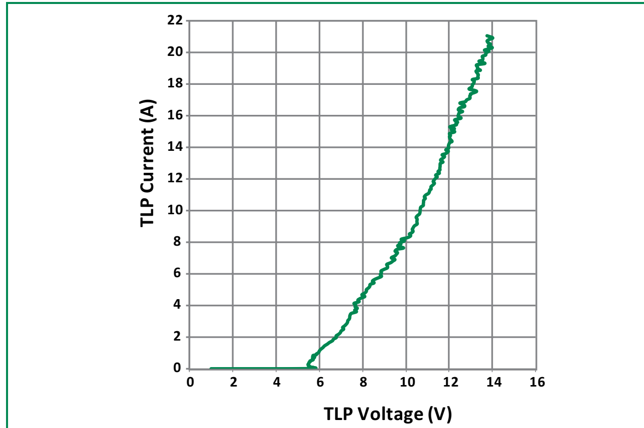
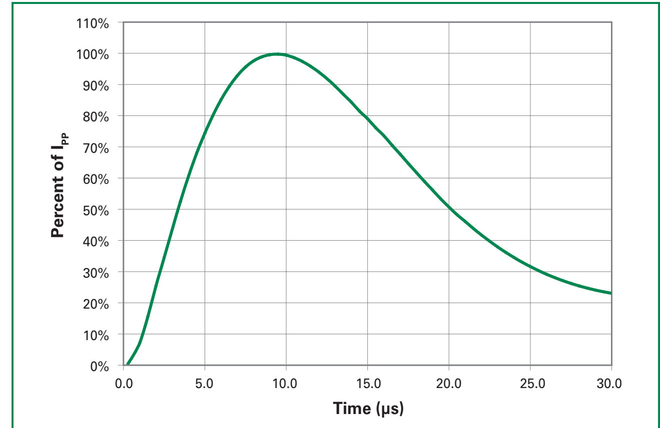
## Transmission Line Pulsing (TLP) Plot

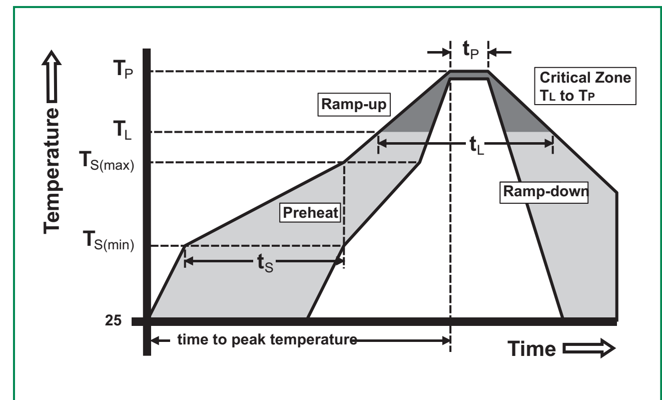



## Pulse Waveform




## Soldering Parameters

| Reflow Condition | | Pb – Free assembly |
|---|---|---|
| Pre Heat | - Temperature Min ($T_{s(min)}$) | 150°C |
| | - Temperature Max ($T_{s(max)}$) | 200°C |
| | - Time (min to max) ($t_s$) | 60 – 180 secs |
| Average ramp up rate (Liquidus) Temp ($T_L$) to peak | | 3°C/second max |
| $T_{S(max)}$ to $T_L$ - Ramp-up Rate | | 3°C/second max |
| Reflow | - Temperature ($T_L$) (Liquidus) | 217°C |
| | - Temperature ($t_L$) | 60 – 150 seconds |
| Peak Temperature ($T_P$) | | $260^{+0/-5}$ °C |
| Time within 5°C of actual peak Temperature ($t_p$) | | 20 – 40 seconds |
| Ramp-down Rate | | 6°C/second max |
| Time 25°C to peak Temperature ($T_P$) | | 8 minutes Max. |
| Do not exceed | | 260°C |




## Product Characteristics

| | |
|---|---|
| **Lead Plating** | Pre-Plated Frame |
| **Lead Material** | Copper Alloy |
| **Lead Coplanarity** | 0.0004 inches (0.102mm) |
| **Substrate material** | Silicon |
| **Body Material** | Molded Epoxy |
| **Flammability** | UL 94 V-0 |

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

## Ordering Information

| Part Number | Package | Marking | Min. Order Qty. |
|---|---|---|---|
| SP3312TUTG | μDFN-08 | 33H | 3000 |

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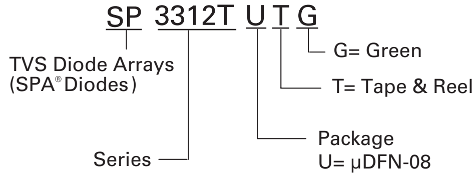
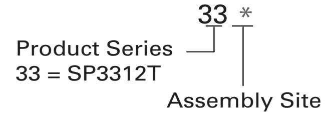
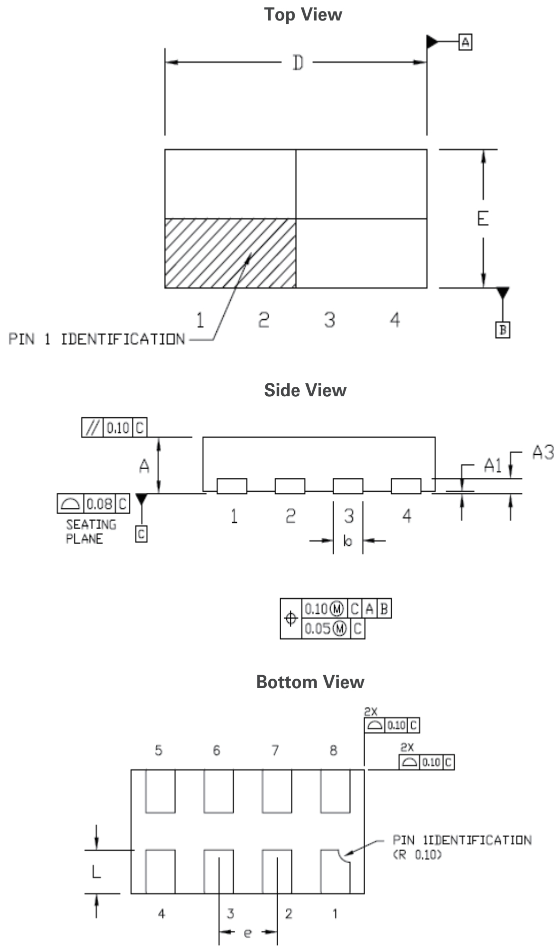
## Part Numbering System




## Part Marking System

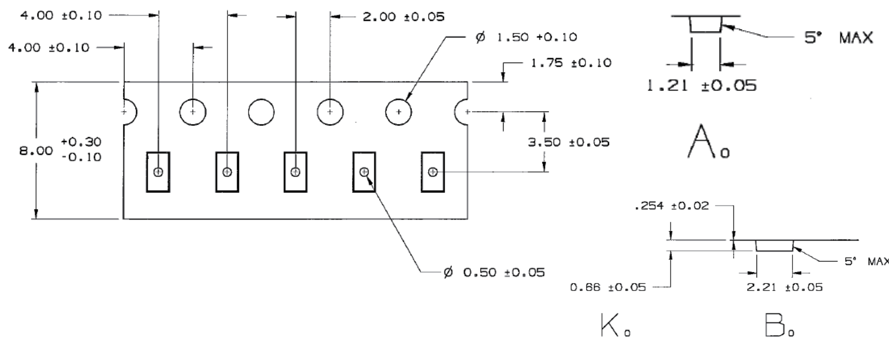



## Package Dimensions — µDFN-08




| Package | µDFN-08 (2.0x1.0mm) | | | | | |
|---|---|---|---|---|---|---|
| JEDEC | MO-229 | | | | | |
| Symbol | Millimeters | | | Inches | | |
| | Min | Nom | Max | Min | Nom | Max |
| **A** | 0.37 | 0.40 | 0.43 | 0.014 | 0.016 | 0.017 |
| **A1** | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| **A3** | 0.127 Ref | | | 0.005 Ref | | |
| **b** | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| **D** | 2.60 | 2.00 | 2.10 | 0.074 | 0.079 | 0.082 |
| **E** | 0.90 | 1.00 | 1.10 | 0.035 | 0.040 | 0.043 |
| **R** | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| **e** | 0.50 BSC | | | 0.020 BSC | | |
| **L** | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

## Embossed Carrier Tape & Reel Specification — µDFN-08

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