User's Guide
SLVUAW9C–September 2016–Revised February 2020

UCD90320 Sequencer and System Health Controller PMBus Command Reference

The UCD90320 Power Supply Sequencer and Monitor supports a wide range of commands that allow an external host to configure, control, and monitor voltage rails and fans. Communication between the sequencer and the host is via an I^2C electrical interface using the PMBus™ command protocol.

The PMBus specification describes the command protocol in general terms. This document describes implementation details that are specific to the UCD90320 Power Supply Sequencer and Monitor. If a command is not described in this document and it is supported by a UCD90320 device (see Table 2), it functions exactly as described in the PMBus specification. In which case, refer to PMBus specification for more details.

See the device-specific data sheet for a complete description of the features.

This document makes reference to "Fusion". The TI Fusion Digital Power Designer (SLVC223) is provided for device configuration. This Microsoft® Windows® based, graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.

Note: This document does not apply to any other UCD90xxx devices

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1 PMBus Specification

This document makes frequent mention of the PMBus specification, specifically, the *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.2. The specification is published by the Power Management Bus Implementers Forum and is available from http://pmbus.org.

The types of status supported by the UCD90320 are shown in Figure 1. Whenever any of these bits are set, the PMBALERT# line is asserted. Unsupported types are denoted with grayed-out text.

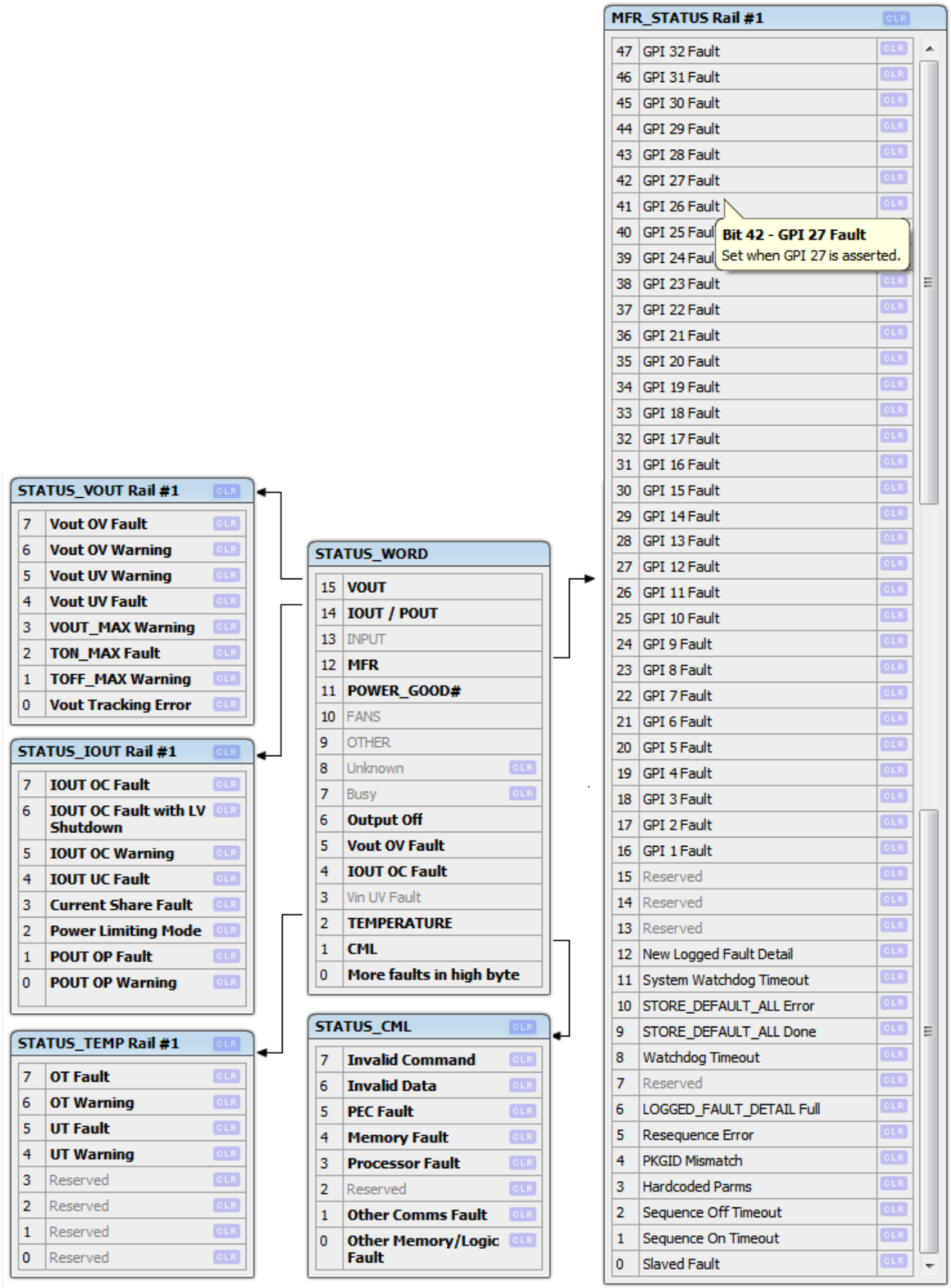

Figure 1. PMBus Status Supported by the UCD90320

1.1 Manufacturer Specific Status (STATUS_MFR_SPECIFIC)

The standard STATUS_MFR_SPECIFIC command does not have enough bits to implement UCD90320's functionalities. This command has been replaced by the MFR_STATUS command (see Section 10.33).

2 Data Formats

Sections 7 and 8 of the PMBus standard provides for five different data formats: three for parameters related to output voltage and two for all other commands. Each PMBus device is expected to support only one of these formats.

2.1 Data Format for Output Voltage Parameters

For parameters related to output voltage, the UCD90320 supports the linear format defined in Section 8.3.1 of the PMBus specification. The linear format uses a 16-bit unsigned mantissa for each parameter, along with an exponent that is shared by all the voltage-related parameters. The exponent is reported in the bottom 5 bits of the VOUT_MODE parameter.

The voltage value is calculated using the equation

$$\text{Voltage} = V \times 2^{X} \quad (1)$$

Where:

Voltage is the parameter of interest, in volts,
V is a 16-bit unsigned binary integer mantissa, and
X is the signed 5-bit twos-complement binary integer exponent from VOUT_MODE.

Exception: The PMBus standard assumes that all output voltages are expressed as positive numbers; therefore, all parameters related to output voltage are unsigned integers, with a few notable exceptions. The VOUT_CAL_OFFSET, and VOUT_CAL_MONITOR values are intended for making fine adjustments to the output voltage and may take on small negative values. As such, these parameters are treated as signed twos-complement binary integers.

2.2 Data Format for Other Parameters

For parameters not directly related to output voltage, the UCD90320 supports the linear data format described in section 7.1 of the PMBus specification. This linear format is a two-byte value that contains an 11-bit, twos-complement mantissa and a 5-bit, twos-complement exponent.

The relationship between the PMBus parameter and the real-world value is given by the formula:

$$R = Y \times 2^{X} \quad (2)$$

Where:

R is the real-world value,
Y is an 11-bit, signed twos-complement binary integer mantissa, and
X is the signed 5-bit, `twos-complement binary integer exponent.

This pseudo floating-point notation allows values as large as ≈33E6 down to ≈15E-6 to be sent over the PMBus. The internal variables used by the UCD90320 firmware are mostly 16 bits wide and do not support such a wide range of values. The resolution of a PMBus setting depends strongly on both the exponent of the PMBus value (larger values have coarser resolution) and the scaling of the internal variables.

2.3 Distinguishing Between Linear Data Formats

The PMBus specification uses the same term, linear, to describe both the 16-bit+exponent format used for the voltage-related parameters as well as the 11-bit+exponent format used for other parameters. In cases where it is necessary to distinguish between these two data formats, this document uses the term LINEAR16 or LINEAR11.

2.4 Translation, Quantization, and Truncation

The internal variables used by the UCD90320 are often scaled to take optimal advantage of the hardware's native units such as ADC or DAC counts rather than volts or amperes. As a result, values that are written and read via PMBus must undergo mathematical translations. These translations, with their inherent quantization, may result in very slight differences between the setting that was written to the UCD90320 and the value that was later read back from it. This is normal and compliant, described in section 7.4 of the PMBus specification.

In some cases, a value written to the device may cause it to exceed the range of its internal variable. In some cases, the device reports this as an error; in other cases it saturates the variable at a safe value. In all cases, the value read back via the PMBus reflects as accurately as possible the internal variable actually being used by the UCD90320.

2.5 8-Bit Time Encoding

To save memory when precision is not needed, several commands will encode a time parameter in 8-bits. The 8 bits are separated into two fields. Bits 6 and 7 are the index for the multiplier field and bits 0 to 5 are the mantissa (0x00 to 0x3F). The two are multiplied together to derive the time. A mantissa of 0 will result in a time of 0 regardless of the multiplier value.

Table 1. 8-Bit Time Encoding

Multiplier Index	Multiplier (ms)	Resulting Range
b'00	1	0 to 63 ms
b'01	8	8 to 504 ms
b'10	64	64 ms to 4.032 s
b'11	512	512 ms to 32.256 s

3 Memory Model

Section 6 of the PMBus specification describes the memory model for PMBus devices. Values used by the PMBus device are loaded into volatile Operating Memory from one or more of the following places:

- Values hard coded into an integrated circuit (IC) design (if any)
- Values programmed from hardware pins (if any)
- A nonvolatile memory called the Default Store
- A nonvolatile memory called the User Store (not supported by the UCD90320)
- Communications from PMBus

The UCD90320 contains RAM that is used as Operating Memory. Embedded Data Flash memory is used to implement the hard-coded values and the Default Store values. Hard-coded values require a new firmware revision. Values in the Default Store may be changed using the STORE_DEFAULT_ALL command described in Section 6.3.

Section 6.1 of the PMBus specification describes the ordering of memory loading and precedence. In general, the hard-coded parameters are loaded into Operating Memory first. Second, any pin-programmable settings take effect. Third, values from the Default Store are loaded. Later, commands issued from the PMBus take effect. In all cases, an operation on a parameter overwrites any prior value that was already in the Operating Memory.

4 Alert Response Address Support

UCD90320 supports using the PMBALERT# line to notify the host of warning or fault conditions, but it does not support the Alert Response Address protocol.

5 Supported PMBus Commands

Table 2 lists the PMBus commands. Commands 00h through CFh are defined in the PMBus specification and are considered to be core commands that are standardized for all manufacturers and products. Commands D0h through FEh are manufacturer specific and may be unique for each manufacturer and product.

The device columns (UCD90120, and so forth) indicate if a command is supported by a given device. The command is supported if a check mark (√) appears in that column. Commands that are not supported by any device are grayed out.

Most commands support writing and reading. Exceptions are indicated in the Comments column.

The Data Format column indicates the format of the data:

Byte	8-bit binary value. See the PMBus specification for details for each command.
LINEAR16	16-bit linear format used for output voltage parameters. Described in Section 2.1.
LINEAR11	11-bit linear format used for parameters other than output voltage. Described in Section 2.2.
n/a	Command does not have a data field.
String	ASCII string. Described in Section 22.2 of the PMBus specification.
Byte Array	A block of data in binary format.

The Scope column indicates how each command is affected by the PAGE setting.

Common	This command does not depend on the PAGE setting. It is a common variable used by all pages.
PAGE	This command applies to the page(s) set by the most recent PAGE command. See Section 6.1 for details.

The Page column in Table 2 points to additional detail about the command. A number that is not in parenthesis corresponds to the page in the *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The number in parenthesis is the page number in this document.

The Data Flash column indicates if the parameter is stored in the Default Store in Data Flash. If an x appears in that column, it is not stored. See Section 6.3 for more information.

Most commands are used for device configuration which is often only done once with the assistance of the TI provided GUI (Fusion). In normal operation, only a subset of the commands are used frequently. Those commands are highlighted in **bold** font.

Table 2. PMBus Commands

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
00	PAGE	R/W Byte	Byte	Common	46 (19)	√	√	√	√	√	√	√	√	x	
01	OPERATION	R/W Byte	Byte	PAGE	49(19)	√	√	√	√	√	√	√	√	x	
02	ON_OFF_CONFIG	R/W Byte	Byte	PAGE	51	√	√	√	√	√	√	√	√		
03	CLEAR_FAULTS	Send Byte	n/a	Common	60	√	√	√	√	√	√	√	√		Write Only
04	PHASE														
05-0F	Reserved														
10	WRITE_PROTECT				43										
11	STORE_DEFAULT_ALL	Send Byte	n/a	Common	43 (20)	√	√	√	√	√	√	√	√		Write Only(1)
12	RESTORE_DEFAULT_ALL	Send Byte	n/a	Common	44 (20)	√									Write Only
13	STORE_DEFAULT_CODE				44										
14	RESTORE_DEFAULT_CODE				44										
15	STORE_USER_ALL				45										
16	RESTORE_USER_ALL				45										
17	STORE_USER_CODE				46										
18	RESTORE_USER_CODE				46										
19	CAPABILITY	Read Byte	Byte	Common	48	√	√	√	√	√	√	√	√		Read Only
1A	QUERY				49										
1B	SMBALERT_MASK	R/W Word	Byte												
1C-1F	Reserved														
20	VOUT_MODE	R/W Byte	Byte	PAGE	24 (21)	√	√	√	√	√	√	√	√		The mode is fixed at 000 (Linear Mode), but the exponent may be modified. See Section 2.1 and Section 6.6 for details.
21	VOUT_COMMAND	R/W Word	LINEAR16 [V]	PAGE	52	√	√	√	√	√	√	√	√		
22	VOUT_TRIM				52										
23	VOUT_CAL_OFFSET				52										
24	VOUT_MAX				53										
25	VOUT_MARGIN_HIGH	R/W Word	LINEAR16 [V]	PAGE	53	√	√	√	√	√	√	√	√		
26	VOUT_MARGIN_LOW	R/W Word	LINEAR16 [V]	PAGE	53	√	√	√	√	√	√	√	√		
27	VOUT_TRANSITION_RATE				53										
28	VOUT_DROOP				54										
29	VOUT_SCALE_LOOP				54										
2A	VOUT_SCALE_MONITOR	R/W Word	LINEAR11 [V/V]	PAGE	54	√	√	√	√	√	√	√	√		
2B-2F	Reserved														

(1) There is a chance that a write to this command will receive a NACK. Once the firmware starts a periodic or commanded update of data flash, it may take up to 100 ms to complete. During that time, writes to these commands will receive a NACK. If this occurs, wait 100 ms and retry the command. This note only applies if the brownout feature is not enabled (see Brownout Enable in MISC_CONFIG).

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
30	COEFFICIENTS				54										
31	POUT_MAX				55										
32	MAX_DUTY				55										
33	FREQUENCY_SWITCH				56										
34	Reserved														
35	VIN_ON				56										
36	VIN_OFF				56										
37	INTERLEAVE				56										
38	IOUT_CAL_GAIN	R/W Word	LINEAR11 [mV/A = mΩ]	PAGE	57 (22)	√	√	√		√	√	√	√		Current sense gain
39	IOUT_CAL_OFFSET	R/W Word	LINEAR11 [A]	PAGE	58	√	√	√		√	√	√	√		
3A	FAN_CONFIG_1_2				58										See FAN_CONFIG command, E8h
3B	**FAN_COMMAND_1**	R/W Word	LINEAR11 [%]	Common	58 ()	√		√			√			x	% Duty cycle (0-100%) RPM Command mode
3C	**FAN_COMMAND_2**	R/W Word	LINEAR11 [%]	Common	60	√		√			√			x	See FAN_COMMAND_1
3D	FAN_CONFIG_3_4				59										See FAN_CONFIG command, E8h
3E	**FAN_COMMAND_3**	R/W Word	LINEAR11 [%]	Common	60	√		√			√			x	See FAN_COMMAND_1
3F	**FAN_COMMAND_4**	R/W Word	LINEAR11 [%]	Common	60	√		√			√			x	See FAN_COMMAND_1
40	VOUT_OV_FAULT_LIMIT	R/W Word	LINEAR16 [V]	PAGE	60	√	√	√	√	√	√	√	√		
41	VOUT_OV_FAULT_RESPONSE	R/W Byte	Byte	PAGE	61 (23)										See FAULT_RESPONSES command
42	VOUT_OV_WARN_LIMIT	R/W Word	LINEAR16 [V]	PAGE	61	√	√	√	√	√	√	√	√		
43	VOUT_UV_WARN_LIMIT	R/W Word	LINEAR16 [V]	PAGE	61	√	√	√	√	√	√	√	√		
44	VOUT_UV_FAULT_LIMIT	R/W Word	LINEAR16 [V]	PAGE	62	√	√	√	√	√	√	√	√		
45	VOUT_UV_FAULT_RESPONSE	R/W Byte	Byte	PAGE	62 (23)										See FAULT_RESPONSES command
46	IOUT_OC_FAULT_LIMIT	R/W Word	LINEAR11 [A]	PAGE	62	√	√	√		√	√	√	√		See (2)
47	IOUT_OC_FAULT_RESPONSE	R/W Byte	Byte	PAGE	62 (23)										See FAULT_RESPONSES command
48	IOUT_OC_LV_FAULT_LIMIT				63										
49	IOUT_OC_LV_FAULT_RESPONSE				63										
4A	IOUT_OC_WARN_LIMIT	R/W Word	LINEAR11 [A]	PAGE	63	√	√	√		√	√	√	√		See (2)
4B	IOUT_UC_FAULT_LIMIT	R/W Word	LINEAR11 [A]	PAGE	63	√	√	√		√	√	√	√		See (2)
4C	IOUT_UC_FAULT_RESPONSE	R/W Byte	Byte	PAGE	64 (23)										See FAULT_RESPONSES command
4D	Reserved														
4E	Reserved														
4F	OT_FAULT_LIMIT	R/W Word	LINEAR11 [°C]	PAGE	64	√	√	√		√	√	√	√		

(2) These values are only applied when associated voltage is in regulation. If there is not an associated voltage monitor, these values are applied after the rail is enabled and after TON_DELAY.

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
50	OT_FAULT_RESPONSE	R/W Byte	Byte	PAGE	64 (23)										See FAULT_RESPONSES command
51	OT_WARN_LIMIT	R/W Word	LINEAR11 [°C]	PAGE	64	√	√	√		√	√	√	√		
52	UT_WARN_LIMIT				64										
53	UT_FAULT_LIMIT				64										
54	UT_FAULT_RESPONSE				64										
55	VIN_OV_FAULT_LIMIT				66										
56	VIN_OV_FAULT_RESPONSE				66										
57	VIN_OV_WARN_LIMIT				66										
58	VIN_UV_WARN_LIMIT				66										
59	VIN_UV_FAULT_LIMIT				67										
5A	VIN_UV_FAULT_RESPONSE				67										
5B	IIN_OC_FAULT_LIMIT				68										
5C	IIN_OC_FAULT_RESPONSE				68										
5D	IIN_OC_WARN_LIMIT				68										
5E	POWER_GOOD_ON	R/W Word	LINEAR16 [V]	PAGE	69	√	√	√	√	√	√	√	√		
5F	POWER_GOOD_OFF	R/W Word	LINEAR16 [V]	PAGE	69	√	√	√	√	√	√	√	√		
60	TON_DELAY	R/W Word	LINEAR11 [ms]	PAGE	70	√	√	√	√	√	√	√	√		This does not apply to retries
61	TON_RISE				70										
62	TON_MAX_FAULT_LIMIT	R/W Word	LINEAR11 [ms]	PAGE	71 (23)	√	√	√	√	√	√	√	√		Maximum time to reach POWER_GOOD_ON
63	TON_MAX_FAULT_RESPONSE	R/W Byte	Byte	PAGE	71 (23)										See FAULT_RESPONSES command
64	TOFF_DELAY	R/W Word	LINEAR11 [ms]	PAGE	71	√	√	√	√	√	√	√	√		
65	TOFF_FALL				71										
66	TOFF_MAX_WARN_LIMIT	R/W Word	LINEAR11 [ms]	PAGE	72	√	√	√	√	√	√	√	√		
67	Reserved														
68	POUT_OP_FAULT_LIMIT				69										
69	POUT_OP_FAULT_RESPONSE				69										
6A	POUT_OP_WARN_LIMIT				70										
6B	PIN_OP_WARN_LIMIT				70										
6C-77	Reserved														
78	**STATUS_BYTE**	Read Byte	Byte	Common	72	√	√	√	√	√	√	√	√	x	Read Only
79	**STATUS_WORD**	Read Word	Word	Common	74	√	√	√	√	√	√	√	√	x	Read Only
7A	**STATUS_VOUT**	Read Byte	Byte	PAGE	75	√	√	√	√	√	√	√	√	x	Read Only
7B	**STATUS_IOUT**	Read Byte	Byte	PAGE	75	√	√	√		√	√	√	√	x	Read Only
7C	STATUS_INPUT				76										
7D	**STATUS_TEMPERATURE**	Read Byte	Byte	PAGE	76	√	√	√		√	√	√	√	x	Read Only

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
7E	**STATUS_CML**	Read Byte	Byte	Common	76	√	√	√	√	√	√	√	√	x	Read Only
7F	STATUS_OTHER				77										
80	STATUS_MFR_SPECIFIC				78										See MFR_STATUS
81	**STATUS_FANS_1_2**	Read Byte	Byte	Common	78 (23)	√		√			√			x	Read Only
82	**STATUS_FANS_3_4**	Read Byte	Byte	Common	79 (23)	√		√			√			x	Read Only
83-87	Reserved														
88	READ_VIN				80										
89	READ_IIN				80										
8A	READ_VCAP				80										
8B	**READ_VOUT**	Read Word	LINEAR16 [V]	PAGE	80	√	√	√	√	√	√	√	√	x	Read Only
8C	**READ_IOUT**	Read Word	LINEAR11 [A]	PAGE	80	√	√	√		√	√	√	√	x	Read Only
8D	**READ_TEMPERATURE_1**	Read Word	LINEAR11 [°C]	Common	80 (24)	√	√	√		√	√	√	√	x	Read Only
8E	**READ_TEMPERATURE_2**	R/W Word	LINEAR11 [°C]	PAGE	80 (24)	√	√	√		√	√	√	√	x	UCD90120 and UCD90124: Read Only
8F	READ_TEMPERATURE_3				80										
90	**READ_FAN_SPEED_1**	Read Word	LINEAR11 [RPM]	Common	81 (25)	√		√			√			x	Read Only (Only valid when the fan is enabled.)
91	**READ_FAN_SPEED_2**	Read Word	LINEAR11 [RPM]	Common	81 (25)	√		√			√			x	Read Only (Only valid when the fan is enabled.)
92	**READ_FAN_SPEED_3**	Read Word	LINEAR11 [RPM]	Common	81 (25)	√		√			√			x	Read Only (Only valid when the fan is enabled.)
93	**READ_FAN_SPEED_4**	Read Word	LINEAR11 [RPM]	Common	81 (25)	√		√			√			x	Read Only (Only valid when the fan is enabled.)
94	READ_DUTY_CYCLE				81										
95	READ_FREQUENCY				81										
96	READ_POUT				81										
97	READ_PIN				81										
98	PMBUS_REVISION	Read Byte	Byte	Common	82	√	√	√	√	√	√	√	√		Read Only
99	MFR_ID	R/W Block (18 bytes)	String	Common	83	√	√	√	√	√	√	√	√		
9A	MFR_MODEL	R/W Block (12 bytes)	String	Common	83	√	√	√	√	√	√	√	√		
9B	MFR_REVISION	R/W Block (12 bytes)	String	Common	83	√	√	√	√	√	√	√	√		
9C	MFR_LOCATION	R/W Block (12 bytes)	String	Common	83	√	√	√	√	√	√	√	√		
9D	MFR_DATE	R/W Block (6 bytes)	String	Common	83	√	√	√	√	√	√	√	√		

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
9E	MFR_SERIAL	R/W Block (12 bytes)	String	Common	83	√	√	√	√	√	√	√	√		
9F	Reserved														
A0	MFR_VIN_MIN				84										
A1	MFR_VIN_MAX				84										
A2	MFR_IIN_MAX				84										
A3	MFR_PIN_MAX				84										
A4	MFR_VOUT_MIN				84										
A5	MFR_VOUT_MAX				84										
A6	MFR_IOUT_MAX				84										
A7	MFR_POUT_MAX				84										
A8	MFR_TAMBIENT_MAX				84										
A9	MFR_TAMBIENT_MIN				84										
AA-AC	Reserved														
AD	IC_DEVICE_ID	Block Read	String	Common	(25)							√	√		PMBus 1.2
AE	IC_DEVICE_REV	Block Read	String	Common	(25)							√	√		PMBuS 1.2
AF	Reserved														
B0-B4	MFR_STATUS_0-MFR_STATUS_4											√	√		Must be used with SMBALERT_MASK (0x1B) to write/read MFR_STATUS SMB alert mask
B5	BLACK_BOX_LOG_FAULT_INFO (USER_DATA_05)	B/W Block	Byte Array	Common								√	√	X	Block Box First Fault log
B6	BLACK_BOX_LOG_RAILS_WARNING (USER_DATA_06)	Block Read	Byte Array	Common								√	√	X	All rails warning when first fault was present
B7	BLACK_BOX_LOG_RAILS_VALUE (USER_DATA_07)	Block Read	Byte Array	Common								√	√	X	All rails value when the first fault was present
B8	RAIL_PROFILE(USER_DATA_08)	Block Read	Byte Array	PAGE	(33)								√		
B9	RAIL_STATE(USER_DATA_09)	Block Read	Byte Array	PAGE	(35)								√		
BA-BF	USER_DATA_05-USER_DATA_0F														
C0-CF	Reserved														
D0	SEQ_TIMEOUT / FAULT_PIN_CONFIG(UCD90240/320) (MFR_SPECIFIC_00)	R/W Word/ R/W Block	LINEAR 11[ms]/ Byte Array	Page/Common	(37)	√						√	√		Must be configured along with GPI_CONFIG which selects the external pin to use for the input source
D1	VOUT_CAL_MONITOR (MFR_SPECIFIC_01)	R/W Word	LINEAR16 [V]	PAGE	(39)	√	√	√	√	√	√	√	√		Offset calibration value for the sensor used in READ_VOUT. Signed.
D2	SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)	R/W Block (4, 6, or 9 bytes)	Byte Array	Common	(39)	√	√	√	√	√	√	√	√		Configures the System Reset function
D3	SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)	R/W Block (4 bytes)	Byte Array	Common	(43)	√	√	√	√	√	√	√	√		Configures the System Watchdog function
D4	SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)	Send Byte	n/a	Common	(45)	√	√	√	√	√	√	√	√		Resets the System Watchdog timeout counter
D5	MONITOR_CONFIG (MFR_SPECIFIC_05)	R/W Block	Byte Array	Common	(45)	√	√	√	√	√	√	√	√		Configure pins for monitoring (voltage, temperature, and so forth)

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
D6	NUM_PAGES (MFR_SPECIFIC_06)	Read Byte	Byte	Common	(48)	√	√	√	√	√	√	√	√		READ-ONLY Returns the number of active pages
D7	RUN_TIME_CLOCK (MFR_SPECIFIC_07)	R/W Block	Byte Array	Common	(49)	√	√	√	√	√	√	√	√		Time in milliseconds and days (4 bytes each)
D8	RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)	R/W Word	LINEAR11 [%]	Common	(49)	√	√	√	√	√	√	√	√		Percent adjustment for calibrating the Run-Time Clock
D9	ROM_MODE (MFR_SPECIFIC_09)	Send Byte	n/a	Common	(50)	√	√	√	√	√	√	√	√		WRITE-ONLY This command sends the device back into ROM mode.
DA	USER_RAM_00 (MFR_SPECIFIC_10)	R/W Byte	Byte	Common	(50)	√	√	√	√	√	√	√	√		RAM value that is set to 0 during device reset. By writing a nonzero value to this variable and then monitoring its value, a host may determine that a device reset has occurred.
DB	SOFT_RESET (MFR_SPECIFIC_11)	Send Byte	n/a	Common	(50)	√	√	√	√	√	√	√	√		WRITE-ONLY This command restarts the controller firmware.
DC	RESET_COUNT (MFR_SPECIFIC_12)	R/W Word [(a)]	2 Bytes[(a)]	Common	(50)	√	√	√	√	√	√	√	√		The number of times that the device has been reset. √
DD	PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)	Read Block (18 bytes)	Byte Array	Common	(51)		√		√	√	√	√	√		Allows encoding on input pins to decide into what state each of the rails should be.
DE	RESEQUENCE (MFR_SPECIFIC_14)	Write Word	2 Bytes	Common	(54)		√	√	√	√	√	√	√	x	Commands selected rails to resequence. (Write Only)
DF	CONSTANTS (MFR_SPECIFIC_15)	Read Block (8 bytes)	Byte Array	Common	(51)	√	√	√	√	√	√	√	√		Fixed information about the device
E0	PWM_SELECT (MFR_SPECIFIC_16)	R/W Byte	Byte	Common	(56)	√	√	√	√	√	√	√	√	x	Determines which PWM the PWM_CONFIG command applies to
E1	PWM_CONFIG (MFR_SPECIFIC_17)	R/W Block (8 bytes)	Byte Array	Common	(56)	√	√	√	√	√	√	√	√		Configures a PWM (frequency, duty cycle, and phase)
E2	PARM_INFO (MFR_SPECIFIC_18)	R/W Block (5 bytes)	Byte Array	Common	(56)	√	√	√	√	√	√	√	√	x	Parm Info <parm base> <parm offset low byte> <parm offset high byte> <parm count> <parm size> This command sets the parameters used by the Parm Value command.
E3	PARM_VALUE (MFR_SPECIFIC_19)	R/W Block	Byte Array	Common	(57)	√	√	√	√	√	√	√	√	x	Value transferred to memory location chosen by the PARM_INFO command
E4	TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)	R/W Word	LINEAR11 [°C/V]	PAGE	(57)	√	√	√		√	√	√	√		Gain calibration for the external sensors used by the READ_TEMPERATURE_2 command
E5	TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)	R/W Word	LINEAR11[°C]	PAGE	(58)	√	√	√		√	√	√	√		Offset calibration for the external sensors used by the READ_TEMPERATURE_2 command
E6	TEMPERATURE_BIAS_PIN (MFR_SPECIFIC_22)														
E7	FAN_CONFIG_INDEX (MFR_SPECIFIC_23)	R/W Byte	Byte	Common	( )	√		√			√			x	Selects to which fan the FAN_CONFIG command applies
E8	FAN_CONFIG (MFR_SPECIFIC_24)	R/W Block (15 Bytes)	Byte Array	Common	( )	√		√			√				Fan configuration – fault detection, auto adjust, and so forth

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
E9	FAULT_RESPONSES (MFR_SPECIFIC_25)	R/W Block (9 Bytes)	Byte Array	PAGE	(58)	√	√	√	√	√	√	√	√		Defines the response to all supported faults
EA	LOGGED_FAULTS (MFR_SPECIFIC_26)	R/W Block	Byte Array	Common	(62)	√	√	√	√	√	√	√	√		Flags in Data Flash that are set when each fault type occurs on each page(1)
EB	LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)	R/W Word	2 bytes	Common	(64)	√	√	√	√	√	√	√	√	x	Number of LOGGED_FAULT_DETAIL entries and a read/write index into those entries
EC	LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)	Read Block	Byte Array	Common	(65)	√	√	√	√	√	√	√	√		Detail information about the faults that have occurred
ED	LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)	R/W Block	Byte Array Byte [°C], LINEAR16 [V], LINEAR11 [amp]	PAGE	(66)	√	√	√	√	√	√	√	√		Peak temperature, voltage, and current for a given page, stored in Data Flash(1)
EE	LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)	R/W Byte	Byte [°C]	Common	(68)	√	√	√		√	√	√	√		Peak internal temperature(1)
EF	LOGGED_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)	R/W Block	Byte Array	Common	(69)	√	√	√	√	√	√	√	√		Selectable fault logging by rail and by fault type
F0	EXECUTE_FLASH (MFR_SPECIFIC_32)	Send Byte	n/a	Common	(70)	√	√	√	√	√	√				If in ROM mode, starts the device executing in FLASH mode. If already in FLASH mode, command has no effect.
F1	SECURITY (MFR_SPECIFIC_33)	R/W Block (6 bytes)	Binary Array	Common	(70)		√		√	√	√	√	√		Sets the password used to secure the unit against unauthorized modification of its settings
F2	SECURITY_BIT_MASK (MFR_SPECIFIC_34)	R/W Block (32 bytes)	Binary Array	Common	(71)		√					√	√		Configures which commands are password protected
F3	MFR_STATUS (MFR_SPECIFIC_35)	Read Block (2 or 4 or 5 bytes)	Byte Array	PAGE	(72)	√	√	√	√	√	√	√	√	x	Replaces the STATUS_MFR_SPECIFIC command
F4	GPI_FAULT_RESPONSES (MFR_SPECIFIC_36)	R/W Block	Byte Array	PAGE	75							√	√		GPI fault responses per page
F5	MARGIN_CONFIG (MFR_SPECIFIC_37)	**UC90240:** R/W Word **All others:** R/W Byte	**UC90240:** R/W Word **All others:** R/W Byte	PAGE	(77)	√	√	√	√	√	√	√	√		Selects the margining pin and other margining configuration
F6	SEQ_CONFIG (MFR_SPECIFIC_38)	R/W Block (6-12 bytes)	Byte Array	PAGE	(78)	√	√	√	√	√	√	√	√		Configures sequencing dependencies and enable pin
F7	GPO_CONFIG_INDEX (MFR_SPECIFIC_39)	R/W Byte	Byte	Common	(84)	√	√	√	√	√	√	√	√	x	Selects to which GPO the GPO_CONFIG command applies. On UCD90240, also selects AND-Path.
F8	GPO_CONFIG (MFR_SPECIFIC_40)	R/W Block (20 or 29 bytes)	Byte Array	Common	(84)	√	√	√	√	√	√	√	√		Configures output pins and their dependencies
F9	GPI_CONFIG (MFR_SPECIFIC_41)	R/W Block (13 bytes)	Byte Array	Common	(100)	√	√	√	√	√	√	√	√		Configures input pins
FA	GPIO_SELECT (MFR_SPECIFIC_42)	R/W Byte	Byte	Common	(104)	√	√	√	√	√	√	√	√	x	Determines to which GPIO the GPIO_CONFIG command applies
FB	GPIO_CONFIG (MFR_SPECIFIC_43)	R/W Byte	Byte	Common	(104)	√	√	√	√	√	√	√	√		Set or get the state of a GPIO
FC	MISC_CONFIG (MFR_SPECIFIC_44)	R/W Block	2 Bytes	Common	(105)	√	√	√	√	√	√	√	√		Miscellaneous configuration settings
FD	DEVICE_ID (MFR_SPECIFIC_45)	Read Block (up to 32 bytes)	String	Common	(104)	√	√	√	√	√	√	√	√		Returns ASCII string with hardware and firmware version information of the controller

Table 2. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	Page	UCD90124	UCD9090	UCD90910	UCD90160	UCD90120A	UCD90124A	UCD90240	UCD90320	Data Flash	Comments
FE	Mfr_Specific_Extended_Command														
FF	PMBUS_Extended_Command														

6 Implementation Details for PMBus Core Commands

The following PMBus core commands are defined in the PMBus specification. This section describes details that are unique to the UCD90320 implementation.

6.1 (00h) PAGE

The PAGE command provides the ability to configure, control, and monitor multiple outputs on one unit using a single PMBus physical address. When the PAGE command is sent, all subsequent commands are applied to settings for the rail selected by the PAGE command.

The Fusion Digital Power Designer software uses the term Rail to refer to a voltage output. Rails are numbered starting with one, whereas pages are numbered starting at zero. The relationship between the PMBus PAGE value and the Rail number is shown in Table 3.

Setting PAGE = 0xFF means that the following write commands are to be applied to all outputs. A page setting of 0xFF is invalid for all read commands, with the exception of the PAGE command.

Table 3. Relationship Between PAGE and Rail

Page	Output Rail
0	1
1	2
2	3
...	...
23(1)	24
24 – 254	Invalid
255 (0xFF)	All

(1) The maximum number of rails on the UCD90320 is 24.

Section 11.10 of the PMBus specification describes the PAGE command in more detail.

6.2 (01h) OPERATION

This command is used to turn outputs on and off along with input from the CONTROL pin. Section 12.1 of the PMBus specification describes this command in more detail.

The UCD90320 supports the following modes for the Operation command:

- Immediate Off (No Sequencing)
- Soft Off (With Sequencing)
- On Nominal (No Margining)
- On Margin High (Ignore Faults)
- On Margin High (Act on Fault)
- On Margin Low (Ignore Faults)
- On Margin Low (Act on Fault)

6.3 (11h) STORE_DEFAULT_ALL

The STORE_DEFAULT_ALL command saves the PMBus parameters from Operating Memory into the Default Store in Data Flash. The UCD90320 uses the most recently written set of Default Store values at startup or after a RESTORE_DEFAULT_ALL command. If the Default Store has never been written, values from the hard-coded memory are used.

NOTE: The device configuration will be corrupted if a power cycle or a reset occurs before this save operation is completed. To ensure a successful save operation, after writing the STORE_DEFAULT_ALL command, wait for the STORE_DEFAULT_ALL_DONE bit to be set (see the MFR_STATUS). Once that bit is set, check the STORE_DEFAULT_ALL_ERROR bit. If the STORE_DEFAULT_ALL_DONE bit is set and the STORE_DEFAULT_ ALL_ERROR is not set, the operation was successful.

NOTE: Monitoring and other tasks (including PMBus communication) are not performed during this save operation which may take up to 100 milliseconds.

6.4 (12h) RESTORE_DEFAULT_ALL

The RESTORE_DEFAULT_ALL command restores the PMBus parameters from the Default Store into Operating Memory. If the Default Store has never been written, values from the hard-coded memory are used

NOTE: Resetting the device is a better (more thorough) way to perform this operation.

6.5 (1Bh) SMBALERT_MASK

This command is added in PMBUS specification 1.2 and is described in section 15.38. It is used to block a status bit(s) from causing the SMBALERT# signal to be asserted. Refer to PMBUS specification document for format details. This command has to be used together with status command codes in order to write or read the mask of a specific status bit. The status command codes that can be used with this command include:

- STATUS_VOUT
- STATUS_IOUT
- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_FANS_1_2
- STATUS_FANS_3_4

Another status command code, MFR_STATUS, also needs to work with the SMBALERT_MASK command. However, SMBALERT_MASK can only write/read one byte mask at a time. Since MFR_STATUS contains 40 bits, it is split into 5 sub-commands to work with the SMBALERT_MASK command:

- MFR_STATUS_0: for MFR_STATUS bit 7 to 0
- MFR_STATUS_1: for MFR_STATUS bit 15 to 8
- MFR_STATUS_2: for MFR_STATUS bit 23 to 16
- MFR_STATUS_3: for MFR_STATUS bit 31 to 24
- MFR_STATUS_4: for MFR_STATUS bit 39 to 32

6.6 (20h) VOUT_MODE

This command, described in Sections 8.1 and 8.2 of the PMBus specification, indicates the data format used for all commands related to output voltage (all LINEAR16 commands). The command includes a 3-bit Mode field and a 5-bit Parameter field. In UCD90320, the Mode field is a read-only and is fixed to 000b(linear data format, described in Section 2.1). The Parameter field is the exponent value and can be modified.

NOTE: This exponent field must be updated before modifying any value that is affected by this setting (all LINEAR16 commands).

Table 4 shows the influence that the exponent value has on the voltage range that can be monitored and the monitoring resolution. For example, to monitor a voltage that is 8 V when enabled, set the exponent to –11.

Table 4. Exponent Influence on Voltage Range and Resolution

Exponent	Range (V)		Resolution (mV)
–7	0	255.99219	7.81250
–8	0	127.99609	3.90625
–9	0	63.99805	1.95313
–10	0	31.99902	0.97656
–11	0	15.99951	0.48828
–12	0	7.99976	0.24414
–13	0	3.99988	0.12207
–14	0	1.99994	0.06104
–15	0	0.99997	0.03052

Given that the actual nominal voltage on the monitor pin will be 1.875 volts (this allows for a 25% overhead). Table 5 shows examples of VOUT_MODE and VOUT_SCALE_MONITOR settings for various monitoring ranges. The voltage in the table is the nominal value for the monitored voltage before being modified with a resistor-divider circuit to fit below the voltage monitoring limit of 2.5 V.

Table 5. Example Settings for Voltage Monitoring Ranges

Exponent	High		Low	
	Voltage	Scale	Voltage	Scale
–7	192	0.009766	96	0.019531
–8	96	0.019531	48	0.039063
–9	48	0.039063	24	0.078125
–10	24	0.078125	12	0.15625
–11	12	0.15625	6	0.3125
–12	6	0.3125	3	0.625
–13	3	0.625	1.5	1.25
–14	1.5	1.25	0.75	2.5
–15	0.75	2.5	0.375	5

6.7 (38h) IOUT_CAL_GAIN

This command, described in section 14.8 of the PMBus specification, is used to configure the gain of the current-sense circuit. The units for this command are milliohms (mV/A).

Note that some ambiguity exists in Rev 1.1 of the PMBus specification. One sentence says that the command uses the *conductance* of the sense resistor, but a later sentence says that the resistance must be used. In one place, the units are listed as ohms, but the default value is declared as 0 milliohms.

Rev 1.0 of the PMBus specification used resistance (not conductance) and milliohms. Rev 1.2 has cleared up this ambiguity and revert to the Rev 1.0 wording. For the UCD90320 devices, the ambiguous language in Rev 1.1 is interpreted to have the same meaning as Rev 1.0 (that is, milliohms).

6.8 (41h – 69h) xxx_FAULT_RESPONSE

The following commands are replaced by the FAULT_RESPONSES command (see Section 10.23).

Table 6. Replaced Fault Response Commands

Code	Command
41h	VOUT_OV_FAULT_RESPONSE
45h	VOUT_UV_FAULT_RESPONSE
47h	IOUT_OC_FAULT_RESPONSE
4Ch	IOUT_UC_FAULT_RESPONSE
50h	OT_FAULT_RESPONSE
63h	TON_MAX_FAULT_RESPONSE

6.9 (62h) TON_MAX_FAULT_LIMIT

This command, described in Section 16.3 of the PMBus specification, states that the "command sets an upper limit, in ms, on how long the unit can attempt to power up the output without reaching the *output undervoltage fault limit*". For the UCD90320, this command will instead "set an upper limit, in ms, on how long the unit can attempt to power up the output without reaching the *POWER_GOOD_ON voltage level*."

For devices other than the UCD90120 and UCD90124: When no voltage monitor pin is assigned to a rail, the sequencer cannot monitor the rail voltage and determine its power-good state. Therefore, after the rail is enabled, it will be given power-good state after a delay time defined by TON_MAX_FAULT_LIMIT.

6.10 (66h) TOFF_MAX_WARN_LIMIT

For devices other than the UCD90120 and UCD90124: When there is no voltage monitor pin assigned to a rail, this time is used to determine when a rail leaves the power-good state after it is disabled. In this case, setting TOFF_MAX_WARN_LIMIT to 0x7FFF (No Limit) will result in no delay between disabling the rail and leaving the power-good state.

6.11 (80h) STATUS_MFR_SPECIFIC

The UCD90320 has replaced the STATUS_MFR_SPECIFIC command with MFR_STATUS (see Section 10.33) in order to support more than eight status bits.

6.12 (81h) STATUS_FAN_1_2 and (82h) STATUS_FAN_3_4

The FAN_n_FAULT bit is set to 1 when the measured fan speed is less than the value set by the "speed fault limit" in the FAN_CONFIG (0xE8) command for 5 consecutive seconds.

Table 7 and Table 8 outline what is supported in these commands.

Table 7. STATUS_FAN_1_2 Support

Bit	Name	Description	Supported
7	FAN_1_FAULT	Fan 1 Fault	Yes
6	FAN_2_FAULT	Fan 2 Fault	Yes
5	FAN_1_WARN	Fan 1 Warning	No
4	FAN_2_WARN	Fan 2 Warning	No
3	SPD_1	Fan 1 Speed Overridden	No
2	SPD_2	Fan 2 Speed Overridden	No
1	AIRFLOW_FAULT	Airflow Fault	No
0	AIRFLOW_WARN	Airflow Warning	No

Table 8. STATUS_FAN_3_4 Support

Bit	Name	Description	Supported
7	FAN_3_FAULT	Fan 3 Fault	Yes
6	FAN_4_FAULT	Fan 4 Fault	Yes

Table 8. STATUS_FAN_3_4 Support (continued)

Bit	Name	Description	Supported
5	FAN_3_WARN	Fan 3 Warning	No
4	FAN_4_WARN	Fan 4 Warning	No
3	SPD_3	Fan 3 Speed Overridden	No
2	SPD_4	Fan 4 Speed Overridden	No
1	AIRFLOW_FAULT	Airflow Fault	No
0	AIRFLOW_WARN	Airflow Warning	No

Note for versions with more than four fans: When more than four fans are supported, the fan fault status are packed in the existing STATUS_FANS_1_2 (1-8) and STATUS_FANS_3_4 (9-16) commands as shown in Table 9 and Table 10 .

Table 9. STATUS_FAN_1_2 Support With More Than Four Fans

Bit	Name	Description
0	FAN_1_FAULT	Fan 1 Fault
1	FAN_2_FAULT	Fan 2 Fault
2	FAN_3_FAULT	Fan 3 Fault
3	FAN_4_FAULT	Fan 4 Fault
4	FAN_5_FAULT	Fan 5 Fault
5	FAN_6_FAULT	Fan 6 Fault
6	FAN_7_FAULT	Fan 7 Fault
7	FAN_8_FAULT	Fan 8 Fault

Table 10. STATUS_FAN_3_4 Support With More Than Four Fans

Bit	Name	Description
0	FAN_9_FAULT	Fan 9 Fault
1	FAN_10_FAULT	Fan 10 Fault
2	FAN_11_FAULT	Fan 11 Fault
3	FAN_12_FAULT	Fan 12 Fault
4	FAN_13_FAULT	Fan 13 Fault
5	FAN_14_FAULT	Fan 14 Fault
6	FAN_15_FAULT	Fan 15 Fault
7	FAN_16_FAULT	Fan 16 Fault

6.13 (8Dh) READ_TEMPERATURE_1

This read-only command returns the temperature from a sensor embedded inside the UCD90320 controller.

6.14 (8Eh) READ_TEMPERATURE_2

This paged command returns the temperature from an external temperature sensor located in or near an output power module.

NOTE: If no temperature monitor pin is assigned to a rail, the internal temperature sensor is used for that rail. See the MONITOR_CONFIG command (Section 10.6).

Devices other than the UCD90120 and UCD90124: If the user writes this command, the written value will be used as the temperature until another value is written by the user, regardless whether or not a temperature monitor pin is assigned to the rail. When a temperature monitor pin is assigned, once READ_TEMPERATURE_2 is written, the temperature monitor pin will not be used again until the device is reset. Similarly, when no temperature monitor pin is assigned, once READ_TEMPERATURE_2 is written, the internal temperature sensor will not be used again until the device is reset.

6.15 (90-93h) FAN_SPEED_1 Through FAN_SPEED_4

The UCD90320 device does not support a fan function.

6.16 (ADh) IC_DEVICE_ID

This command is added in PMBUS1.2. It is used to read the part number of the device.

6.17 (AEh) IC_DEVICE_REV

This command is added in PMBUS1.2. It is used to read the revision of the device.

7 Input and Output Pin Configuration

Each of the input pins (GPI, and so forth) and output pins (Enable, PWM, GPO, and so forth) are configured using one byte. These bits are defined as follows:

Bit	15	14	13	12	11	10	9	8
Purpose						**Polarity** 0 = Active low 1 = Active high	**Mode** 0 = Unused 1 = Input 2 = Actively driven output 3 = Open-drain output	
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Purpose	Table 11UCD9090 Pin ID Definitions							

Bit 11 is miscellaneous bit for the given Pin. Currently this bit is only valid for GPI_CONFIG command. When this bit is set with GPI_CONFIG command, the corresponding pin is behaved as FAULT pin instead of GPI pin. MAX 4 pin could be configured as Fault pin. Device shall NACK if there are more than 4 pins are configured as Fault pin.

Bit 10 sets the pin polarity. This determines when the pin is asserted.

Bits 9:8 set the mode for the pin.

Bits 7:0 select the Pin ID of the desired I/O pin. The pin IDs are numbers from 0 through 84.

This configuration byte is used in several of the following commands, such as SEQ_CONFIG, GPO_CONFIG, GPI_CONFIG, and FAULT_PIN_CONFIG. The command often dictates the Mode of the pin. For example, an Enable can only be an output. It cannot be configured as an input. But, for consistency, this configuration byte format is always used.

WARNING

Pin Usage Conflicts

It is possible to issue commands with pin selections that may conflict with other settings. Because the interactions between settings are so complex and depend on the order in which the PMBus commands are issued, the UCD90320 firmware does not attempt to detect and prevent all possible invalid setting combinations. The Fusion Digital Power Designer GUI provides some additional validity checking, but it is ultimately up to the user to ensure that conflicting GPIO configurations are not selected.

Example: If a command is used to configure a pin for a specific GPIO or sequencing purpose and then issued again with the same pin unassigned, the pin may not revert back to its default usage until after the controller has been reset or power cycled.

Table 11. UCD90320 Pin ID Definitions

Pin Index	UCD90320 Name	PinNum	MARGIN	EN	LGPO	GPI	GPIO
0	MAR01(GPIO)	J13	Y	N	N	Y	Y
1	MAR02(GPIO)	L5	Y	N	N	Y	Y
2	MAR03(GPIO)	D8	Y	N	N	Y	Y
3	MAR04(GPIO)	K6	Y	N	N	Y	Y
4	MAR05(GPIO)	D4	Y	N	N	Y	Y
5	MAR06(GPIO)	E4	Y	N	N	Y	Y
6	MAR07(GPIO)	F5	Y	N	N	Y	Y

Table 11. UCD90320 Pin ID Definitions (continued)

Pin Index	UCD90320 Name	PinNum	MARGIN	EN	LGPO	GPI	GPIO
7	MAR08(GPIO)	N5	Y	N	N	Y	Y
8	MAR09(GPIO)	N6	Y	N	N	Y	Y
9	MAR10(GPIO)	K5	Y	N	N	Y	Y
10	MAR11(GPIO)	M6	Y	N	N	Y	Y
11	MAR12(GPIO)	L6	Y	N	N	Y	Y
12	MAR13(GPIO)	D11	Y	N	N	Y	Y
13	MAR14(GPIO)	C12	Y	N	N	Y	Y
14	MAR15(GPIO)	A13	Y	N	N	Y	Y
15	MAR16(GPIO)	B13	Y	N	N	Y	Y
16	MAR17(GPIO)	D12	Y	N	N	Y	Y
17	MAR18(GPIO)	C13	Y	N	N	Y	Y
18	MAR19(GPIO)	E12	Y	N	N	Y	Y
19	MAR20(GPIO)	E13	Y	N	N	Y	Y
20	MAR21(GPIO)	M13	Y	N	N	Y	Y
21	MAR22(GPIO)	L12	Y	N	N	Y	Y
22	MAR23(GPIO)	M5	Y	N	N	Y	Y
23	MAR24(GPIO)	J12	Y	N	N	Y	Y
24	EN1(GPIO)	M9	N	Y	N	Y	Y
25	EN2(GPIO)	N9	N	Y	N	Y	Y
26	EN3(GPIO)	L10	N	Y	N	Y	Y
27	EN4(GPIO)	K10	N	Y	N	Y	Y
28	EN5(GPIO)	L9	N	Y	N	Y	Y
29	EN6(GPIO)	K9	N	Y	N	Y	Y
30	EN7(GPIO)	N8	N	Y	N	Y	Y
31	EN8(GPIO)	M8	N	Y	N	Y	Y
32	EN9(GPIO)	L8	N	Y	N	Y	Y
33	EN10(GPIO)	K8	N	Y	N	Y	Y
34	EN11(GPIO)	N7	N	Y	N	Y	Y
35	EN12(GPIO)	M7	N	Y	N	Y	Y
36	EN13(GPIO)	K7	N	Y	N	Y	Y
37	EN14(GPIO)	L7	N	Y	N	Y	Y
38	EN15(GPIO)	N4	N	Y	N	Y	Y
39	EN16(GPIO)	N3	N	Y	N	Y	Y
40	EN17(GPIO)	K3	N	Y	N	Y	Y
41	EN18(GPIO)	K4	N	Y	N	Y	Y
42	EN19(GPIO)	J4	N	Y	N	Y	Y
43	EN20(GPIO)	J2	N	Y	N	Y	Y
44	EN21(GPIO)	J3	N	Y	N	Y	Y
45	EN22(GPIO)	H4	N	Y	N	Y	Y
46	EN23(GPIO)	H3	N	Y	N	Y	Y
47	EN24(GPIO)	G4	N	Y	N	Y	Y
48	EN25(GPIO)	F13	N	Y	N	Y	Y
49	EN26(GPIO)	F12	N	Y	N	Y	Y
50	EN27(GPIO)	G11	N	Y	N	Y	Y
51	EN28(GPIO)	H10	N	Y	N	Y	Y
52	EN29(GPIO)	H13	N	Y	N	Y	Y
53	EN30(GPIO)	H12	N	Y	N	Y	Y

Table 11. UCD90320 Pin ID Definitions (continued)

Pin Index	UCD90320 Name	PinNum	MARGIN	EN	LGPO	GPI	GPIO
54	EN31(GPIO)	H11	N	Y	N	Y	Y
55	EN32(GPIO)	L13	N	Y	N	Y	Y
56	LGPO1(GPIO)	C9	N	N	Y	Y	Y
57	LGPO2(GPIO)	B9	N	N	Y	Y	Y
58	LGPO3(GPIO)	A9	N	N	Y	Y	Y
59	LGPO4(GPIO)	C8	N	N	Y	Y	Y
60	LGPO5(GPIO)	D5	N	N	Y	Y	Y
61	LGPO6(GPIO)	C5	N	N	Y	Y	Y
62	LGPO7(GPIO)	C6	N	N	Y	Y	Y
63	LGPO8(GPIO)	C4	N	N	Y	Y	Y
64	LGPO9(GPIO)	L3	N	N	Y	Y	Y
65	LGPO10(GPIO)	M1	N	N	Y	Y	Y
66	LGPO11(GPIO)	M2	N	N	Y	Y	Y
67	LGPO12(GPIO)	M3	N	N	Y	Y	Y
68	LGPO13(GPIO)	L4	N	N	Y	Y	Y
69	LGPO14(GPIO)	N1	N	N	Y	Y	Y
70	LGPO15(GPIO)	M4	N	N	Y	Y	Y
71	LGPO16(GPIO)	N2	N	N	Y	Y	Y
72	DMON1(GPIO)	F4	N	N	N	Y	Y
73	DMON2(GPIO)	F3	N	N	N	Y	Y
74	DMON3(GPIO)	G3	N	N	N	Y	Y
75	DMON4(GPIO)	D10	N	N	N	Y	Y
76	DMON5(GPIO)	L11	N	N	N	Y	Y
77	DMON6(GPIO)	N12	N	N	N	Y	Y
78	DMON7(GPIO)	N11	N	N	N	Y	Y
79	DMON8(GPIO)	M11	N	N	N	Y	Y
80	GPIO1	B11	N	N	N	Y	Y
81	GPIO2	B12	N	N	N	Y	Y
82	GPIO3	C11	N	N	N	Y	Y
83	GPIO4	A12	N	N	N	Y	Y

8 PWM Configuration

The first 24 pins identified in Table 11 can be configured as PWM outputs. The PWM pins can be used to margin a rail (see also Section 10.35), or as a general-purpose PWM (see also Section 10.18)

Table 12 outlines the range of frequencies that can be configured for the various PWMs

Table 12. PWM-Supported Frequencies

PWM Type	Supported Frequencies
PWM	1 kHz to 1 MHz

9 Implementation Details for User Data Commands

9.1 (B5h) BLACK_BOX_FAULT_INFO (USER_DATA_05)

The read/write block common command returns detail information of the first fault.

1. 1. The time that I happened in milliseconds and days
2. Whether or not the fault is page specific
3. The page or GPI that triggered the fault (when applicable)
4. The type of fault.
5. Status of all GPOs when the fault occurred
6. Status of all GPIs when the fault occurred

Clearing the Log: Writing a block whose data bytes are all 0x00 clears BLACK BOX log entries. Nonzero values in any data byte returns a NACK due to Invalid Data. Clearing the black box log will allow to re-log the same GPI fault in both blackbox log and normal fault log.

Table 13. BLACK_BOX_FAULT_INFO Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B5
1	0		BYTE_COUNT =18
2	1	0	**Bit** **Description** 0 paged or non-paged fault 1: first fault log valid(1)/not valid(0) 2: Reserved 7:3 fault_page_num
3	2	1	Days(low byte)
4	3	2	Days(high byte)(1)
5	4	3	Milliseconds(low byte)(2)
6	5	4	Milliseconds(middle Byte)
7	6	5	Milliseconds(middle high byte)
8	7	6	Milliseconds(high byte) **Bit** **Description** 7:3 **Fault Type see Table 52** 2:0 Milliseconds[26:24]
9	8	7	Fault Value(low byte) See Table 52
10	9	8	Fault Value(middle low byte) See Table 52
11	10	9	Fault Value(middle high byte) See Table 52
12	11	10	Fault Value(high byte) See Table 52
13	12	11	**Bit** 0 Not Valid Log(0)/Valid Log(1)(3) 7:1 Reserved bits
14	13	12	GPO status bit mask **Bit** **Description** 7:0 GPO[7-0]

(1) The days is offset from 2000-01-01 00:00:00.00. It is responsible of application to add that time base when retrieving the time stamp.

(2) when this bit is set, only the first 10 byte payload data in the blackbox log(BLACK_BOX_FAULT_INFO) is valid, which describes the simple information of the first fault. GPIs and GPOs in the BLACK_BOX_FAULT_INFO, RAILS_WARNING and RAILS_VALUES may not be valid which is decided by the valid log bit.

(3) when this bit set, whole blackbox log is valid. Application can call RAILS_WARNING and RAILS_VALUE command to retrieve the rest black box log information.

Table 13. BLACK_BOX_FAULT_INFO Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
15	14	13	**Bit** **Description** 7:0 GPO[15-8]
16	15	14	GPI status bit mask (low byte). **Bit** **Description** 7:0 GPI[7-0]
17	16	15	GPI status bit mask (middle byte) **Bit** **Description** 7:0 GPI[15-8]
18	17	16	GPI status bit mask (high byte) **Bit** **Description** 7:0 GPI[23-16]
19	18	17	GPI status bit mask(high byte) **Bit** **Description** 7:0 GPI[31-24]

9.1.1 Fault Info

Table 14. Fault Info Format

Bit(s)	Description
23	Page Specific (1 – yes, 0 – no)
22-17	Fault Type(see Table 52)
16	Reserved
15-0	Days(1)

(1) when this bit is set, only the first 10 byte payload data in the blackbox log(BLACK_BOX_FAULT_INFO) is valid, which describes the simple information of the first fault. GPIs and GPOs in the BLACK_BOX_FAULT_INFO, RAILS_WARNING and RAILS_VALUES may not be valid which is decided by the valid log bit.

9.2 (B6h) BLACK_BOX_FAULT_RAILS_WARNING(USER_DATA_06)

The block read-only common command returns warning status of all rails

Table 15. BLACK_BOX_FAULT_WARNING Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B6
1	0		BYTE_COUNT = 32
2	1	0	Rail 1 warning status **Bit** **Description** 7 Overvoltage warning 6 Undervoltage warning 5 Overcurrent Warning 4-3 Reserved 2 Power-down TOFF_MAX warning 1 Overtemperature warning 0 Reserved
3	2	1	Rail 2 warning status same as Rail1
…	…	…	Rail N warning status same as Rail1

Table 15. BLACK_BOX_FAULT_WARNING Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
33	32	31	Rail 24 warning status same as Rail1

9.3 (B7h) BLACK_BOX_LOG_RAILS_VALUE(USER_DATA_07)

The block read-only paged command returns warning status and monitored values for a given rail.

Table 16. BLACK_BOX_FAULT_WARNING Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B7
1	0		BYTE_COUNT = 7
2	1	0	Warning status (see Table 15)
3	2	1	Monitored voltage value [low byte]
4	3	2	Monitored voltage value [high byte]
5	4	3	Monitored current value [low byte]
6	5	4	Monitored current value [high byte]
7	6	5	Monitored temperature value [low byte]
8	7	6	Monitored temperature value [high byte]

Table 17. Rail N Value

Description	Value Units	Description
Voltage Rail	Voltage	LINEAR16
Current Rail	Current	LINEAR11
Temperature Rail	Temperature	LINEAR11

9.4 (B8h) RAIL_PROFILE(USER_DATA_08)

This R/W Block paged command selects the index of the rail profile that will be used for later VOUT_COMMAND, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARNING_LIMIT, VOUT_MARGIN_HIGH, POWER_GOOD_ON, VOUT_MARGIN_LOW, POWER_GOOD_OFF, VOUT_UV_WARNING_LIMIT and VOUT_UV_FAULT_LIMIT commands. A GPI must assigned to switch the profile based on it asserted/de-asserted state.

Table 18. RAIL_PROFILE Command Format (Write)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B8h
1	0		BYTE_COUNT = 2
2	1	0	Number Profile
3	2	1	Profile Index
			Bit description: 7:4: Read only 3:0: profile index

Table 19. RAIL_PROFILE Command Format (Read)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B8h
1	0		BYTE_COUNT = 2
2	1	0	Number Profile
3	2	1	Profile Index
			Bit description: 7:4: Current profile index used by device 3:0: profile index (set in write command)

9.4.1 Number Profile

In the RAIL_PROFILE write command, number profile is used to perform various operations when combined with profile index, see Table 20.

Table 20. Number Profile (write)

Number Profile	Descriptions	Profile Index
0×00	Access Profile	Profile index to access
0×1-0×4	Total number Profiles for given rail	Profile index to access, it should less than total number profile
0×05-0×FF	Invalid command	Invalid command

When Number profile is set to 0, the profile index parameter is used to set the right profile index for host to access. Device shall NACK this command when the profile index is bigger or equal than total available profile for the given rail.

When number profile is set to 1-4, device shall add or delete profiles properly based on the existing number profile and receiving number profile. If the new number profile is bigger than the existing number profile, device shall add the extra new profiles; otherwise device shall delete the extra profile. If the profile to be deleted is the same one under used, device shall NACK the command. The profile index associated with this command indicates the profile index to be accessed from host. If the profile index associated with the number profile is bigger than or equal the number profile, device shall NACK this command.

Device shall NACK this command if number profile is bigger than 4.

When importing a new project, Application must call this command with correct profile number for the given rail. Otherwise device will use the profile information from the existing rail to process.

In the RAIL_PROFILE read command, number profile returns total number of profiles for the given rail.

9.4.2 Profile Index

Each rail (except GPI rail and rail without voltage monitoring) shall have at least one profile and may have up to 4 profiles with total 50 sharing profile pool. Once all 50 profiles have been allocated, no new profile shall be added and Device shall NACK host. The profile index shall range from 0 to 3.

9.5 (B9h) RAIL_STATE (USER_DATA_09)

The Read Block Paged Command returns the current state of the pages.

Table 21. RAIL_STATE Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B9
1	0		BYTE_COUNT = 1
2	1	0	Rail State(see Table 22)

Table 22. Rail State

RAIL STATE	Value	Description
IDLE	1	On condition is not met, or rail is shut down due to fault, or rail is waiting for the resequence
SEQ_ON	2	Wait the dependency to be met to assert ENABLE signal
START_DELAY	3	TON_DELAY to assert ENABLE signal
RAMP_UP	4	Enable is asserted and rail is on the way to reach power good threshold. If the power good threshold is set to 0 V, the rail stays at this state even if the monitored voltage is bigger than 0 V.
REGULATION	5	Once the monitoring voltage is over POWER_GOOD when enable signal is asserted, rails stay at this state even if the voltage is below POWER_GOOD late as long as there is no fault action taken.
SEQ_OFF	6	Wait the dependency to be met to de-assert ENABLE signal
STOP_DELAY	7	TOFF_DELAY to de-assert ENABLE signal
RAMP_DOWN	8	Enable signal is de-asserted and rail is ramping down. This state is only available if TOFF_MAX_WARN_LIMIT is not set to unlimited; or If the turn off is triggered by a fault action, rail must not be under fault retry to show RAMP DOWN state. Otherwise, IDLE state is present.

10 Implementation Details for Manufacturer-Specific Commands

10.1 (D0h) FAULT_PIN_CONFIG (MFR_SPECIFIC_00)

This Read/Write block common command configures the function of a given fault pin. This command allows pins to be configured as fault-influenced outputs. The state of the output pin is determined by any faults of a selection of rails. (F4h) GPI_FAULT_RESPONSES (MFR_SPECIFIC_36) shall also be called for the given pin to configure the proper response when a fault is detected on the fault bus. However when used TI Fusion GUI, it automatically call these two commands when FAULT_PIN_CONFIG is issued based on the inputs.

Table 23. FAULT_PIN_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D0
1	0		BYTE_COUNT = 33
2	1	0	Page Mask for Fault Pin 0(Byte 0 – LSB)
3	2	1	Page Mask for Fault Pin 0(Byte 1)
4	3	2	Page Mask for Fault Pin 0(Byte 2)
5	4	3	Page_Mask for fault Pin 0(Byte 3 – MSB)
6	5	4	Reserved(must be set to 0)
7	6	5	Reserved(must be set to 0)
8	7	6	Reserved(must be set to 0)
9	8	7	Reserved (must be set to 0)
10	9	8	Page Mask for Fault Pin 1(Byte 0 – LSB)
11	10	9	Page Mask for Fault Pin 1(Byte 1)
12	11	10	Page Mask for Fault Pin 1(Byte 2)
13	12	11	Page Mask for Fault Pin 1(Byte 3 - MSB)
14	13	12	Reserved(must be set to 0)
15	14	13	Reserved (must be set to 0)
16	15	14	Reserved (must be set to 0)
17	16	15	Reserved (must be set to 0)
18	17	16	Page Mask for Fault Pin 2(Byte 0 – LSB)
19	18	17	Page Mask for Fault Pin 2(Byte 1)
20	19	18	Page Mask for Fault Pin 2(Byte 2)
21	20	19	Page Mask for Fault Pin 2(Byte 3 - MSB)
22	21	20	Reserved (must be set to 0)
23	22	21	Reserved (must be set to 0)
24	23	22	Reserved (must be set to 0)
25	24	23	Reserved (must be set to 0)
26	25	24	Page Mask for Fault Pin 3(Byte 0 – LSB)
27	26	25	Page Mask for Fault Pin 3(Byte 1)
28	27	26	Page Mask for Fault Pin 3(Byte 2)
29	28	27	Page Mask for Fault Pin 3(Byte 3 - MSB)
30	29	28	Reserved(must be set to 0)
31	30	29	Reserved(must be set to 0)
32	31	30	Reserved(must be set to 0)
33	32	31	Reserved(must be set to 0)
34	33	32	Other Mask

10.1.1 Fault Pin Configuration

The Fault pin configuration is done by the GPI_CONFIG command; see Section 10.39 for more details. Maximum 4 Fault pins is supported by the device

10.1.2 Page Mask

The Page Mask consists of three configuration bytes. The bits are defined as follows:

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24
Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16
Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

Each selects which pages are to be used in a given fault pin. Setting the bit associated with a given page to 1 enables the associated faults of that page. If the bit associated with a page is set to 0, the faults for page have no effect on the fault pin output.

The following faults have the impact on the fault pin:

RESEQUENCE_ERROR	SEQ_ON_TIMEOUT	SEQ_OFF_TIMEOUT	OT_FAULT	IOUT_OC_FAULT
IOUT_UC_FAULT	VOUT_UV_FAULT	VOUT_OV_FAULT	TON_MAX_FAULT	

10.1.3 Other Mask

This mask determines which fault pin state is influenced by system watchdog fault (see Section 10.4) and resequencer error. Setting the bit associated with a given fault pin to 1 enables that the system watchdog/resequence fault influenced the output of the fault pin. If the bit associated with a fault pin is set to 0, the system watchdog/resequence fault has no effect on the state of the fault pin.

Bit	7	6	5	4	3	2	1	0
Purpose	resequence Error	resequence Error	resequence Error	resequence Error	System Watchdog	System Watchdog	System Watchdog	System Watchdog
	Fault Pin 3	Fault Pin 2	Fault Pin 1	Fault Pin 0	Fault Pin 3	Fault Pin 2	Fault Pin 1	Fault Pin 0

10.2 (D1h) VOUT_CAL_MONITOR (MFR_SPECIFIC_01)

This Read/Write Word paged command is used to apply a fixed offset voltage to the output voltage measured by the device and reported by the READ_VOUT command. It is typically used by the PMBus device manufacturer to calibrate a device in the factory.

The VOUT_CAL_MONITOR has two data bytes formatted as a two's-complement binary integer. The effect on this command depends on the settings of the VOUT_MODE command

10.3 (D2h) SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)

This Read/Write Block common command configures the system reset function. The system reset function allows the device to provide an external reset signal to the system. This signal can be based on time, the power-good state of selected rails, the state of selected GPI pins, or a combination of these things. This ensures that key devices (for example, a CPU) are held in reset until other dependent devices (for example, peripherals) are fully powered. A reset pulse can also be generated as a result of a System Watchdog Timeout.

Table 24. SYSTEM_RESET_CONFIG Command Format

Byte Number (Write)	Byte Number (Read	Payload Index	Description	
0				CMD = D2
1	0			BYTE_COUNT = 15
2	1	0		Page Flags – Byte 0 (LSB)
3	2	1		Page Flags – Byte 1
4	3	2		Page Flags – Byte 2
5	4	3		Page Flags – Byte 3(MSB)
6	5	4		GPI Flags – Byte 0 (LSB)
7	6	5		GPI Flags – Byte 1
8	7	6		GPI Flags – Byte 2
9	8	7		GPI Flags - Byte3 (MSB)
10	9	8		Delay Time
11	10	9		Pulse Time
12	11	10	7:3	GPI Number
			2	De-Assert when Power-Good
			1	Assert when NOT Power-Good
			0	Assert when Watchdog Timeout
13	12	11	7	Enable
			6:5	Reserved
			4	Watchdog Timeout Assertion Uses GPI Tracking Release Delay
			3:0	GPI Tracking Release Delay(100 µs)
14	13	12		GPI Tracking Release Delay (1ms)
15	14	13		Reset Pin Configuration
16	15	14	7:3	Reserved
			2	Polarity for Reset pin
			1:0	Pin mode for Reset Pin

10.3.1 GPI Flags

When “De-assert When Power-Good” is selected, the reset pin is de-asserted after the GPI pins identified by these bits reach the asserted state and then the Delay Time passes. (See Section 10.39)

When “Assert When NOT Power-Good” is selected, the reset pin is immediately asserted whenever the any of the GPI pins identified by these bits leaves the asserted state.

Bit	31	30	29	28	27	26	25	24
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI 27	GPI 26	GPI 25	GPI 24

Bit	23	22	21	20	19	18	17	16
Purpose	GPI 23	GPI 22	GPI 21	GPI 20	GPI 19	GPI 18	GPI 17	GPI 16

Bit	15	14	13	12	11	10	9	8
Purpose	GPI 15	GPI 14	GPI 13	GPI 12	GPI 11	GPI 10	GPI 9	GPI 8

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

10.3.2 Page Flags

When “Assert When NOT Power-Good” is selected, the reset pin is immediately asserted whenever the any of the pages identified by these bits leaves the power-good state.

When “De-assert When Power-Good” is selected, the reset pin is de-asserted after the pages identified by these bits reach the power-good state and then the Delay Time passes.

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24

Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

10.3.3 De-Assert When Power-Good

When this bit is set, the reset pin is de-asserted whenever the pages identified by the Page Flags reach power-good, the GPI pins identified by the GPI Flags are asserted, and then the time identified by the Delay Time expires.

10.3.4 Assert When NOT Power-Good

When this bit is set, the reset pin is immediately asserted whenever any of the pages identified in the Page Flags leaves the power-good state or any of the GPI pins identified by the GPI Flags are de-asserted. Whenever the reset pin is asserted because of the “Assert when NOT Power-Good” function, the device attempts to de-asserted the reset pin based on the Delay Time or a combination of the power-good state of selected rails, the asserted state of selected GPIs, and the Delay Time. The Delay Time must be nonzero when this is the only enabled feature of the system reset function.

10.3.5 Assert When Watchdog Timeout

When this bit is set, a system watchdog timeout causes the reset pin to be asserted for the time identified by the Delay Time.

If the “Watchdog Timeout Assertion Uses GPI Tracking Release Delay” bit is set, the GPI Tracking Release Delay is used instead of the Delay Time.

10.3.6 Delay Time

These bits define how long the reset pin is asserted. This byte is formatted according the 8-bit time encoding defined in *Section 2.5*.

10.3.7 Pulse Time

When this byte is nonzero, the pulse feature is enabled and this byte defines how long the reset pin is de-asserted after the Delay Time has passed. This byte is formatted according the 8-bit time encoding defined in Section 2.5.

10.3.8 GPI Tracking

The GPI Tracking function allows the system reset pin to be more precisely influenced by a specific GPI pin. (The GPI pin may be a reset signal from another device or a push button.) Whenever the GPI de-asserts, the system reset will immediately assert. When the GPI asserts, the system reset will be held asserted for the GPI Tracking Release Delay time. After this delay time, the system reset will be de-asserted. The system reset pin tracks the inverse of the GPI to allow the GPI to be used with the “De-Assert When Power-Good” function.

Table 25. GPI Tracking Configuration

Configuration Parameter	Description
Enable	This bit enables the GPI Tracking function.
GPI Number	These bits identify which one of the GPI pins will be tracked (See Section 10.39).
GPI Tracking Release Delay (100 µs)	These bits are multiplied by 100µs and used as the higher precision portion of the GPI Tracking Delay.
GPI Tracking Release Delay (1 ms)	This byte is formatted according the 8-bit time encoding defined in Section 2.4.

10.3.9 Reset Pin Configuration

This configures the reset pin. See also Section 7.

10.4 (D3h) SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)

This Read/Write Block common command configures the system watchdog function. This function keeps a timeout counter running. That counter is reset when the watchdog input (WDI) pin is toggled or when the SYSTEM_WATCHDOG_RESET command is written. If the counter is not periodically reset within the amount of time identified by the Reset Period byte, the watchdog output (WDO) pin is asserted. The output pin stays asserted until the watchdog input pin is toggled or until the SYSTEM_WATCHDOG_RESET command is written.

Table 26. SYSTEM_WATCHDOG_CONFIG Command Format(1)(2)

Byte Number (Write)	Byte Number (Read	Payload Index	Bit	Description
0				CMD = D3
1	0			BYTE_COUNT = 6
2	1	0	7	Enable
			6	Watch System Reset Pin
			5	Max Fan Speed With Timeout
			4	Disable Until System Reset Release
			3:0	Start Time
3	2	1		Input Pin (WDI) Configuration
			7:0	Pin ID for WDI pin

(1) Each of these pins is optional.
(2) The state of the input pin only gets checked every millisecond. Therefore, the minimum time-between-toggles on the input pin must be no less than two milliseconds.

Table 26. SYSTEM_WATCHDOG_CONFIG Command Format[1][2] (continued)

Byte Number (Write)	Byte Number (Read	Payload Index	Bit	Description
4	3	2		Input Pin (WDI) Configuration
			7:3	Reserved
			2	Polarity for WDI pin
			1:0	Pin mode for WDI Pin
5	4	3		Reset Period
6	5	4		Output Pin (WDO) Configuration
			7:0	Pin ID for WDO pin
7	6	5		Output Pin (WDO) Configuration 7:3: Reserved
			7:3	Reserved
			2	Polarity for WDI pin
			1:0	Pin mode for WDI Pin

10.4.1 Enable

The Enable bit enables the system watchdog function.

10.4.2 Watch System Reset Pin

When the Watch System Reset Pin bit is set, the System Reset pin (see Section 10.3) influences the system watchdog timeout behavior. When the system reset pin is asserted, a watchdog timeout no longer occurs until the reset is de-asserted. Once it is de-asserted, the system watchdog function waits the Start Time before monitoring the Input Pin again.

10.4.3 Max Fan Speed With Timeout

If this bit is set, all fans are set to the maximum speed when a watchdog timeout occurs. The UCD90320 device does not support this feature.

10.4.4 Disable Until System Reset Release

When the Disable Until System Reset Release bit is set, the System Watchdog Reset function is temporarily disabled until the System Reset pin is de-asserted. This temporarily disabled state only applies when the device comes out of reset or when the System Watchdog Reset command is written.

10.4.5 Start Time

The Start Time bits identify the time to delay before monitoring the input pin.

Encoding	Start Time (Seconds)
0000	0
0001	0.1
0010	0.2
0011	0.4
0100	0.8
0101	1.6
0110	3.2
0111	6.4
1000	12.8
1001	25.6
1010	51.2

Encoding	Start Time (Seconds)
1011	102.4
1100	204.8
1101	409.6
1110	819.2
1111	1638.4

10.4.6 Input Pin (WDI) Configuration

This bit configures the input pin (see Section 7).

10.4.7 Reset Period

The system watchdog's timeout counter must be reset within the period of time defined by this byte, else the output pin is asserted. Either of these actions resets the counter:

- Toggle the watchdog Input Pin (WDI)
- Write to the SYSTEM_WATCHDOG_RESET command

All other devices: This byte is formatted according the 8-bit time encoding defined in Section 2.5. The system watchdog does not function as expected when the reset period is set to 0.

Table 27. Reset Period Configuration for UCD90320

Multiplier Index	Multiplier (ms)	Resulting Range
b'00	1	0 to 63 ms
b'01	16	16 to 1008 ms
b'10	256	256 ms to 16.128 s
b'11	4096	4096 ms to 258048 ms

10.4.8 Output Pin (WDO) Configuration

This configures the output pin (see Section 7). This pin is asserted if the system watchdog's timeout counter is not reset within the given time period defined by the Reset Period byte.

10.5 (D4h) SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)

This write-only, Send Byte common command resets the system watchdog's timeout counter. This is the equivalent to toggling the system watchdog Input Pin (WDI).

10.6 (D5h) MONITOR_CONFIG (MFR_SPECIFIC_05)

The read/write block common command configures monitor pins. They can be configured individually for one of the various types of monitoring listed in Table 28. The command format is shown in Table 29. The Monitor Type and Page byte format is shown in Table 30.

The byte position in this command determines which monitor is being configured. The size of the write command is variable. It can be up to the number of monitors supported by the given device (see Table 31). The UCD90320 NACKs the command if the size exceeds this number.

The MONITOR_CONFIG read command always returns information on all of the monitors in a given package. The number of monitors for each device is shown in Table 31.

Table 28. Monitor Types

Monitor Type	Encoding
Not Assigned	0
Voltage	1
Temperature	2

Table 28. Monitor Types (continued)

Monitor Type	Encoding
Current	3
Voltage With Hardware Comparator(1)	RESERVED
Input Voltage	5
Voltage With AVS	6
Input Voltage With AVS	7

(1) *Voltage with Hardware Comparator* type is not available for UCD90320

Voltage Input monitor type is the same as Voltage monitor type, except that it is to monitor input voltage instead of output voltage. When a rail is configured as Voltage input monitor type, the threshold of POWER_GOOD_OFF and VOUT_UV_FAULT_LIMIT shall be set to the same value, otherwise the function may not function as expected. When the monitor voltage of the vin is below POWER_GOOD_OFF(VOUT_UV_FAULT_LIMIT), the function of Voltage Input monitor is to start graceful shutdown which will record Vin UV fault as the reason for shut down in NV memory with time stamp and ignore UV and UC fault log and warning for all associated rails, which is set by the Fault Slave Mask in the SEQ_CONFIG command, see 10.35.9. It is recommended using high number rail as Voltage input monitor. During the graceful shutdown period, other faults from all associated rails are still logged as normal. When the monitor voltage of the VIN is above POWER_GOOD_ON, the graceful shutdown is cancelled.

Voltage with AVS monitor type is the same as voltage monitor type, except that it supports setting the warning and fault limits by a fixed percentage of the nominal voltages.

Due to the fact that the power supply and UCD90320 may not change Vout setpoint simultaneously or with the same slew rate, UCD90320 will take the following steps to avoid false-triggering warn/fault. If the new VOUT setpoint is higher than the current VOUT setpoint, the OV warn/fault thresholds will be immediately set to their respective new levels; other thresholds will increase by 20mV step size in every 500µs until the new levels are reached. If the new VOUT setpoint is lower than the current VOUT setpoint, the UV warn/fault and Power Good On/Off thresholds will be immediately set to their respective new levels; other thresholds will decrease by 20mV step size in every 500µs until the new levels are reached.

Voltage Input with AVS monitor type is the combination of the Voltage input and Voltage with AVS monitor type.

GPI Rail is a new type rail which is defined as using a GPI pin to monitor the status. It does not have all threshold value. It has only two states: 1: asserted or non-asserted. GPI rail support ACTIVE HIGH only. When it is asserted, it is equivalent as power good. When it is de-asserted, it is equivalent as power not good and UV fault. GPI rail does not support margin function. When the Monitor Pin Index is bigger than 24, device automatically treat the page as a GPI rail. GPI rail is very similar to the VOLTAGE MONITOR type rail.

Table 29. MONITOR_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D5
1	0		BYTE_COUNT = N
2	1	0	Monitor 1 Type and Page
3	2	1	Monitor 2 Type and Page
4	3	2	Monitor 3 Type and Page
↓	↓	↓	↓
N+1	N	N	Monitor N Type and Page

Table 30. Monitor Type and Page Byte

Bits	7:5	4:0	
Definition	Monitor Type (see Table 31)	Monitor Page Number	
		UCD90320:	0-31

The status of the monitor pin can be read with the appropriate read command (READ_VOUT, READ_TEMPERATURE_2, READ_IOUT). The state of these monitor pins are also used to capture and report faults and warnings.

The number of monitor pins varies based on the device. UCD90320 has 24 ADC monitors and 8 GPI monitors available. Any attempt to use a monitor number that is not available on a given device (denoted by “Error” in the table) results in a NACK to the MONITOR_CONFIG write command.

Table 31. ADC Monitor Pin Definitions

Index	Pin Name	157-Pin PinNum	Purposes
1	AMON1	E2	MONITOR
2	AMON2	E1	MONITOR
3	AMON3	F2	MONITOR
4	AMON4	F1	MONITOR
5	AMON5	B3	MONITOR
6	AMON6	A3	MONITOR
7	AMON7	B4	MONITOR
8	AMON8	A4	MONITOR
9	AMON9	B5	MONITOR
10	AMON10	A5	MONITOR
11	AMON11	B6	MONITOR
12	AMON12	A6	MONITOR
13	AMON13	C1	MONITOR
14	AMON14	C2	MONITOR
15	AMON15	B1	MONITOR
16	AMON16	B2	MONITOR
17-	AMON17	G2	MONITOR
18	AMON18	G1	MONITOR
19	AMON19	H1	MONITOR
20	AMON20	H2	MONITOR
21	AMON21	B7	MONITOR
22	AMON22	A7	MONITOR
23	AMON23	B8	MONITOR
24	AMON24	A8	MONITOR
25	DMON1	F4	GPI MONITOR
26	DMON2	F3	GPI MONITOR
27	DMON3	G3	GPI MONITOR
28	DMON4	D10	GPI MONITOR
29	DMON5	L11	GPI MONITOR
30	DMON6	N12	GPI MONITOR
31	DMON7	N11	GPI MONITOR
32	DMON8	M11	GPI MONITOR

10.7 (D6h) NUM_PAGES (MFR_SPECIFIC_06)

This read-only, send byte common command returns the number of active pages. This value is determined by the MONITOR_CONFIG and SEQ_CONFIG commands (see Section 10.6 and Section 10.36). It is the higher page number derived from these two evaluations:

- The highest number page that has an enable pin assigned to it. (SEQ_CONFIG)
- The highest number page that has a monitor pin assigned to it. (MONITOR_CONFIG)

10.8 (D7h) RUN_TIME_CLOCK (MFR_SPECIFIC_07)

This command returns the Run-Time Clock value. It is given in milliseconds and days. Both are 32-bit numbers. The Run-Time clock may also be written. This allows the clock to be periodically corrected by the host. It also allows the clock to be initialized to the actual, absolute time in years (for example, March 23, 2010). The user must translate the absolute time to days and milliseconds.

The three usage scenarios for the Run-Time Clock are:

- Time from power-on: the Run-Time Clock starts from 0 each time the device is powered on.
- Local time: an external processor sets the Run-Time Clock to real-world time each time the device is powered-on.
- After power-down, device compares the time stamp from the latest fault log against the one from peak log to see which one is newer as run time clock when power returns.

The Run-Time clock value is used to time-stamp any faults that are logged (see Section 10.26).

Table 32. RUN_TIME_CLOCK Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D7
1	0		BYTE_COUNT = 8
2	1	0	Milliseconds (high byte)
3	2	1	Milliseconds
4	3	2	Milliseconds
5	4	3	Milliseconds (low byte)
6	5	4	Days (high byte)
7	6	5	Days
8	7	6	Days
9	8	7	Days (low byte)

10.9 (D8h) RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)

This read/write word common command has two data bytes formatted in the Linear11 Data format. The units are percent change in how a millisecond is measured. The default value is 0.0%. Typical values are likely to be in the range from –2% to +2%. The command allows values from –100% to +99.9%. If the value returned from the RUN_TIME_CLOCK command (see Section 10.8) is slow, you use a negative percentage of the appropriate amount to correct it. If it is fast, you use a positive percentage. This command is not supported by UCD90320.

10.10 (D9h) ROM_MODE (MFR_SPECIFIC_09)

This Send Byte common command sends the system into ROM mode. Issue this command before attempting to download new firmware to the device. After this command is received, it takes approximately 50 milliseconds for the device to enter ROM mode and become responsive to addition commands.

10.11 (DAh) USER_RAM_00 (MFR_SPECIFIC_10)

This Read/Write Byte common command allows the user to read/write a byte value to RAM in the device. This RAM value is reset to a known value (0) when the controller is reset. By monitoring this value, the user is able to tell that the controller has been reset during operation.

Note that this parameter is not stored to nonvolatile Default Store memory when the STORE_DEFAULT_ALL command is issued.

10.12 (DBh) SOFT_RESET (MFR_SPECIFIC_11)

This Write-Only Send Byte common command restarts the controller firmware. Any active voltage outputs are turned off before the firmware restarts.

10.13 (DCh) RESET_COUNT (MFR_SPECIFIC_12)

This Read/Write Word command allows the user to track how many times the device has been reset. On a device that has not been configured, this value is zero and the number of resets is not tracked. To use this feature, the value must be changed to something other than zero and the device must be reset. After that, this value is incremented each time the device restarted (reset or power-on) and completes the start-up sequence.

If the brownout feature is not enabled (see Brownout Enable in Section 10.42) and this feature is enabled, the data flash will be written to each time the device is restarted. If the brownout feature is enabled, this lowers the number of times that the flash is written.

NOTE: This is a Read/Write byte command. If the reset count exceeds the maximum value (255), it is set to zero and began counting again from there. This rollover occurs 255 times. When the count rolls over the 256th time, the count remains zero and this function is disabled.

10.14 (DDh) PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)

This Read/write Block common command can be used to allow an encoding on 3 input pins to determine the state of all of the rails (the system state). The input pins can then be used to put the system in a low power mode, for example. With each system state, the user will define which rails are on and which rails are off. If a new state is presented on the input pins, and a rail is required to change state, it will do so with regard to its startup or shutdown dependencies – all changes are done with full sequencing functionality.

The OPERATION command is modified when this function causes a rail to change its state. This means that the ON_OFF_CONFIG for a given rail must be set to use the OPERATION command for this function to have any effect on the rail state.

NOTE: Whenever the device is reset, these pins are sampled and the system state, if enabled, is used to update each rail state.

Table 33. Changes to the OPERATION Command

New State	Soft Off Enable	OPERATION Command
On	n/a	0x80
Off	0	0x00
Off	1	0x40

The first 3 pins configured with the GPI_CONFIG command (see Section 10.39) can be used to select 1 of 8 system states.

Table 34. GPI Selection of System States

GPI 2 State	GPI 1 State	GPI 0 State	System State
NOT Asserted	NOT Asserted	NOT Asserted	0
NOT Asserted	NOT Asserted	Asserted	1
NOT Asserted	Asserted	NOT Asserted	2
NOT Asserted	Asserted	Asserted	3
Asserted	NOT Asserted	NOT Asserted	4
Asserted	NOT Asserted	Asserted	5
Asserted	Asserted	NOT Asserted	6
Asserted	Asserted	Asserted	7

CAUTION

When selecting a new System State, changes to the status of the GPI pins must not take longer than 1 microsecond.

Table 35. PIN_SELECTED_RAIL_STATES Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DD
1	0		BYTE_COUNT = 34
2	1	0	System State Enables
3	2	1	Soft Off Enables
4	3	2	System State 0 (Byte 0 – LSB)
5	4	3	System State 0 (Byte 1)
6	5	4	System State 0 (Byte 2)
7	6	5	System State 0 (Byte 3)
8	7	6	System State 1 (Byte 0 – LSB)
9	8	7	System State 1 (Byte 1)
10	9	8	System State 1 (Byte 2)
11	10	9	System State 1 (Byte 3)
12	11	10	System State 2 (Byte 0 – LSB)
13	12	11	System State 2 (Byte 1)
14	13	12	System State 2 (Byte 2)
15	14	13	System State 2 (Byte 3)
16	15	14	System State 3 (Byte 0 – LSB)
17	16	15	System State 3 (Byte 1)
18	17	16	System State 3 (Byte 2)
19	18	17	System State 3 (Byte 3)
20	19	18	System State 4 (Byte 0 – LSB)
21	20	19	System State 4 (Byte 1)
22	21	20	System State 4 (Byte 2)
23	22	21	System State 4 (Byte 3)
24	23	22	System State 5 (Byte 0 – LSB)
25	24	23	System State 5 (Byte 1)
26	25	24	System State 5 (Byte 2)
27	26	25	System State 5 (Byte 3)

Table 35. PIN_SELECTED_RAIL_STATES Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
28	27	26	System State 6 (Byte 0 – LSB)
29	28	27	System State 6 (Byte 1)
30	29	28	System State 6 (Byte 2)
31	30	29	System State 6 (Byte 3)
32	31	30	System State 7 (Byte 0 – LSB)
33	32	31	System State 7 (Byte 1)
34	33	32	System State 7 (Byte 2)
35	34	33	System State 7 (Byte 3)

10.14.1 System State Enables

Each bit in the System State Enables byte is used to enable or disable one of the 8 System States.

Bit	7	6	5	4	3	2	1	0
Purpose	System State 7 Enable	System State 6 Enable	System State 5 Enable	System State 4 Enable	System State 3 Enable	System State 2 Enable	System State 1 Enable	System State 0 Enable

10.14.2 Soft-Off Enables

Each bit in the Soft Off Enables byte determines how to turn off (1-soft off or 0-immediate) any rails commanded to turn off by the associated System State.

Bit	7	6	5	4	3	2	1	0
Purpose	System State 7 Soft-Off Enable	System State 6 Soft-Off Enable	System State 5 Soft-Off Enable	System State 4 Soft-Off Enable	System State 3 Soft-Off Enable	System State 2 Soft-Off Enable	System State 1 Soft-Off Enable	System State 0 Soft-Off Enable

10.14.3 System State[(1)]

The bits in the System State bytes determine if a rail should change states or not (1-on or 0-off).

(1) This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Purpose	PAGE23 ON/OFF	PAGE22 ON/OFF	PAGE21 ON/OFF	PAGE20 ON/OFF	PAGE19 ON/OFF	PAGE18 ON/OFF	PAGE17 ON/OFF	PAGE16 ON/OFF
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Purpose	PAGE15 ON/OFF	PAGE14 ON/OFF	PAGE13 ON/OFF	PAGE12 ON/OFF	PAGE11 ON/OFF	PAGE10 ON/OFF	PAGE9 ON/OFF	PAGE8 ON/OFF
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Purpose	PAGE7 ON/OFF	PAGE6 ON/OFF	PAGE5 ON/OFF	PAGE4 ON/OFF	PAGE3 ON/OFF	PAGE2 ON/OFF	PAGE1 ON/OFF	PAGE0 ON/OFF

10.15 (DEh) RESEQUENCE (MFR_SPECIFIC_14)

This Write block common command is used to command specific rails to resequence. If a rail is commanded to resequence, it will first perform a soft off. After all of the rails that have been commanded to resequence have turned off (the voltage has fallen below POWER_GOOD_OFF), there will be a delay before the rails are commanded to turn back on. The delay is defined by the “Time between Resequences” byte in the MISC_CONFIG command (see Section 10.42). After the delay, the rails will turn on according to any dependencies and/or TON_DELAY.

Table 36. RESEQUENCE Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DF
1	0		BYTE_COUNT = 4
2	1	0	Resequence page mask (byte0 LSB)
3	2	1	Resequence page mask (byte1)
4	3	2	Resequence page mask (byte2)
5	4	3	Resequence page mask (byte3 MSB)

The bits in the three bytes that make up this command determine if a rail should resequence or not (1-yes or 0-no).

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24

Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

This command is not supported by UCD90320.

10.16 (DFh) CONSTANTS (MFR_SPECIFIC_15)

This Read Block common command provides fixed information about the device.

Table 37. CONSTANTS Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DF
1	0		BYTE_COUNT = 8
2	1	0	Maximum Number of Digital Comparators
3	2	1	Maximum Number of General-Purpose Outputs (GPOs)
4	3	2	Maximum Number of General-Purpose Inputs (GPIs)
5	4	3	Maximum Number of Pages
6	5	4	Maximum Number of Fans
7	6	5	Maximum Number of Monitors
8	7	6	Maximum Number of Entries in the Logged Fault Detail (see Section 10.26)
9	8	7	Maximum Number of PWM outputs

Table 38. CONSTANTS for Each Device

Constant	90120	90120A	90124	90124A	9090	90160	90910	90240	90320
Digital Comparators	6	6	6	6	6	6	6	0	0
GPOs	12	12	12	12	10	16	10	12	16
GPIs	8	8	8	8	8	8	8	24	32
Pages	12	12	12	12	10	16	10	24	32
Fans	0	0	4	4	0	0	10	0	0
Monitors	13	13	13	13	11	16	13	24	32
Logged Fault Detail Entries	16	16	10	12	30	18	12	100	100
PWM outputs	12	12	12	12	10	12	12	24	24

10.17 (E0h) PWM_SELECT (MFR_SPECIFIC_16)

This Read/Write Byte common command determines which PWM that the PWM_CONFIG command applies to. The value given here must be a valid Pin ID.

Table 39. Valid PWM Pin IDs

Device	Valid Pin IDs	Details
UCD90320	0-23	See Table 11

10.18 (E1h) PWM_CONFIG (MFR_SPECIFIC_17)

This Read/Write Block common command configures the PWM identified by the PWM_SELECT command. The duty cycle is in LINEAR11 format and valid values are between 0 and 100 (%). Frequency is an unformatted, 32-bit value. See Section 8 for more information about configuring the PWM frequency. The Phase is in LINEAR11 format and valid values are less than 360 (degrees) and greater than or equal to 0. Attempts to write invalid values to this command will result in a NACK. To un-configure a PWM, set the frequency to zero, perform a STORE_DEFAULTS_ALL command, and reset the device.

Table 40. PWM_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E1
1	0		BYTE_COUNT = 8
2	1	0	Duty cycle (high byte)
3	2	1	Duty cycle (low byte)
4	3	2	Frequency (high byte)
5	4	3	Frequency
6	5	4	Frequency
7	6	5	Frequency (low byte)
8	7	6	Reserved
9	8	7	Reserved

10.19 (E2h) PARM_INFO (MFR_SPECIFIC_18)

This Read/Write Block common command is used to configure the parameters used by the PARM_VALUE command.

PARM_INFO and PARM_VALUE are combined to provide a method for reading or writing to any RAM address, hardware register, etc. A map file specific to the firmware release may be required to determine the offset for a particular RAM variable, because variables may be in different locations for each release.

Parm_index – Index for base address

0 = RAM

1 = Hardware Peripherals

2 = Constants in Data Flash (Read Only, unless unlocked)

3 = Constants in Program Flash (Read Only)

4 = Data Flash Control Registers

5 = EEPROM (Read only, with Parm_size = 4 only)

Parm_offset – offset from the base address selected by parm_base.

Parm_count – number of elements to read or write

Parm_size – the size of each element in bytes. (Valid values are 1, 2, or 4).

The PARM_INFO command updates four variables that are needed to issue a generic read/write of RAM, hardware registers, etc. The four variables are parm_index, parm_offset, parm_count, and parm_size and their description follows.

Table 41. PARM_INFO Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E2
1	0		BYTE_COUNT = 6
2	1	0	Index
3	2	1	Offset (low byte)
4	3	2	Offset (middle byte)
5	4	3	Offset (high byte)
6	5	4	Count
7	6	5	Size

10.20 (E3h) PARM_VALUE (MFR_SPECIFIC_19)

This Read/Write Block common command is used to read and write to RAM addresses or hardware peripheral registers. This command assumes that the PARM_INFO command has be previously run to set up the parm_base, parm_offset, parm_count, and parm_size variables as needed.

10.21 (E4h) TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)

This Read/Write Word common command sets the gain calibration for the external sensors used by the READ_TEMPERATURE_2 command. Each external temperature sensor (typically one per power output rail) has its own calibration setting.

This command has two data bytes formatted in the Linear11 Data format. The units are Celsius degrees per Volt.

10.22 (E5h) TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)

This Read/Write Word common command sets the offset calibration for the external sensors used by the READ_TEMPERATURE_2 command. Each external temperature sensor (typically one per power output rail) has its own calibration setting.

This command has two data bytes formatted in the Linear11 Data format. The units are degrees Celsius.

10.23 (E9h) FAULT_RESPONSES (MFR_SPECIFIC_25)

This paged, read/write block command sets the response to each fault condition. This command is used instead of these standard PMBus commands:

- VOUT_OV_FAULT_RESPONSE
- VOUT_UV_FAULT_RESPONSE
- IOUT_OC_FAULT_RESPONSE
- IOUT_UC_FAULT_RESPONSE
- OT_FAULT_RESPONSE
- TON_MAX_FAULT_RESPONSE

As with the original PMBus fault response commands, whenever a fault occurs:

- The corresponding fault bit is the status register is set.
- The PMBus ALERT pin is asserted.
- The fault bit, once set, is cleared only in accordance to Section 10.2.3 in the PMBus specification and not when the fault condition is removed or corrected.

The command format is show in Table 42.

Table 42. FAULT_RESPONSES Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E9
1	0		BYTE_COUNT = 9
2	1	0	VOUT_OV Fault Response
3	2	1	VOUT_UV Fault Response
4	3	2	IOUT_OC Fault Response
5	4	3	IOUT_UC Fault Response
6	5	4	OT Fault Response
7	6	5	TON_MAX Fault Response
8	7	6	Time between retries
9	8	7	Max glitch time for voltage faults
10	9	8	Max glitch time for non-voltage faults

10.23.1 Fault Response Bytes

The Fault Response bytes (the first eight bytes) are formatted as shown in Table 43.

Table 43. Fault Response Byte Format

Bits	Description	Value	Meaning
7	Operation	n/a	When this bit is set to one, the device shuts down (disables the output) and responds according to the retry setting in bits [3:0]. The function associated with the following Glitch Filter bit, may delay or prevent the shutdown.
			When set to zero, the PMBus device continues operation without interruption.
6	Glitch Filter	n/a	When this bit is set to one, the device continues operation for a delay time specified by the “Max glitch time for voltage faults” or the “Max glitch time for non-voltage faults” byte. If the fault condition is removed during the delay time, the timer will reset and the fault will be ignored. If the fault condition is present for longer than the delay time, the device will respond to the fault as programmed in the Retry Setting (bits[3:0]).
5	Soft Stop	n/a	If this bit is set to 1, the rail will come to a soft stop (using TOFF_DELAY). If it is set to 0, the rail shuts down immediately.
4	resequence	n/a	When this bit is set to 1 and the retries have been exhausted, the rail and its Fault Slaves are shutdown in a manner based on the Soft Stop bit. All of those rails are resequenced after a delay time defined by the “Time between Resequences” byte in the MISC_CONFIG command (see Section 10.42)

Table 43. Fault Response Byte Format (continued)

Bits	Description	Value	Meaning
3:0	Retry Setting	0000	A 0 value for the Retry Setting means that the device does not attempt to restart the rail. The rail remains off until a turn-off and then turn-on command (by OPERATION command or CONTROL pin or Pin-Selected State) are received.
		0001–1110[1]	The device attempts to restart the rail for the number of times set by these bits. The minimum number is 1 and the maximum number is 14. If the rail fails to restart successfully within the allowed number of retries, the device disables the rail and remains off unless Resequence bit is set. The rail can be also turned back on according to the conditions described in Section 10.7 of PMBus specification. The time between the start of each restart attempt is set by the ”Time between retries” byte.
		1111	The device attempts to restart the rail continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the rail to shut down.

10.23.2 Resequence

The option to resequence is offered as a response to each type of fault. The resequence operation is not performed until the retries are exhausted for a given fault. During the resequence operation:

- All rails designated as Fault Shutdown Slaves (FSS) of the faulted rail are immediately disabled (Stop Immediately) or disabled according to the configured shutdown sequence (Stop With Delay)
- After the faulted rail and FSS rail enables are de-asserted and all of these rails have turned off (the voltage has fallen below POWER_GOOD_OFF), the UCD90xxx waits for a programmable delay time (for more information, see Section 10.42). While waiting for the rails to turn off, an error is reported if any of the rails reaches its TOFF_MAX_WARN_LIMIT. If this occurs, a configurable option is available to continue with the re-sequencing operation or not; for more information, see Section 10.42. It is also configurable to ignore rail’s POWR_GOOD_OFF and TOFF_WARNING status when resequencing. See Section 10.42. This is mainly for those rails whose EN signals are not controlled by UCD.
- Sequence n Times repeats until the faulted rail and FSS rails successfully achieve regulation or for a user-selected 1, 2, 3, or 4 times; for more information see Section 10.42. If the resequence operation is successful, this resequence counter is reset if all of the rails that where resequenced maintain normal operation (power-good and no retries) for 1 second. (If a rail is identified as one of the group of rails to resequence but the rail was not supposed to be on when the resequence occurs, the device does not wait for that rail to come on before declaring the resequence operation successful.) If the rails are resequenced the maximum number times and they fail to reach normal operation, a device reset is required to reset the resequence counter. Rails can be commanded off and then on in an attempt to get them back to normal operation.
- After the resequence delay time, the faulted rail and FSS rails are sequenced on according to the start-up sequence configuration; for more information see Section 10.42.

This resequence operation is straight-forward if there is only one set of faulted-rail and FSS rails. If two or more occur at the same time, you always get the more conservative behavior. For example, if a set of rails is already on its second resequence, and the device is configured to resequence three times, and another set of rails enters the resequence state, that second set of rails is only resequenced once. Another example – if one set of rails is waiting on all of its rails to shut down so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shut down before re-sequencing.

If the rails at the resequence state are set by the GPI fault response, the entire resequence action is suspended until the GPI fault is physically clear.

10.23.3 Time Between Retries

When configured to do so, this value determines the amount of time that the device waits before it tries to re-enable a rail after it was shut down due to a fault.

This byte is formatted according to Section 2.5. For UCD90320, the minimum value is 1ms.

[1] This retry count is reset whenever the rail stays in regulation for a TON_MAX_FAULT_LIMIT amount of time without having a glitch. (If TON_MAX_FAULT_LIMIT is set to 0, 4 seconds are used for the time.) Glitches on faults where the Operation bit is set to zero are ignored.

10.23.4 Maximum Glitch Time for Voltage Faults

The value in this byte is multiplied by 400 µs to get the “Max glitch time for voltage faults”. This applies to the following faults: VOUT_OV, VOUT_UV

10.23.5 Maximum Glitch Time for Non-Voltage Faults

The value in this byte is multiplied by 100ms to get the “Max glitch time for non-voltage faults”. This applies to the following faults: IOUT_OC, IOUT_UC, OT

10.24 (EAh) LOGGED_FAULTS (MFR_SPECIFIC_26)

This read/write block common command reports a history of all faults that have ever been reported and logged into nonvolatile memory.

Clearing the Log: Writing a block whose data bytes are all 0x00 resets all logged entries to 0. This also clears the LOGGED_FAULT_DETAIL entries (see Section 10.26). Nonzero values in any data byte returns a NACK due to Invalid Data.

10.24.1 Command Format

This command returns a binary array in the order shown in Table 44. The command sends information for all pages, even when some pages are not active. Log entries for inactive pages are reported as 0x00.

Table 44. LOGGED_FAULTS Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 37
2	1	0	Non-Paged Faults
3	2	1	GPI Faults (Byte 0 – LSB)
4	3	2	GPI Faults (Byte 1)
5	4	3	GPI Faults (Byte 2)
6	5	4	GPI Faults (Byte 3 - MSB)
7	6	5	Page 0 Faults
		. . .	Page 1 Faults
37	36	35	. . .
38	37	36	Page 31 Faults

10.24.2 Non-Paged Faults

The bit definitions for common faults are shown in Table 45.

By examining this single bit (bit 0 of the Non-Paged Faults byte), a host can determine if any page-dependent, GPI, or fan faults have occurred. A value of 0 in this bit indicates that all of the page-dependent, GPI, and fan fault log entries are 0 and need not be read. A value of 1 in this bit indicates that one or more of the page-dependent, GPI, or fan faults have occurred. In that case, the host must examine all of the log entries to determine which ones have log information.

Table 45. Non-Paged Fault Log Bit Definitions

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	LOG_NOT_EMPTY	No
1	System Watchdog Timeout	Yes
2	resequence Error	No
3	Watchdog Timeout	Yes
4	Reserved	No

Table 45. Non-Paged Fault Log Bit Definitions (continued)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
5	Reserved	No
6	Reserved	No
7	Reserved	No

10.24.3 GPI Faults

The bit definitions for GPI faults are shown inTable 46. These bits are set whenever the associated GPI is de-asserted.

Table 46. GPI Fault Log Bit Definitions

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
		Byte 0 (LSB)
0	GPI_0	Yes
1	GPI_1	Yes
2	GPI_2	Yes
3	GPI_3	Yes
4	GPI_4	Yes
5	GPI_5	Yes
6	GPI_6	Yes
7	GPI_7	Yes
		Byte 1
0	GPI_8	Yes
1	GPI_9	Yes
2	GPI_10	Yes
3	GPI_11	Yes
4	GPI_12	Yes
5	GPI_13	Yes
6	GPI_14	Yes
7	GPI_15	Yes
		Byte 2
0	GPI_16	Yes
1	GPI_17	Yes
2	GPI_18	Yes
3	GPI_19	Yes
4	GPI_20	Yes
5	GPI_21	Yes
6	GPI_22	Yes
7	GPI_23	Yes
		Byte 3
0	GPI_24	Yes
1	GPI_25	Yes
2	GPI_26	Yes
3	GPI_27	Yes
4	GPI_28	Yes
5	GPI_29	Yes
6	GPI_30	Yes

Table 46. GPI Fault Log Bit Definitions (continued)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
7	GPI_31	Yes

10.24.4 Page-Dependent Faults

The bit definitions for page-dependent faults are shown in Table 47.

Table 47. Page-Dependent Fault Log Bit Definitions

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	VOUT_OV Fault	Yes
1	VOUT_UV Fault	Yes
2	TON_MAX Fault	Yes
3	IOUT_OC Fault	Yes
4	IOUT_UC Fault	Yes
5	TEMPERATURE_OT Fault	Yes
6	Sequence On Timeout	Yes
7	Sequence Off Timeout	Yes

10.25 (EBh) LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)

The read form of this command reports the total number of LOGGED_FAULT_DETAIL entries and the current value of the index into those entries (see Section 10.26). The Fault Index byte can be written.

Table 48. LOGGED_FAULT_DETAIL_INDEX Command Format

Byte Number	Description
1	Fault Index(R/W)
2	Total Number of LOGGED_FAULT_DETAIL entries (Read Only))

10.26 (ECh) LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)

This read-only block common command returns detail information about a given fault:

- The time that it happened in milliseconds (0 to 86400000) and days (0 to 1048575)
- Whether or not the fault is page specific
- The page that the fault occurred on (when applicable)
- The type of fault (see Section 10.24)

Table 49. LOGGED_FAULT_DETAIL Command Format

Byte Number (Read)	Payload Index	Description
		CMD = EC
0		BYTE_COUNT = 12
1	0	Page number + Milliseconds (high byte)(1)
2	1	Milliseconds
3	2	Milliseconds
4	3	Milliseconds (low byte)
5	4	Fault ID + Days (high byte)
6	5	Fault ID + Days
7	6	Fault ID + Days
8	7	Fault ID + Days (low byte)
9	8	Fault Value (low byte)
10	9	Fault Value (middle byte)
11	10	Fault Value (middle high byte)(2)
12	11	Fault Value (high byte)(2)

(1) Page number is at bits 31:27 and Milliseconds is at bit 26:0.
(2) This byte is valid only if the current fault type is either Sequence On Timeout or Sequence Off Timeout.

New LOGGED_FAULT_DETAIL entries for a given fault are logged once and then not logged again until one of the following events occurs[2]:

- Firmware is restarted
- The rail stays in regulation for the amount of time determined by TON_MAX_FAULT_LIMIT. If TON_MAX_FAULT_LIMIT is set to 0, 4 seconds are used for the time.
- The rail is turned off and then turned back on. (1)
- The CLEAR_FAULTS command is written
- The LOGGED_FAULTS command is written

(1) This applies to paged faults only.

(2) Everything GPI state is changed to de-asserted, a GPI fault is logged.

The maximum number of entries per device is show in Table 50. Once the maximum entries have been logged, no more detail is logged until the fault log is cleared (see Section 10.24). Unless, the “Enable Log FIFO” bit in the MISC_CONFIG command is set (see Table 69).

Table 50. Number of Log Entries in Each Device Type

Device	Entries
UCD90120	16
UCD90120A	16
UCD90124	10
UCD90124A	12
UCD9090	30
UCD90910	12
UCD90160	18
UCD90240	100
UCD90320	100

The Days field is a 32-bit value where the top bits are used to encode other information as shown in Table 51.

Table 51. Fault Identification + Days

Bits(s)	Description
31	Page Specific (1 – yes, 0 – no)
30–27	Fault Type
26–11	Days[1]
10-0	Reserved

(1) The days is offset from 2000-01-01 00:00:00.00. It is responsible of application to add the that time base when retrieving the time stamp.

Information on the Fault Value (units and formatting) is shown in Table 52.

Table 52. Fault Value

Fault Type Number	Paged?	Description	Fault Value Units	Data Format
0	No	Reserved		
1	No	System Watchdog Timeout	Not Valid	n/a
2	No	Resequence Error	Not Valid	n/a
3	No	Watchdog Timeout	Not Valid	n/a
4	No	Reserved		
5	No	Reserved		
6	No	Reserved		
7	No	Reserved		
8	No	Fan Fault[1]	RPM	LINEAR11
9	No	GPI Fault[1]	Not Valid	n/a
0	Yes	VOUT_OV Fault	Voltage	LINEAR16
1	Yes	VOUT_UV Fault	Voltage	LINEAR16
2	Yes	TON_MAX Fault	Voltage	LINEAR16
3	Yes	IOUT_OC Fault	Current	LINEAR11
4	Yes	IOUT_UC Fault	Current	LINEAR11
5	Yes	TEMPERATURE_OT Fault	Temperature	LINEAR11
6	Yes	Sequence On Timeout	N/A	Bit Mask[2][3]
7	Yes	Sequence Off Timeout	N/A	Bit Mask[2][3]

(1) The Page Number is used to encode which Fan or GPI that the fault information applies to.

(2) Any bit set to 1 corresponds to a page dependency that is not met. The GPI dependencies that are not met are OR'ed into the top 8 bits. So, for example, if page dependencies 2 and 5 are not met and GPI W (bit 4) dependency is not met, the fault value is 0x1024.

(3) Any bit set to 1 corresponds to a page dependency that is not met. The GPI dependencies that are not met are OR'ed into the all 24 bits. So, for example, if page dependencies 2 and 5 are not met and GPI W (bit 4) dependency is not met, the fault value is 0x000034

10.27 (EDh) LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)

This Read/Write Block paged command returns the maximum temperatures, voltages, and currents seen during operation for a given page. Provisions exist to reset this nonvolatile logged information.

This command returns a binary array in the order shown in Table 53. Each temperature is one unsigned byte that contains the temperature in degrees C. Each voltage is two bytes in LINEAR16 format. Each current is two bytes in LINEAR11 format.

The temperature is from the external temperature sensor associated with this page and is the same one reported by the READ_TEMPERATURE_2 command.

Table 53. LOGGED_PAGE_PEAKS Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = ED
1	0		BYTE_COUNT = 5(1)
2	1	0	Temperature(1)(2)
3	2	1	Voltage (low byte)
4	3	2	Voltage (high byte)
5	4	3	Current (low byte)(1)(3)
6	5	4	Current (high byte)(1)(3)

(1) the byte count varies up on the device monitoring feature, see (2) and (3) the following.
(2) This byte is only available if device support temperature monitoring.
(3) These two bytes are only available if device support current monitoring.

Clearing the Log: Writing a block whose data bytes are all 0x00 resets all logged entries to 0. Nonzero values in any data byte return a NACK due to Invalid Data. The peaks can be cleared for all pages by setting the PAGE command to 0xFF.

NOTE: The log must be cleared before the device begins normal operation.

Flash Memory Management: To reduce unnecessary stress on the Flash memory, the peak values are stored in volatile RAM memory and only written to flash memory under certain conditions:

I. If at least one temperature, voltage, or current value exceeds its previously logged maximum value a 30-second timer is started. At the end of this timer interval, the values are copied from RAM to flash memory. During a transient event, the peak value may reach several new maximums in rapid succession; the 30-second timer combines them together for a single write operation.

II. If a new fault is recorded in the fault log (see Section 10.24), both the peak log and the fault log are written to Flash.

10.28 (EEh) LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)

This Read/Write Byte common command returns the maximum internal temperature in degrees Celsius. Provisions exist to reset this nonvolatile logged information. The internal temperature sensor reading is the same one reported by the READ_TEMPERATURE_1 command.

Clearing the Log: Writing a value of 0x00 resets the log. Non-zero values return a NACK due to Invalid Data.

10.29 (EFh) LOGGED_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)

This Read/Write Block command selects what fault detail (see Section 10.25) is logging by rail and by fault type. The command, the bytes in the command, and the bits in those bytes are formatted the same as the LOGGED_FAULTS command (see Section 10.24). For this LOGGED_FAULT_DETAIL_ENABLES command, the bits select if a fault is logged (1) or not (0).

Table 54. LOGGED_FAULT_DETAIL_ENABLES Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EF
1	0		BYTE_COUNT = 37
2	1	0	Non-paged Enable Flags
3	2	1	GPI Enable Flags - Byte 0 (LSB)
4	3	2	GPI Enable Flags - Byte 1
5	4	3	GPI Enable Flags - Byte 2

Table 54. LOGGED_FAULT_DETAIL_ENABLES Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
6	5	4	GPI Enable Flags - Byte 3 (MSB)
7	6	5	Page Enable Flags – Page 0
8	7	6	Page Enable Flags – Page 1
9	8	7	Page Enable Flags – Page 2
10	9	8	Page Enable Flags – Page 3
11	10	9	Page Enable Flags – Page 4
12	11	10	Page Enable Flags – Page 5
13	12	11	Page Enable Flags – Page 6
14	13	12	Page Enable Flags – Page 7
15	14	13	Page Enable Flags – Page 8
16	15	14	Page Enable Flags – Page 9
17	16	15	Page Enable Flags – Page 10
18	17	16	Page Enable Flags – Page 11
19	18	17	Page Enable Flags – Page 12
20	19	18	Page Enable Flags – Page 13
21	20	19	Page Enable Flags – Page 14
22	21	20	Page Enable Flags – Page 15
23	22	21	Page Enable Flags – Page 16
24	23	22	Page Enable Flags – Page 17
25	24	23	Page Enable Flags – Page 18
26	25	24	Page Enable Flags – Page 19
27	26	25	Page Enable Flags – Page 20
28	27	26	Page Enable Flags – Page 21
29	28	27	Page Enable Flags – Page 22
30	29	28	Page Enable Flags – Page 23
...	...	...	
38	37	36	Page Enable Flags – Page 31

10.30 (F0h) EXECUTE_FLASH (MFR_SPECIFIC_32)

If the device is in ROM mode, this command starts the device executing in FLASH mode. If the device is already in FLASH mode, the command has no effect. This command is not supported by UCD90320.

10.31 (F1h) SECURITY (MFR_SPECIFIC_33)

This Read/Write Block common command allows certain commands to be write-protected. The data for this command is a 6-byte binary string containing the password. The password is stored in nonvolatile memory, and is used to secure the unit against unauthorized modification of its settings.

While security is turned on, attempting to write to a protected command while security is on results in a NACK. There is an exception for protected “Send Byte” commands. They do not return a NACK, but they are ignored.

These are the only commands that can be written when security is enabled:

```
CLEAR_FAULTS
GPIO_SELECT
GPO_CONFIG_INDEX
LOGGED_FAULT_DETAIL_INDEX
OPERATION
PAGE
PARM_INFO
```

```
PWM_SELECT
READ_TEMPERATURE_2
RESEQUENCE
RUN_TIME_CLOCK
SECURITY
STORE_DEFAULT_ALL
SYSTEM_WATCHDOG_RESET
USER_RAM_00
```

10.31.1 Enabling Security

When security has not yet been enabled or has been disabled, writing this command sets the new password. After the password is set to any value other than [0xFF FF FF FF FF FF], security is enabled. After security has been enabled, a STORE_DEFAULT_ALL command must be issued to restore the security setting after the device is reset.

10.31.2 Disabling Security

Any time security is enabled, it can be temporarily disabled by writing the password to this command. It can be permanently disabled by first disabling security, then setting the password to [0xFF FF FF FF FF FF], and then issuing a STORE_DEFAULT_ALL command.

If the sent password does not match the stored password, the write command is NACKed. Additional attempts to write this command are NACKed until the device is reset. This prevents an attacker from merely sending the command repeatedly with all possible passwords.

This command is not supported by UCD90320.

10.31.3 Reading This Command

For security reasons, reading this value does not return the actual password. The response code depends on the present security setting.

Read Response Code	Meaning
0x00 00 00 00 00 00	Security is turned off.
0x00 00 00 00 00 01	Security is turned on.
0x00 00 00 00 00 02	This command is locked due to incorrect password entry.

A PMBus host does not need to validate the entire 6-byte response code. Only the last byte is significant to determining the security status: 0x00 (security off), 0x01 (security on), 0x02 (Invalid password).

10.32 (F2h) SECURITY_BIT_MASK (MFR_SPECIFIC_34)

This command is not supported by the UCD90320 device.

10.33 (F3h) MFR_STATUS (MFR_SPECIFIC_35)

This is a R/W block common command. The Manufacturer Status bits are defined in Table 55. With the exception of the STORE_DEFAULT_ALL_DONE bit, whenever any of these bits are set, the PMBALERT# line is asserted.

Table 55. Manufacturer Specific Status

Byte Number (write)	Byte Number (Read)	Payload Index	Bit in Each Payload Byte	Name	Descriptions
0					CMD = F3
1	0				BYTE_COUNT = 6
2	1	0	0	GPI25 Fault	Set whenever the GPI is de-asserted.
2	1	0	1	GPI26 Fault	See GPI25, bit 0 byte 0
2	1	0	2	GPI27 Fault	See GPI25, bit 0 byte 0

Table 55. Manufacturer Specific Status (continued)

Byte Number (write)	Byte Number (Read)	Payload Index	Bit in Each Payload Byte	Name	Descriptions
2	1	0	3	GPI28 Fault	See GPI25, bit 0 byte 0
2	1	0	4	GPI29 Fault	See GPI25, bit 0 byte 0
2	1	0	5	GPI30 Fault	See GPI25, bit 0 byte 0
2	1	0	6	GPI31 Fault	See GPI25, bit 0 byte 0
2	1	0	7	GPI32 Fault	See GPI25, bit 0 byte 0
3	2	1	0	GPI17 Fault	See GPI25, bit 0 byte 0
3	2	1	1	GPI18 Fault	See GPI25, bit 0 byte 0
3	2	1	2	GPI19 Fault	See GPI25, bit 0 byte 0
3	2	1	3	GPI20 Fault	See GPI25, bit 0 byte 0
3	2	1	4	GPI21 Fault	See GPI25, bit 0 byte 0
3	2	1	5	GPI22 Fault	See GPI25, bit 0 byte 0
3	2	1	6	GPI23 Fault	See GPI25, bit 0 byte 0
3	2	1	7	GPI24 Fault	See GPI25, bit 0 byte 0
4	3	2	0	GPI9 Fault	See GPI25, bit 0 byte 0
4	3	2	1	GPI10 Fault	See GPI25, bit 0 byte 0
4	3	2	2	GPI11 Fault	See GPI25, bit 0 byte 0
4	3	2	3	GPI12 Fault	See GPI25, bit 0 byte 0
4	3	2	4	GPI13 Fault	See GPI25, bit 0 byte 0
4	3	2	5	GPI14 Fault	See GPI25, bit 0 byte 0
4	3	2	6	GPI15 Fault	See GPI25, bit 0 byte 0
4	3	2	7	GPI16 Fault	See GPI25, bit 0 byte 0
5	4	3	0	GPI1 Fault	See GPI25, bit 0 byte 0
5	4	3	1	GPI2 Fault	See GPI25, bit 0 byte 0
5	4	3	2	GPI3 Fault	See GPI25, bit 0 byte 0
5	4	3	3	GPI4 Fault	See GPI25, bit 0 byte 0
5	4	3	4	GPI5 Fault	See GPI25, bit 0 byte 0
5	4	3	5	GPI6 Fault	See GPI25, bit 0 byte 0
5	4	3	6	GPI7 Fault	See GPI25, bit 0 byte 0
5	4	3	7	GPI8 Fault	See GPI25, bit 0 byte 0
6	5	4	0	WATCHDOG_TIMEOUT	A UCD90320 internal watchdog timeout reset has occurred
6	5	4	1	STORE_DEFAULT_ALL_DONE	The STORE_DEFAULT_ALL operation has completed
6	5	4	2	STORE_DEFAULT_ALL_ERROR	An error occurred during STORE_DEFAULT_ALL
6	5	4	3	SYSTEM_WATCHDOG_TIMEOUT	A system watchdog timeout reset has occurred (see Section 10.36.9)
6	5	4	4	NEW_ LOGGED_FAULT_DETAIL	This bit is set whenever a new fault detail entry is logged. It is cleared whenever the LOGGED_FAULT_DETAIL command is read.
6	5	4	5	STORE_PARM_VALUE_ERROR	An error occurred during downloading the configuration
6	5	4	6:7	Reserved	
7	6	5	0	SLAVED_FAULT	The rail was shutdown because it is dependent on another rail that had a fault (paged) [See Section 10.36.9]
7	6	5	1	SEQ_ON_TIMEOUT	Sequence on timeout (paged) [See Section 10.36]
7	6	5	2	SEQ_OFF_TIMEOUT	Sequence off timeout (paged) [See Section 10.36]
7	6	5	3	HARDCODED_PARMS	PMBus hard-coded configuration values have been loaded into RAM. The data flash image on the device is empty or corrupt. This state is referred to as a NOBOARD configuration. This default configuration only minimally configures the device (for example, no rails are defined). Executing a STORE_DEFAULT_ALL command updates the data flash on the device. After a STORE_DEFAULT_ALL and reset, this HARDCODED_PARMS status bit is cleared. It also can be cleared with the CLEAR_FAULTS command.
7	6	5	4	PKGID_MISMATCH	Hardware Package ID does not match firmware

Table 55. Manufacturer Specific Status (continued)

Byte Number (write)	Byte Number (Read)	Payload Index	Bit in Each Payload Byte	Name	Descriptions
7	6	5	5	RESEQUENCE_ERROR	An error occurred during the re-sequencing operation. This occurs when one of the rails that are part of the resequence operation does not turn off before its TOFF_MAX_WARN_LIMIT.
7	6	5	6	LOGGED_FAULT_DETAIL_FULL	The LOGGED_FAULT_DETAIL buffer is full [See Section 10.29]
7	6	5	7	Reserved	

10.34 (F4h) GPI_FAULT_RESPONSES (MFR_SPECIFIC_36)

This paged Read/Write Block common command configures sets the rail response to GPI faults. The fault flag must be set for the corresponding GPI via GPI_CONFIG (0xF9 10.38) command, or this command is ignored. GPI is treated as fault only if it is transited from assertion to de-assertion. Please see **Fault Enable Flags** at 0 for more details. But if this command is used for the rail profile toggle, the Fault Enable flag is not required set via GPI_CONFIG to enable rail profile toggle. If the Fault Enable flag is set under use case of rail profile, a fault is reported and logged.

Table 56. GPI_FAULT_RESPONSES Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F4
1	0		BYTE_COUNT = 39
2	1	0	GPI Fault Responses – GPI 0
3	2	1	GPI Fault Responses – GPI 1
4	3	2	GPI Fault Responses – GPI 2
5	4	3	GPI Fault Responses – GPI 3
6	5	4	GPI Fault Responses – GPI 4
7	6	5	GPI Fault Responses – GPI 5
8	7	6	GPI Fault Responses – GPI 6
9	8	7	GPI Fault Responses – GPI 7
10	9	8	GPI Fault Responses – GPI 8
11	10	9	GPI Fault Responses – GPI 9
12	11	10	GPI Fault Responses – GPI 10
13	12	11	GPI Fault Responses – GPI 11
14	13	12	GPI Fault Responses – GPI 12
15	14	13	GPI Fault Responses – GPI 13
16	15	14	GPI Fault Responses – GPI 14
17	16	15	GPI Fault Responses – GPI 15
18	17	16	GPI Fault Responses – GPI 16
19	18	17	GPI Fault Responses – GPI 17
20	19	18	GPI Fault Responses – GPI 18
21	20	19	GPI Fault Responses – GPI 19
22	21	20	GPI Fault Responses – GPI 20
23	22	21	GPI Fault Responses – GPI 21
24	23	22	GPI Fault Responses – GPI 22
25	24	23	GPI Fault Responses – GPI 23
26	25	24	GPI Fault Responses – GPI 24
27	26	25	GPI Fault Responses – GPI 25

Table 56. GPI_FAULT_RESPONSES Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
28	27	26	GPI Fault Responses – GPI 26
29	28	27	GPI Fault Responses – GPI 27
30	29	28	GPI Fault Responses – GPI 28
31	30	29	GPI Fault Responses – GPI 29
32	31	30	GPI Fault Responses – GPI 30
33	32	31	GPI Fault Responses – GPI 31
34	33	32	Time between retries
35	34	33	Max glitch time for GPI(high byte)
36	35	34	Max glitch time for GPI(low byte)
37	36	35	GPI number Rail Profile Selection 1
38	37	36	GPI number Rail Profile Selection 2
39	38	37	Block Out period for profile (high byte)
40	39	38	Block Out period for profile (low byte)

10.34.1 Fault Responses Byte

Section 10.23.1 lists the byte definition of Fault Responses Byte.

10.34.2 Time Between Retries

When configured to do so, this value determines the amount of time that the device waits before it tries to re-enable a rail after it was shut down due to a fault. The byte is formatted according to Section 2.5. This value has to be 1ms or bigger.

10.34.3 Max Glitch Time for GPI

The value in these bytes is multiplied by 300us to get the max glitch of GPI input if the GPI is used for fault response.

10.34.4 GPI Number Rail Profile Pin Selection

Rail Profile Selection can be enabled with the input pin identified by this byte. The function is ignored if the value of this byte is 0 and the corresponding profile selection state is default at de-asserted. When this function is enabled, the assigned GPI pin is used to select the predefine Rail Profile based on the asserted status. Section 9.4 describes the RAIL_PROFILE_INDEX pre-defined rail profile. Moreover, the assigned GPI pin cannot be used for other functions, such as Fault response, GPO output. It is application's responsibility to make sure the setting are correct, Device does not perform any checks about these. Each Rail could have up to 2 GPI as rail profile selection.

Table 57. Rail Profile Pin Selection

Rail Profile Index	GPI Number Rail Profile Selection 2	GPI Number Rail Profile Selection 1	Rail has 1 Profile	Rail has 2 Profiles	Rail has 3 Profiles	Rail has 4 Profiles
0	De-asserted	De-asserted	0	0	0	0
1	De-asserted	Asserted	0	1	1	1
2	Asserted	De-asserted	0	0	2	2
3	Asserted	Asserted	0	1	2	3

10.34.5 Block Out Period for Profile

The value in these two bytes multiplied by 400 µs defines the block out period which blocks all voltage related fault on the giving rail when profile is changed. Block out period is only reloaded when there is profile switched.

10.35 (F5h) MARGIN_CONFIG (MFR_SPECIFIC_37)

This paged Read/Write Byte command configures if a given rail can be margined, and if so, how. GPI Rail does not support margin function.

Table 58. MARGIN_CONFIG Command Format

Bit(s)	Name	Description
Byte 0		
7:5	Reserved	Reserved
4:0	PWM Pin	Selects the PWM pin. This value is a PWM-capable pin ID from Table 11. The frequency for the PWM is configured with the PWM_CONFIG command.
Byte 1		
7:6	Mode(1)	b'00: DISABLE - Margining is disabled b'01: ENABLE_HIGH_IMPEDANCE - When not margining, the PWM pin is put in a high-impedance state b'10: ENABLE_ACTIVE_TRIM - When not margining, the PWM duty cycle is continuously adjusted to keep the voltage at VOUT_COMMAND b'11: ENABLE_FIXED_DUTY_CYCLE - When not margining, the PWM duty cycle is set to a fixed duty cycle
5	Ignore Faults	When margining is enabled with a pin, this bit determines if faults (over-voltage and under-voltage) are ignored or not.
4	Duty Cycle	This bit determines the relationship between the duty cycle and the output voltage. The output voltage increases when the duty cycle: 1 – increases 0 – decreases
3:0	Reserved	Reserved

(1) If the Mode is not DISABLE, the associated PWM_CONFIG command must be written before the MARGIN_CONFIG command is written.

10.36 (F6h) SEQ_CONFIG (MFR_SPECIFIC_38)

This Read/Write Block command configures the sequencing dependencies and enable pin for a given rail.

Features include:

- Sequencing – Configures interdependency between how voltage rails are enabled/disabled
- Fault Slaves – Configure slave pages which also shut down when a fault occurs
- Enable Pin – Identifies the enable pin, and its operating characteristics.

NOTE: All configurations done with the GPI_CONFIG command must be done before writing this command.

NOTE: When this command is written, the enable pin for the rail is de-asserted. Then the state of the rail is reevaluated. If it is determined that the rail should be on, the enable pin is asserted.

Table 59. SEQ_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F6
1	0		BYTE_COUNT = 29
2	1	0	Enable Pin Configuration it Definitions: 7:0: Pin Id of Enable Pin
3	2	1	Enable Pin Configuration Bit Definitions: 7:3: Reserved 2: Polarity of Enable pin 1:0 Pin Mode of Enable Pin
4	3	2	GPI Sequence On Dependency Mask (Byte 0 - LSB)
5	4	3	GPI Sequence On Dependency Mask (Byte 1)
6	5	4	GPI Sequence On Dependency Mask (Byte 2)
7	6	5	GPI Sequence On Dependency Mask (Byte 3 - MSB)
8	7	6	GPI Sequence Off Dependency Mask (Byte 0 - LSB)
9	8	7	GPI Sequence Off Dependency Mask (Byte 1)
10	9	8	GPI Sequence Off Dependency Mask (Byte 2)
11	10	9	GPI Sequence On Dependency Mask (Byte 3 - MSB)
12	11	10	Sequencing Timeout Configuration
13	12	11	Sequencing On Timeout
14	13	12	Sequencing Off Timeout
15	14	13	Page Sequence On Dependency Mask (Byte 0 - LSB)
16	15	14	Page Sequence On Dependency Mask (Byte 1)
17	16	15	Page Sequence On Dependency Mask (Byte 2)
18	17	16	Page Sequence On Dependency Mask (Byte 3 - MSB)
19	18	17	Page Sequence Off Dependency Mask (Byte 0 - LSB)
20	19	18	Page Sequence Off Dependency Mask (Byte 1)
21	20	19	Page Sequence Off Dependency Mask (Byte 2)
22	21	20	Page Sequence Off Dependency Mask (Byte 3 - MSB)
23	22	21	Fault Slaves Mask (Byte 0 - LSB)
24	23	22	Fault Slaves Mask (Byte 1)
25	24	23	Fault Slaves Mask (Byte 2)
26	25	24	Fault Slaves Mask (Byte 3 - MSB)
27	26	25	GPO Sequence Off Dependency Mask(Byte 0 – LSB)
28	27	26	GPO Sequence On Dependency Mask(Byte 1)
29	28	27	GPO Sequence Off Dependency Mask(Byte 0 – LSB)
30	29	28	GPO Sequence Off Dependency Mask(Byte 1)

The turn on condition for each page can depend on the state of several other pages and/or input pins. The same pages and pins also may be used to control multiple pages. The GPI and Page dependencies (Sequence On Dependencies) define a set of conditions which allow a page to turn on when met. Note that the logical AND of all conditions must be met. Once the page is on, these dependencies have no further effect on the operating status of the page. Specifically, they do not cause a page to turn off.

Sequence On Dependencies work in parallel with the PMBus defined mechanisms used to enable an output. That is, both the Sequence On Dependencies and the PMBus mechanism must be satisfied. For example, if the page responds to an OPERATION command, until ON is specified by the command, the page remains off even if all of the sequencing Sequence On Dependencies are met. Further, the order in which they are met is irrelevant; the OPERATION command can be issued first and then the sequencing requirements, when met, turn on the output, or the sequencing requirements can be met first in which case the page would wait for the command. In the ON_OFF_CONFIG command a “None” setting, is still subject to the specified Sequence On Dependencies.

Turn on delay (TON_DELAY) is applied after the page has been commanded on and Sequence On Dependencies are met.

Unless the rail is instructed to turn off immediately, these same comments apply to the Sequence Off Dependencies – they must be met before the rail is turned off, the turn off delay (TOFF_DELAY) is applied after the dependencies are met, etc.

After a fault, the PMBus specification declares that an OFF/ON sequence occur before the rail is allowed to restart. Note that the toggle of sequencing pin is interpreted to meet this requirement. For example, consider a page that responds to the CTRL_PIN and has a Turn-On Dependency which shuts down due to a fault. A toggle low then high on either the CTRL_PIN or the sequencing pin is sufficient to restart the page.

NOTE: Some tables in the following subsections assume that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.36.1 Enable Pin Configuration

See Section 7 for byte format and details.

Enable pins are configured just like output pins. They are active once conditions dictate that a page must be enabled and inactive until then. The conditions are defined by the **GPI Dependency Mask** and the **Page Dependency Mask** in this command and the value given by the TON_DELAY command.

NOTE: The “input” mode is invalid for enable pins. Attempting to set the mode bits returns a NACK due to Invalid Data.

10.36.2 GPI Sequence On Dependency Mask

Each of the 32 pages has its own GPI Sequence On Dependency Mask, whose bits are defined as follows:

Bit	31	30	29	28	27	26	25	24
Purpose	GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24

Bit	23	22	21	20	19	18	17	16
Purpose	GPI23	GPI22	GPI21	GPI20	GPI19	GPI18	GPI17	GPI16

Bit	15	14	13	12	11	10	9	8
Purpose	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8

Bit	7	6	5	4	3	2	1	0
Purpose	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

The enable pin for the page is not asserted until all of the input pins selected by the GPI bits are asserted. Once the enable pin is asserted, the state of these GPI pins has no effect on the state of the enable pin. Each page can depend on the state of up to thirty-two input pins. The same pins can be used to control multiple pages. (see Section 10.39)

10.36.3 GPI Sequence Off Dependency Mask

Each of the 32 pages has its own GPI Sequence Off Dependency Mask, whose bits are defined as follows:

Bit	31	30	29	28	27	26	25	24
Purpose	GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Purpose	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

Bit	15	14	13	12	11	10	9	8
Purpose	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8

Bit	7	6	5	4	3	2	1	0
Purpose	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

The enable pin for the page is not de-asserted until all of the input pins selected by the GPI bits are de-asserted. Once the enable pin is de-asserted, the state of these GPI pins has no effect on the state of the enable pin.

Each page can depend on the state of up to thirty-two input pins. The same pins can be used to control multiple pages. (see Section 10.39)

10.36.4 Sequencing Timeout Configuration

The configuration bits in Table 60 dictate how the device will respond to sequence timeouts. Whenever a sequencing timeout occurs, the associated status and log information will be updated.

Table 60. Sequencing Timeout Configuration Byte

Bit(s)	Name	Description
7:4	Reserved	
3:2	Sequence-Off Timeout Action	This bits determine what action will be taken after a sequence-off timeout occurs: b'00 – The device continues to wait indefinitely for the sequence-off dependencies to be met. b'01 – The device stops waiting for the sequence-off dependencies to be met and continues the process of disabling the rail. b'10 – (same as b'00 action) b'11 – (same as b'00 action)
1:0	Sequence-On Timeout Action	This bits determine what action occurs after a sequence-on timeout occurs: b'00 – The device continues to waits indefinitely for the sequence-on dependencies to be met. b'01 – The device stops waiting for the sequence-on dependencies to be met and continues the process of enabling the rail. b'10 – The device resequences this rail and all fault shutdown slaves associated with this rail. This operation is defined by the "Time between Resequences" byte and the "Max Resequences" field in the MISC_CONFIG command (see Section 2.5). b'11 – (same as b'00 action)

10.36.5 Sequencing On Timeout

This timeout value is used to check that rail sequences on within a certain period of time. In other words, this timeout is used to detect if one of the rail's sequence-on dependencies is never met. When this occurs, a status bit will be set. A timeout value of 0 disables the timeout monitoring function.

This byte is formatted according to Section 2.5.

10.36.6 Sequencing Off Timeout

This timeout value is used to check that rail sequences off within a certain period of time. In other words, this timeout is used to detect if one of the rail's sequence-off dependencies is never met. When this occurs, a status bit will be set.

A timeout value of 0 disables the timeout monitoring function. This byte is formatted according to Section 2.5.

10.36.7 Page Sequence On Dependency Mask

Each of the 32 pages has its own Page Sequence On Dependency Mask, whose bits are defined as follows:

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24

Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

The enable pin for the page is not asserted until all of the rails selected by these bits have reached their power-good state.

Each page can depend on the state of several other pages. The same pages can be used to control other pages as well.

10.36.8 Page Sequence Off Dependency Mask

Each of the 23 pages has its own Page Sequence Off Dependency Mask, whose bits are defined as follows:

Bit	31	30	29	28	27	26	25	24
Purpose	PAGE31	PAGE30	PAGE29	PAGE28	PAGE27	PAGE26	PAGE25	PAGE24

Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

The enable pin for the page is not de-asserted until all of the rails selected by these bits have left their power-good state.

Each page can depend on the state of several other pages. The same pages can be used to control other pages as well.

10.36.9 Fault Slaves Mask

Each of the 213 pages has its own Fault Slaves Mask, whose bits are defined as follows:

31	30	29	28	27	26	25	24
Page31 fault slave	Page30 fault slave	Page29 fault slave	Page28 fault slave	Page27 fault slave	Page26 fault slave	Page25 fault slave	Page24 fault slave
23	22	21	20	19	18	17	16
Page23 fault slave	Page22 fault slave	Page21 fault slave	Page20 fault slave	Page19 fault slave	Page18 fault slave	Page17 fault slave	Page16 fault slave
15	14	13	12	11	10	9	8
Page15 fault slave	Page14 fault slave	Page13 fault slave	Page12 fault slave	Page11 fault slave	Page10 fault slave	Page9 fault slave	Page8 fault slave
7	6	5	4	3	2	1	0
Page7 fault slave	Page6 fault slave	Page5 fault slave	Page4 fault slave	Page3 fault slave	Page2 fault slave	Page1 fault slave	Page0 fault slave

Each page can have multiple fault slave pages. When a fault occurs on any pages, if its response is set to shut down, all slave pages are also shut down. If retries are specified for the master page, the slave page(s) remain running until all retries are exhausted. The slave pages are shut down using sequence off dependencies and TOFF_DELAY. The dependent pages do not perform any retries as a result of this action.

After being shut down, slave rails are latched off as if they had experienced the fault. To re-enable their outputs, an off command must be received before another on command is accepted. A status bit is set in their MFR_STATUS word indicating the reason they are latched off.

The fault slaves Mask is also part of graceful shutdown function, which is defined in the 10.6(MONITOR_CONFIG command).During the graceful shutdown period, the UV faults from those rails defined by the Mask are not logged and responded.

10.36.10 GPO Sequence On Sependency Mask

Each of the 32 pages has its own GPO Sequence On Dependency Mask, whose bits are defined as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0

The enable pin for the page is not asserted until all of the pins selected by the LGPO bits are asserted. Once the enable pin is asserted, the state of these LGPO pins has no effect on the state of the enable pin.

Each page can depend on the state of up to sixteen LGPO pins. The same pins can be used to control multiple pages. (See Section 10.39)

10.36.11 GPO Sequence Off Sependency Mask

Each of the 32 pages has its own GPO Sequence Off Dependency Mask, whose bits are defined as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0

The enable pin for the page is not de-asserted until all of the pins selected by the GPO bits are de-asserted. Once the enable pin is de-asserted, the state of these GPO has no effect on the state of the enable pin.

Each page can depend on the state of up to sixteen GPO. The same GPO can be used to control multiple pages. (See Section 10.38)

10.37 (F7h) GPO_CONFIG_INDEX (MFR_SPECIFIC_39)

This R/W Byte common command selects the index of the GPO that will be used for later GPO_CONFIG commands.

7	6	5	4	3	2	1	0
0	0	0	GPO Index				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 61. Relationship Between GPO_CONFIG_INDEX and the Actual GPO Number

GPO_CONFIG_INDEX	GPO
0	1
1	2
...	...
15	16

10.38 (F8h) GPO_CONFIG (MFR_SPECIFIC_40)

This Read/Write Block paged command configures the functionality of a given output pin. This paged command allows pins to be configured as status/GPI-influenced outputs. The state of the output pin is determined by a selection of GPIs and statuses that are processed through some combinational logic with optional inversion steps. In most cases, the statuses are related to pages (for example, Power Good).

NOTE: All configurations done with the MONITOR_CONFIG, GPI_CONFIG, and SEQ_CONFIG commands must be done before writing this command.

Figure 2 provides an overview of how the state of the GPO is determined.

NOTE: This document refers to the AND paths starting with “AND Path 0”. Fusion refers to the AND paths starting with and index of 1 instead of 0.

NOTE: The information in Figure 2 implies that the device supports 12 rails (0 to 11). For the UCD90320, this is not the case. It only supports 32 rails and the interpretation of this information should be adjusted for the correct number of rails.

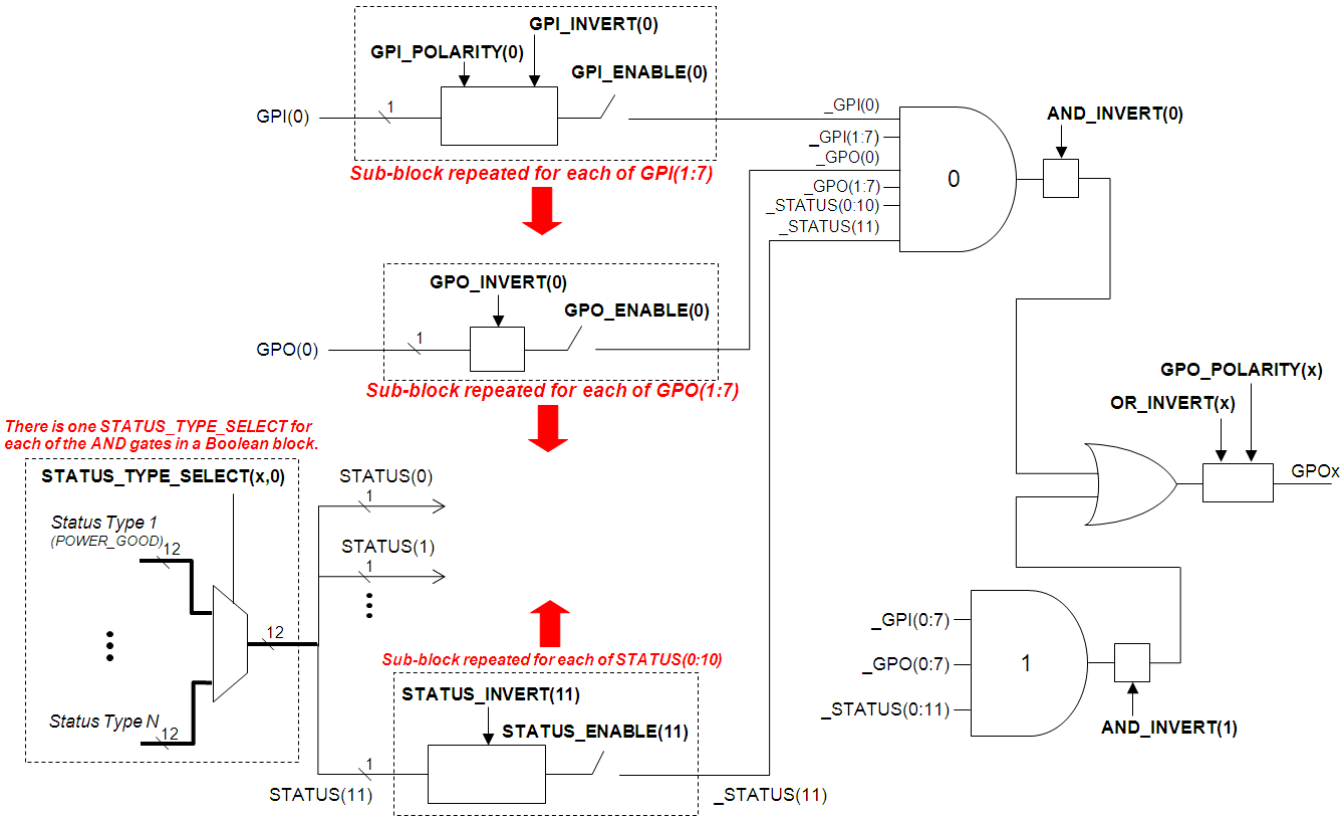

Figure 2. Factors Determining the State of a GPO

NOTE: For the sake of code efficiency, all configured/active GPOs must be packed in the lower page numbers. This means, if there is only one configured GPO, it must be associated with page zero. If there are two, they must be associated with page zero and one.

Table 62. GPO_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F8
1	0		BYTE_COUNT = 54
2	1	0	Output Pin Configuration Bit Descriptions: 7:0: Pin ID for GPO pin
3	2	1	Output Pin Configuration Bit Descriptions: 7:3: Reserved 2: Polarity of GPO pin 1:0: Pin Mode of GPO pin
4	3	2	Bit Descriptions: 7: Assert Delay Enable 6: De-assert Delay Enable 5: Invert OR Output 4: Ignore Inputs During Delay 3:0: High Resolution Delay Count
5	4	3	Millisecond Delay

Table 62. GPO_CONFIG Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
6	5	4	AND Path 0 Configuration Bit Description 7 Invert AND Output 6 State Machine Mode Enable 5:0 Status Type
7	6	5	AND Path 1 Configuration Bit Description 7 Invert AND Output 6 Reserved 5:0 Status Type
			AND Path 0
8	7	6	Status Mask (Byte 0 - LSB)
9	8	7	Status Mask (Byte 1)
10	9	8	Status Mask (Byte 2)
11	10	9	Status Mask (Byte 3)
12	11	10	Status Inversion Mask (Byte 0 - LSB)
13	12	11	Status Inversion Mask (Byte 1)
14	13	12	Status Inversion Mask (Byte 2)
15	14	13	Status Inversion Mask (Byte 3)
16	15	14	GPI Mask (Byte 0 – LSB)
17	16	15	GPI Mask (Byte 1)
18	17	16	GPI Mask (Byte 2)
19	18	17	GPI Mask (Byte 3 – LSB)
20	19	18	GPI Inversion Mask (Byte 0 – LSB)
21	20	19	GPI Inversion Mask (Byte 1)
22	21	20	GPI Inversion Mask (Byte 2)
23	22	21	GPI Inversion Mask (Byte 3 - LSB)
24	23	22	GPO Mask (Byte 0 – LSB)
25	24	23	GPO Mask (Byte 1)
26	25	24	Reserved
27	26	25	GPO Mask (Byte 3)Reserved
28	27	26	GPO Inversion Mask (Byte 0 – LSB)
29	28	27	GPO Inversion Mask (Byte 1)
30	29	28	Reserved
31	30	29	Reserved
			AND Path 0
32	31	30	Status Mask (Byte 0 - LSB)
33	32	31	Status Mask (Byte 1)
34	33	32	Status Mask (Byte 2)
35	34	33	Status Mask (Byte 3)
36	35	34	Status Inversion Mask (Byte 0 - LSB)
37	36	35	Status Inversion Mask (Byte 1)
38	37	36	Status Inversion Mask (Byte 2)
39	38	37	Status Inversion Mask (Byte 3)
40	39	38	GPI Mask (Byte 0 – LSB)
41	40	39	GPI Mask (Byte !)
42	41	40	GPI Mask (Byte 2)
43	42	41	GPI Mask (Byte 3 – MSB)

Table 62. GPO_CONFIG Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
44	43	42	GPI Inversion Mask (Byte 0 – LSB)
45	44	43	GPI Inversion Mask (Byte 1)
46	45	44	GPI Inversion Mask (Byte 2)
47	46	45	GPI Inversion Mask (Byte 3 – MSB)
48	47	46	GPO Mask (Byte 0 – LSB)
49	48	47	GPO Mask (Byte 1)
50	49	48	Reserved
51	50	49	Reserved
52	51	50	GPO Inversion Mask (Byte 0 – LSB)
53	52	51	GPO Inversion Mask (Byte 1)
54	53	52	Reserved
55	54	53	Reserved

10.38.1 Output Pin Configuration

This configures which pin is used for this GPO, its polarity, and if it is actively driven or not. For details, see Section 7. A mode of “Input” causes this command to be rejected (receive a NACK).

This value must be equal to the Pin ID from Table 11.

10.38.2 Assert Delay Enable

When this bit is set there will be a delay (High Resolution and/or Millisecond) before the GPO is asserted.

10.38.3 De-Assert Delay Enable

When this bit is set there will be a delay (High Resolution and/or Millisecond) before the GPO is de-asserted.

10.38.4 Invert OR Output

When this bit is set, the result of the OR operation is inverted. This can be used to change the OR operation into an AND operation, (a OR b) = (a’ AND b’)’.

10.38.5 Ignore Inputs During Delay

When this bit is set, changes to the inputs affecting the state of the GPO is ignored while the update to the GPO is delayed. For example, Figure 3 shows the behavior when a GPO simply follows the state of a GPI with a 3 millisecond delay on assertion and de-assertion.

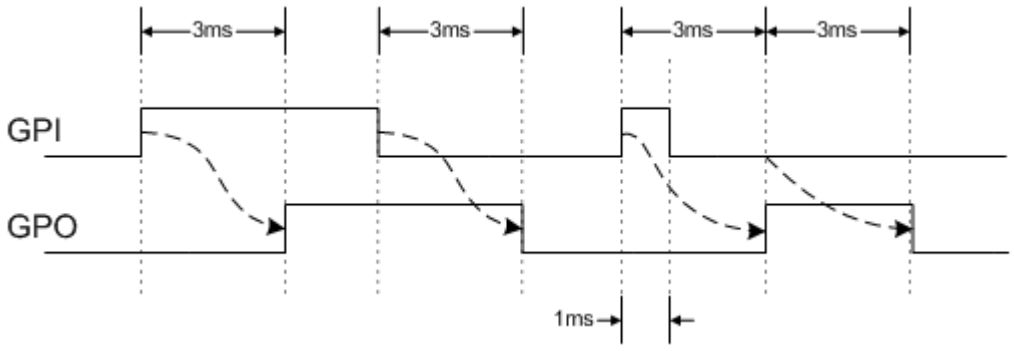

Figure 3. Ignore Inputs On

Figure 4 shows the behavior of previous example without this bit set.

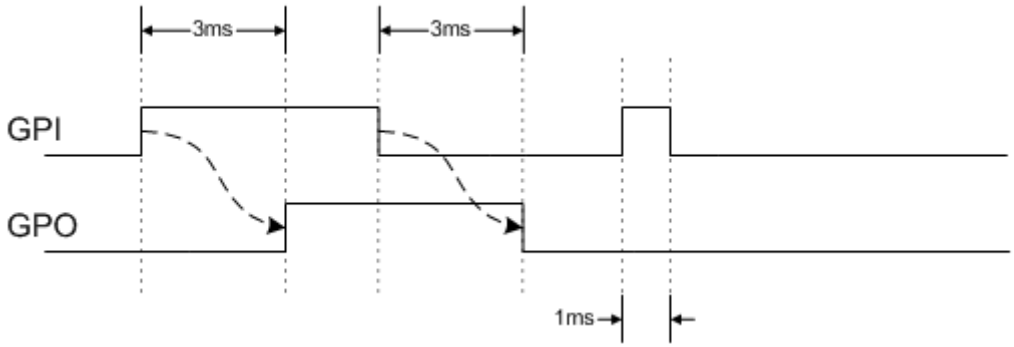

Figure 4. Ignore Inputs Off

With this bit set, and there is a 3 ms delay on the de-assertion, and no delay on assertion, Figure 5 shows the behavior for this example.

NOTE: The second deassert-to-assert pulse is only as long as the sampling period used for the GPI pins, which happens to be 100 µs.

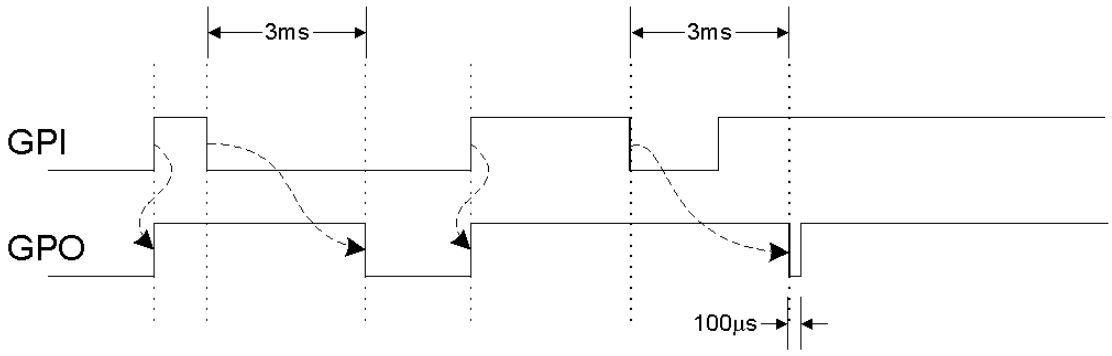

Figure 5. Ignore Inputs On with Delay

10.38.6 Invert AND Output

When this bit is set, the associated AND path result is inverted before it is fed into the OR gate. This can be used to change the AND operation into an OR operation, (a' AND b')' = (a OR b).

10.38.7 State Machine Mode Enable

When this bit is set, only one of the AND path is used at a given time. When the GPO logic result is currently TRUE, AND path 0 is used until the result becomes FALSE. When the GPO logic result is currently FALSE, AND path 1 is used until the result becomes TRUE. This logic provides a very simple state machine and allows for more complex logical combinations.

NOTE: The device initially evaluates AND path 0. If it is TRUE, it continues to evaluate AND path 0. If it is FALSE, it begins evaluating AND path 1.

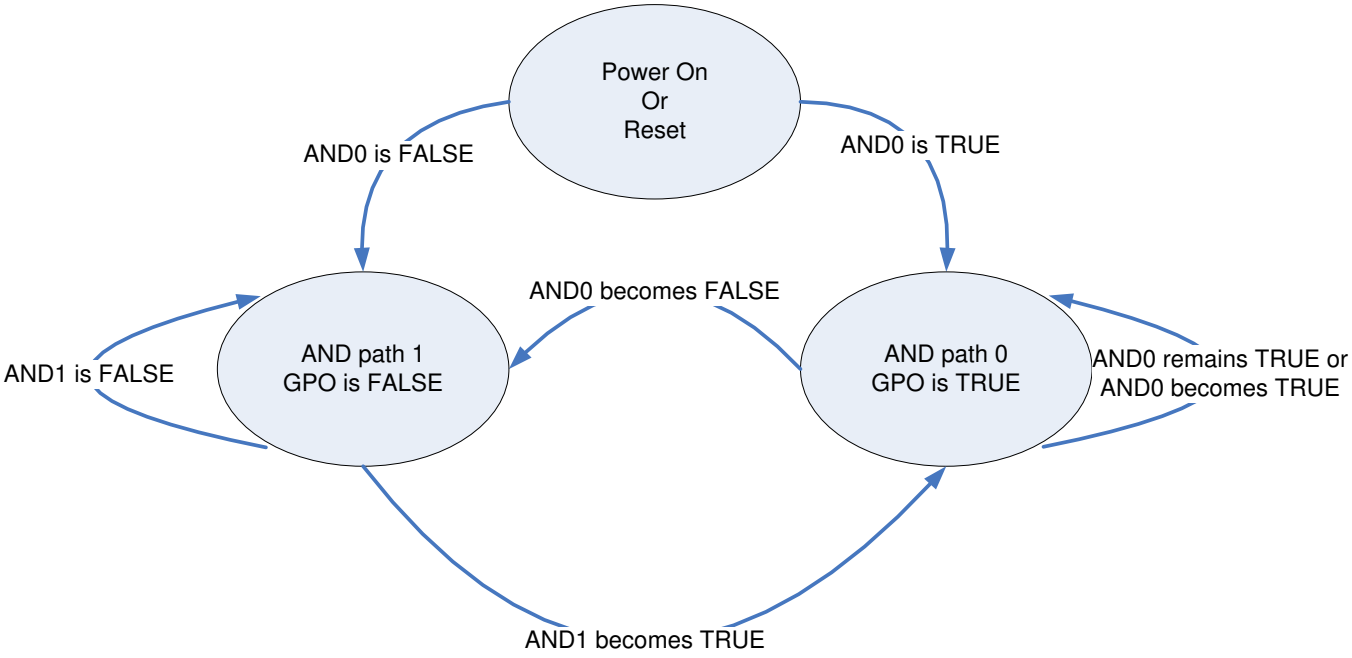

Figure 6. State Machine

For example, for a GPO to be asserted if two GPI pins are both asserted and stay asserted until both GPIs are de-asserted, we need to apply an AND operation when the GPO is de-asserted and apply an OR operation when the GPO is asserted. This behavior is shown in Figure 7, where waveform 1 is a GPO, waveform 2 is a GPI, and waveform 3 is a GPO.

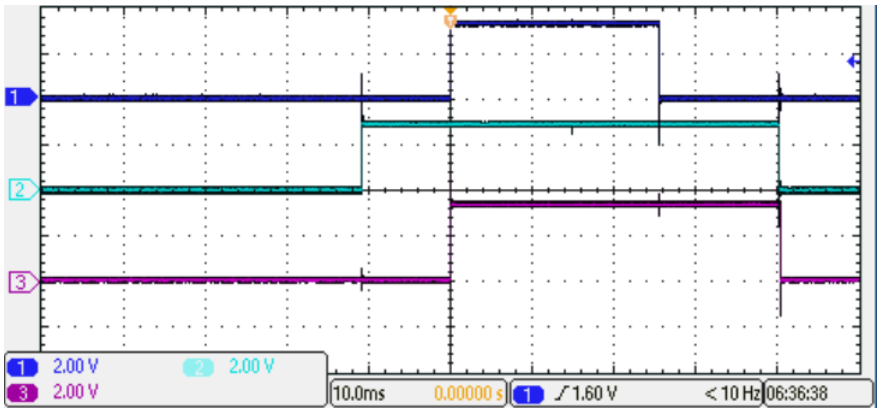

Figure 7. Example of State Machine

This behavior is configured by setting the “State Machine Mode Enable”, configuring AND path 0 as (GPI1’ AND GPI2’)’, and configuring AND path 1 as (GPI1 AND GPI2).

10.38.8 High Resolution Delay Count

This value is multiplied by 100 µs to define the high resolution delay.

10.38.9 9 Millisecond Delay

This value is used to delay the update of a GPO. This byte is formatted according the 8-bit time encoding defined in Section 2.5.

NOTE: Updates to the GPO may be filtered out by the delay time. Any changes in the inputs determining the state of the GPO that are less than the delay time will have no effect on the state of the GPO.

10.38.10 Status Mask

The Status Mask is made up of four configuration bytes whose bits are defined as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PAGE 31	PAGE 30	PAGE 29	PAGE 28	PAGE 27	PAGE 26	PAGE 25	PAGE 24	PAGE 23	PAGE 22	PAGE 21	PAGE 20	PAGE 19	PAGE 18	PAGE 17	PAGE 16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGE 15	PAGE 14	PAGE 13	PAGE 12	PAGE 11	PAGE 10	PAGE 9	PAGE 8	PAGE 7	PAGE 6	PAGE 5	PAGE 4	PAGE 3	PAGE 2	PAGE 1	PAGE 0

Each bit selects which page(s) are to be used in a given AND path. Setting the bit associated with a given page to 1 enables the associated status for that page. If the bit associated with a page is set to 0, the status for page has no effect on the state of the GPO.

10.38.11 Status Inversion Mask

Each of the statuses for a given page (denoting by setting the appropriate bit here to 1) may be inverted before being used in a given AND path. Setting the bit for a page to 1 causes the associated status to be inverted. Setting the bit to 0 has no effect.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PAGE 31	PAGE 30	PAGE 29	PAGE 28	PAGE 27	PAGE 26	PAGE 25	PAGE 24	PAGE 23	PAGE 22	PAGE 21	PAGE 20	PAGE 19	PAGE 18	PAGE 17	PAGE 16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGE 15	PAGE 14	PAGE 13	PAGE 12	PAGE 11	PAGE 10	PAGE 9	PAGE 8	PAGE 7	PAGE 6	PAGE 5	PAGE 4	PAGE 3	PAGE 2	PAGE 1	PAGE 0

10.38.12 GPI Mask

This mask determines which of the GPIs are used for the given AND path. Setting the bit associated with a given GPI to 1 enables that GPI's state to influence the state of the GPO. If the bit associated with a GPI is set to 0, the state of that GPI has no effect on the state of the GPO. (See Section 10.39)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24	GPI23	GPI22	GPI21	GPI20	GPI19	GPI18	GPI17	GPI16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

10.38.13 GPI Inversion Mask

This mask determines if the GPI state is inverted before being used for the given AND path. Setting the bit for a GPI to 1 causes the associated state to be inverted. Setting the bit to 0 has no effect.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24	GPI23	GPI22	GPI21	GPI20	GPI19	GPI18	GPI17	GPI16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

10.38.14 GPO Mask

This mask determines which of the first 8 GPOs are used for the given AND path. Setting the bit associated with a given GPO to 1 enables that GPO's state to influence the state of another GPO. If the bit associated with a GPO is set to 0, the state of that GPO has no effect on the state of another GPO.

NOTE: The pin polarity setting for a GPO does not affect the influence of that GPO on another GPO.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0

10.38.15 GPO Inversion Mask

This mask determines if the GPO state is inverted before being used for the given AND path. Setting the bit for a GPO to 1 causes the associated state to be inverted. Setting the bit to 0 has no effect.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0

10.38.16 Status Type Select

This selection determines which status type is applied to the Status Mask. Each AND path can select a different status type.

The _LATCH version of these status flags is latched and only cleared when explicitly directed to with a command (CLEAR_FAULTS) or a GPI (see Section 10.39.3). The non-_LATCH version is the actual current state of the condition.

NOTE: The MARGIN_EN and MRG_LOW_nHIGH statuses are updated based on GPI pins (see GPI_CONFIG, see Section 10.39) and/or the OPERATION command. Whenever the OPERATION command disables margining, the MRG_LOW_nHIGH status will be set to true.

NOTE: After the following status types are set, they require that the rail is turned off and then back on before they are cleared: TON_MAX_FAULT, TOFF_MAX_WARN, SEQ_ON_TIMEOUT, SEQ_OFF_TIMEOUT. Note that a resequence operation will clear these status types, because it will turn the rail off and then turn the rail on.

NOTE: When the _LATCH version of a status flag is cleared, it will stay FALSE even if the status is still TRUE. After that, it will only become TRUE again after the status goes to the FALSE state and back to the TRUE state.

Table 63. Status Types

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH

Table 63. Status Types (continued)

Encoding	Status Type
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	IOUT_OC_FAULT
10	IOUT_OC_WARN
11	IOUT_UC_FAULT
12	TEMP_OT_FAULT
13	TEMP_OT_WARN
14	SEQ_ON_TIMEOUT
15	SEQ_OFF_TIMEOUT
16	SYSTEM_WATCHDOG_TIMEOUT
17	VOUT_OV_FAULT_LATCH
18	VOUT_OV_WARN_LATCH
19	VOUT_UV_WARN_LATCH
20	VOUT_UV_FAULT_LATCH
21	TON_MAX_FAULT_LATCH
22	TOFF_MAX_WARN_LATCH
23	IOUT_OC_FAULT_LATCH
24	IOUT_OC_WARN_LATCH
25	IOUT_UC_FAULT_LATCH
26	TEMP_OT_FAULT_LATCH
27	TEMP_OT_WARN_LATCH
28	SEQ_ON_TIMEOUT_LATCH
29	SEQ_OFF_TIMEOUT_LATCH
30	SYSTEM_WATCHDOG_TIMEOUT_LATCH

10.38.17 GPO Configuration Examples

Example 1: GPO = POWER_GOOD(0) *AND* POWER_GOOD(2) *AND* POWER_GOOD(5) *AND* POWER_GOOD(7) *AND* POWER_GOOD(8)

Status Mask 0 = 0x01A3
Status Inversion Mask 0 = 0x0000
GPI Mask 0 = 0x00
Status Type Select 0 = 0

Status Mask 1 = 0x0000
GPI Mask 1 = 0x00

Status Mask 2 = 0x0000
GPI Mask 2 = 0x00

Status Mask 3 = 0x0000
GPI Mask 3 = 0x00

Example 2: GPO = (*NOT* POWER_GOOD[0]) *OR* (*NOT* POWER_GOOD[2]) *OR* (*NOT* POWER_GOOD[5]) *OR* (*NOT* POWER_GOOD[7])

Status Mask 0 = 0x0001
Status Inversion Mask 0 = 0x0001
GPI Mask 0 = 0x00
Status Type Select 0 = 0

Status Mask 1 = 0x0004
Status Inversion Mask 1 = 0x0004
GPI Mask 1 = 0x00
Status Type Select 1 = 0

Status Mask 2 = 0x0020
Status Inversion Mask 2 = 0x0020
GPI Mask 2 = 0x00
Status Type Select 2 = 0

Status Mask 3 = 0x0080
Status Inversion Mask 3 = 0x0080
GPI Mask 3 = 0x00
Status Type Select 3 = 0

Example 3: GPO = ((*NOT* POWER_GOOD[0]) *AND* (*NOT* GPI[3])) *OR* ((*NOT* POWER_GOOD[1]) *AND* (*NOT* GPI[3])) *OR* (VOUT_OV_WARN[2] *AND* (*NOT* GPI[3]))

Status Mask 0 = 0x0001
Status Inversion Mask 0 = 0x0001
GPI Mask 0 = 0x04
GPI Inversion Mask 0 = 0x04
Status Type Select 0 = 0

Status Mask 1 = 0x0002
Status Inversion Mask 1 = 0x0002
GPI Mask 1 = 0x04
GPI Inversion Mask 1 = 0x04
Status Type Select 1 = 0

Status Mask 2 = 0x0004
Status Inversion Mask 2 = 0x0004
GPI Mask 2 = 0x04
GPI Inversion Mask 2 = 0x04
Status Type Select 2 = 3

Status Mask 3 = 0x0000
GPI Mask 3 = 0x00

Example 4: GPO = (GPI[0] *AND* GPI[2]) *OR* (GPI[0] *AND* (*NOT* GPI[4]) *AND* (*NOT* GPI[7]) *OR* GPI[3] *OR* GPI[7]

Status Mask 0 = 0x0000
GPI Mask 0 = 0x05
GPI Inversion Mask 0 = 0x00

Status Mask 1 = 0x0000
GPI Mask 1 = 0x91
GPI Inversion Mask 1 = 0x90

Status Mask 2 = 0x0000

GPI Mask 2 = 0x04
GPI Inversion Mask 2 = 0x00

Status Mask 3 = 0x0000
GPI Mask 3 = 0x80
GPI Inversion Mask 3 = 0x00

Example 5: GPO = VOUT_OV_WARN[1] *AND* IOUT_OC_WARN[1]
Cannot implement this directly. Apply the relationship (a AND b) = (a' OR b')' = >
GPO = *NOT* ((*NOT* VOUT_OV_WARN[1]) *OR* (*NOT* IOUT_OC_WARN[1]))

Status Mask 0 = 0x0002
Status Inversion Mask 0 = 0x0002
GPI Mask 0 = 0x00
Status Type Select 0 = 4

Status Mask 1 = 0x0002
Status Inversion Mask 1 = 0x0002
GPI Mask 1 = 0x00
Status Type Select 1 = 16

Status Mask 2 = 0x0000
GPI Mask 2 = 0x00

Status Mask 3 = 0x0000
GPI Mask 3 = 0x00

10.39 (F9h) GPI_CONFIG (MFR_SPECIFIC_41)

This Read/Write Block common command configures the functionality for the input pins (GPI). Up to 23 pins may be configured as control inputs.

Table 64. GPI_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 57
2	1	0	GPI_0 Pin Configuration. See Table 65
3	2	1	GPI_0/1 Pin Configuration. See Table 65
4	3	2	GPI_1 Pin Configuration. See Table 65
5	4	3	GPI_2 Pin Configuration. See Table 65
6	5	4	GPI_2/3 Pin Configuration. See Table 65
7	6	5	GPI_3 Pin Configuration. See Table 65
...	...	...	...
44	43	42	GPI_28 Pin Configuration. See Table 65
45	44	43	GPI_28/29 Pin Configuration. See Table 65
46	45	44	GPI_29 Pin Configuration. See Table 65
47	46	45	GPI_30 Pin Configuration. See Table 65
48	47	46	GPI_30/31 Pin Configuration. See Table 65
49	48	47	GPI_31 Pin Configuration. See Table 65
50	49	48	Fault Enable Flags – Byte 0 (LSB)
51	50	49	Fault Enable Flags – Byte 1
52	51	50	Fault Enable Flags – Byte 2
53	52	51	Fault Enable Flags – Byte 3 (MSB)
54	53	52	Latched Statuses Clear Pin Selection
55	54	53	“Margin Enable” (MRG_EN) Pin Selection
56	55	54	“Margin Low/Not-High” (MRG_LOW_nHIGH) Pin Selection
57	56	55	Fans Installed Pin Selection
58	57	56	Debug Mode Pin Selection

10.39.1 GPI Pin Configuration

These bytes configure which pin is used for each GPI and its polarity. A mode other than “Unused” or “Input” causes this command to be rejected (receive Please see

Table 65. GPI Pin Configuration

GPI Index M + 1				GPI Index M			
BYTE N + 1				BYTE N + 2			BYTE N
Bit[7]	Bit[6]	Bit[5:4]	Bit[3:0]	Bit[7:4]	Bit[3]	Bit[2]	Bit[1:0]	Bit[7:0]
Fault Pin	Polarity	Mode	Pin ID[7:4]	Pin ID[3:0]	Fault Pin	Polarity	Mode	Pin ID[7:0]

N = (GPI _M/ 2) * 3

NOTE: The input pin configurations, if used, must start in the Input Pin Configuration byte and continue in consecutive order with no gaps. That is, no Unused-Mode Pin Configurations can be between any Input-Mode Pin Configurations.

NOTE: Fault Pin bit. When this bit is set with GPI_CONFIG command, the corresponding pin is behaved as FAULT pin instead of GPI pin. MAX 4 pin could be configured as Fault pin. Device shall NACK if there are more than 4 pins are configured as Fault pin. The first fault pin is the first pin who has the fault pin bit set. Fault Enable Flags

When the bit corresponding to a given GPI is set, the de-assertion of the GPI is treated as a fault. This fault will be noted in the MFR_STATUS command (see Section 10.33) and will be logged if configured to do so (see Section 10.29). When a GPI fault occurs, the PMBALERT# pin is asserted.

Table 66. Fault Enable Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPI31	GPI30	GPI29	GPI28	GPI27	GPI26	GPI25	GPI24	GPI23	GPI22	GPI21	GPI20	GPI19	GPI18	GPI17	GPI16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

10.39.2 Sequence Timeout Pin Selection

The SEQ_TIMEOUT command (D0h) defines a window during which an external event is expected to occur. That event is defined by the Input Pin selected by this byte (see Table 67). The pin is ignored if the value of this byte is zero or the SEQ_TIMEOUT window is set to 0.

Table 67. GPI Selection

Value	Description
0	Unused
1	GPI_0 Pin Configuration
2	GPI_1 Pin Configuration
3	GPI_2 Pin Configuration
4	GPI_3 Pin Configuration
5	GPI_4 Pin Configuration
6	GPI_5 Pin Configuration
7	GPI_6 Pin Configuration
8	GPI_7 Pin Configuration
9	GPI_8 Pin Configuration
10	GPI_9 Pin Configuration
11	GPI_10 Pin Configuration
12	GPI_11 Pin Configuration
13	GPI_12 Pin Configuration
14	GPI_13 Pin Configuration
15	GPI_14 Pin Configuration
16	GPI_15 Pin Configuration
17	GPI_16 Pin Configuration
18	GPI_17 Pin Configuration
19	GPI_18 Pin Configuration
20	GPI_19 Pin Configuration
21	GPI_20 Pin Configuration
22	GPI_21 Pin Configuration
23	GPI_22 Pin Configuration
24	GPI_23 Pin Configuration
25	GPI_24 Pin Configuration
26	GPI_25 Pin Configuration
27	GPI_26 Pin Configuration

Table 67. GPI Selection (continued)

Value	Description
28	GPI_27 Pin Configuration
29	GPI_28 Pin Configuration
30	GPI_29 Pin Configuration
31	GPI_30 Pin Configuration
32	GPI_31 Pin Configuration
33-255	Invalid

10.39.3 Latched Statuses Clear Pin Selection

The latched status types (_LATCH) in the GPO_CONFIG command can be cleared by a pin. That Input Pin is selected by this byte (see Table 67). The pin is ignored if the value of this byte is 0. This pin is edge-sensitive.

10.39.4 MRG_EN Pin Selection

Margining can be enabled with the Input Pin selected by this byte (see Table 67). The pin is ignored if the value of this byte is 0.

When this pin is asserted, all rails with margining enabled (see Section 10.35) are put in a margined state (low or high).

NOTE: If a valid pin is selected with this byte, a valid pin must be selected with the MRG_LOW_nHIGH byte as well.

10.39.5 MRG_LOW_nHIGH Pin Selection

The margining level (low or high) can be selected with the Input Pin identified by this byte (see Table 67). The pin is ignored if the value of this byte is 0.

When this pin is asserted and the MRG_EN pin is asserted, all rails with margining enabled (see Section 10.35) are put in the low margined state.

When this pin is not asserted and the MRG_EN pin is asserted, all rails with margining enabled are put in the high margined state.

10.39.6 Debug Mode Pin Selection

Debug Function can be enabled with the input pin identified by this byte. The pin is ignored if the value of the byte is 0. Under Debug Mode, device shall not active PMBus alert pin for any faults/warnings, not response for any fault responses and not log any faults. This function is mainly designed for debug purpose and it is not recommended in the final production

The following faults/warnings are impacted by debug mode.

VOUT_OV_FAULT	TON_MAX	IOUT_UC	SYSTEM_WATCHDOG_TIMEOUT
VOUT_OV_WARNING	TOFF_MAX Warning	OT_FAULT	SEQ_ON_TIMEOUT
VOUT_UV_FAULT	IOUT_OC_FAULT	OT_WARNING	SEQ_OFF_TIMEOUT
VOUT_UV_WARNING	IOUT_OC_WARNING	SLAVE_FAULT	RESEQUENCE_ERROR
All GPI de-asserted			

When the debug mode is on, the rail sequence on/off dependency conditions are ignored, as soon as the sequence on/off timeout is expired, the rails will be sequenced on or off accordingly regardless of the timeout action, if the sequence on/off timeout value is set to 0, the rails will be sequenced on or off immediately. The fault pin shall not pull the fault bus low when debug mode is on. Moreover LGPOs affected by these events should be back to their original states when debug mode is on. System watchdog function is disable when debug mode is on.

10.40 (FAh) GPIO_SELECT (MFR_SPECIFIC_42)

This Read/Write byte common command determines to which GPIO that the GPIO_CONFIG command applies. The value must be a valid Pin ID from 0 – 83. See Table 11.

10.41 (FBh) GPIO_CONFIG (MFR_SPECIFIC_43)

This Read/Write Byte common command configures the GPIO identified by the GPIO_SELECT command. The Status bit is read-only and gives the current state of the pin. The other bits determine if the pin is configured as an input or an output. The Enable bit must be set for the configuration information to be processed. The Out_Enable bit determines if the pin is to be an output (1 – actively driven) or an input (0 – high impedance). The Out_Value bit determines the state of the pin when it is configured as an output. If a change to an output pin's state is temporary, this command should be written a second time with same values as the first write, but with the Enable bit set to 0. This will keep the device from using the temporary configuration if a STORE_DEFAULT_ALL command is issued and a reset is performed.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Status	Out_Value	Out_Enable	Enable

This configuration is stored to nonvolatile memory with the STORE_DEFAULT_ALL command. If the pin is configured as an output, it can take a very short time after a reset or power-cycle for the pin to reach the configured state.

CAUTION

Configuring a pin that is also being used by another function (enable, fan control, etc) may QAlikely result in unexpected and unwanted behavior.

10.42 (FCh) MISC_CONFIG (MFR_SPECIFIC_44)

This Read/Write Block common command configures features not covered by other commands.

Table 68. MISC_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = FC
1	0		BYTE_COUNT = 8
2	1	0	Miscellaneous Configuration Byte
3	2	1	Time between Resequences
4	3	2	External Reference Voltage(low byte)
5	4	3	External Reference Voltage(high byte)
6	5	4	Resequence_rails_mask(low byte)
7	6	5	Resequence_rails_mask(middle low byte)
8	7	6	Resequence_rails_mask(middle high byte)
9	8	7	Resequence_rails_mask(high byte)

10.42.1 Miscellaneous Configuration Byte

The bit definitions for the Miscellaneous Configuration Byte are shown in Table 69.

Table 69. Miscellaneous Configuration Byte

Bit(s)	Name	Description
7	Resequence Continuously	When this bit is set, there is no limit to the number of times that the device will attempt to resequence. The “Max Resequences” value does not apply.
6	Resequence Abort	If a rail fails to turn off during re-sequencing, stop the re-sequencing operation
5:4	Max resequences	The maximum number of times to attempt to resequence. b'00 – 1 time b'01 – 2 times b'10 – 3 times b'11 – 4 times See Section 10.23.2 for more information.
3	Slave	When this bit is set, the device is a slave to take external sync clock. This bit is only valid if it is under multi-chip user case.
2	Enable Log FIFO	When this bit is set, all or part of the LOGGED_FAULT_DETAIL is treated as a FIFO, depending on the “FIFO Entire Log” bit.
1	External ADC Reference	When this bit is set, the external ADC reference (2.4v-3.0v) is used for ADC, see External Reference Voltage 10.41.3. A device reset is required after this bit is changed1.
0	Reserved	

NOTE: It is application’s responsibility to make sure external reference is in place before setting this bit. Otherwise ADC results maybe unpredicted.

10.42.2 Time Between Resequences

This byte is formatted according to Section 2.5.

10.42.3 External Reference Voltage

This field defines the external ADC reference voltage and it follows LINEAR format defined in Section 2.2. The reference voltage should be between 2.4V and 3V with 0.01V resolution.

10.42.4 Resequence_rails_mask

The page mask is made up of four bytes whose bits are defined as follows:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PAGE 31	PAGE 30	PAGE 29	PAGE 28	PAGE 27	PAGE 26	PAGE 25	PAGE 24	PAGE 23	PAGE 22	PAGE 21	PAGE 20	PAGE 19	PAGE 18	PAGE 17	PAGE 16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGE 15	PAGE 14	PAGE 13	PAGE 12	PAGE 11	PAGE 10	PAGE 9	PAGE 8	PAGE 7	PAGE 6	PAGE 5	PAGE 4	PAGE 3	PAGE 2	PAGE 1	PAGE 0

Each bit selects which page(s) should be not checked its POWER_GOOD_OFFf and TOFF_MAX_WARN status when performing resequences. When the corresponding page bit is set to 1, the resequence engine does not check its power_not_good and TOFF_WARN status. When the corresponding page bit is set to 0, the resequence checks its POWER_GOOD_OFF and TOFF_MAX_WARN status.

10.43 (FDh) DEVICE_ID (MFR_SPECIFIC_45)

This Read-only Block Read command returns an ASCII string up to 32 characters in length. It is broken into three or four sections, separated by the vertical bar character (‘|’). The format within each section may change in future releases; therefore, support tools must not rely on specific byte alignment. Instead they must identify the sections and sub-sections using the vertical bar and the periods that separate them.

1. The first section is the hardware device ID (e.g., ‘UCD90xxx ”).
2. The second section contains the firmware version information. Its format is “A.BB.C.DDDD”, where:

   A = Major Release Level (1 character)

BB = Minor Release Level (2 characters)

C = Sub-release (1 character)

DDDD = Build Number (4 characters)

The major and minor release numbers are incremented immediately after each official firmware release.

The sub-release field allows for branching off the main development path to build updates based on older versions.

The build number is automatically updated every time firmware is compiled. The value does not reset to 0 when the release level is updated. Several prerelease versions of firmware can have the same major, minor, and sub-release numbers. These different prerelease versions may be distinguished by the build number.

3. The third section contains the firmware compilation date. The date is reported in YYMMDD format, similar to the MFR_DATE command.
4. The optional fourth section may contain device-specific info.

Example: A typical DEVICE_ID string is `UCD90320|3.00.0.3029|160915`. In this example,

Hardware device = UCD90320

Firmware Major Release = 3

Firmware Minor Release = 00

Firmware Sub-Release = 0

Firmware Build Number = 3029

Firmware Build Date = September 15, 2016

11 Range Checking and Limits

Table 70 shows the numerical limits for all the supported PMBus commands.

Table 70. Range and Limits for PMBus Commands

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
0	PAGE	0	13 or 255	0	
1	OPERATION	See comments	See comments	0	The seven meaningful values for this parameter are 0x00, 0x40, 0x80, 0x94, 0x98, 0x98, 0xA4 and 0xA8.
2	ON_OFF_CONFIG	See comments	See comments	0	>0x20 invalid, all others accepted
3	CLEAR_FAULTS	n/a	n/a	n/a	Write Only
4	PHASE				Not Supported
05-0F	Reserved				
10	WRITE_PROTECT				Not Supported
11	STORE_DEFAULT_ALL	n/a	n/a	n/a	Write Only
12	RESTORE_DEFAULT_ALL	n/a	n/a	n/a	Write Only
13	STORE_DEFAULT_CODE				Not Supported
14	RESTORE_DEFAULT_CODE				Not Supported
15	STORE_USER_ALL				Not Supported
16	RESTORE_USER_ALL				Not Supported
17	STORE_USER_CODE				Not Supported
18	RESTORE_USER_CODE				Not Supported
19	CAPABILITY	n/a	n/a	0xB0	Read Only
1A	QUERY				Not Supported
1B-1F	Reserved				
20	VOUT_MODE	–16	15	0	Five-bit, two's complement exponent
21	VOUT_COMMAND	0	See comment	0	Depends on VOUT_MODE
22	VOUT_TRIM				Not Supported

Table 70. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
23	VOUT_CAL_OFFSET				Not Supported
24	VOUT_MAX				Not Supported
25	VOUT_MARGIN_HIGH	0	See comment	0	Depends on VOUT_MODE
26	VOUT_MARGIN_LOW	0	See comment	0	Depends on VOUT_MODE
27	VOUT_TRANSITION_RATE				Not Supported
28	VOUT_DROOP				Not Supported
29	VOUT_SCALE_LOOP				Not Supported
2A	VOUT_SCALE_MONITOR	0	See comment	0	Depends on VOUT_MODE
2B-2F	Reserved				
30	COEFFICIENTS				Not Supported
31	POUT_MAX				Not Supported
32	MAX_DUTY				Not Supported
33	FREQUENCY_SWITCH				Not Supported
34	Reserved				
35	VIN_ON				Not Supported
36	VIN_OFF				Not Supported
37	INTERLEAVE				Not Supported
38	IOUT_CAL_GAIN	0.6113	20000	0	A number from 20000 to 40031 results in 20000 because of internal resolution.
39	IOUT_CAL_OFFSET	–511.5	511.5	0	
3A	FAN_CONFIG_1_2				Not Supported
3B	FAN_COMMAND_1	0	100	0	
3C	FAN_COMMAND_2	0	100	0	
3D	FAN_CONFIG_3_4				Not Supported
3E	FAN_COMMAND_3	0	100	0	
3F	FAN_COMMAND_4	0	100	0	
40	VOUT_OV_FAULT_LIMIT	0	See comment	0	Depends on VOUT_MODE
41	VOUT_OV_FAULT_RESPONSE				See FAULT_RESPONSES command
42	VOUT_OV_WARN_LIMIT	0	See comment	0	Depends on VOUT_MODE
43	VOUT_UV_WARN_LIMIT	0	See comment	0	Depends on VOUT_MODE
44	VOUT_UV_FAULT_LIMIT	0	See comment	0	Depends on VOUT_MODE
45	VOUT_UV_FAULT_RESPONSE				See FAULT_RESPONSES command
46	IOUT_OC_FAULT_LIMIT	–511.5	511.5	0	
47	IOUT_OC_FAULT_RESPONSE				See FAULT_RESPONSES command
48	IOUT_OC_LV_FAULT_LIMIT				Not Supported
49	IOUT_OC_LV_FAULT_RESPONSE				Not Supported
4A	IOUT_OC_WARN_LIMIT	–511.5	511.5	0	
4B	IOUT_UC_FAULT_LIMIT	–511.5	511.5	0	
4C	IOUT_UC_FAULT_RESPONSE				See FAULT_RESPONSES command
4D	Reserved				
4E	Reserved				
4F	OT_FAULT_LIMIT	–255.75	255.75	0	
50	OT_FAULT_RESPONSE				See FAULT_RESPONSES command
51	OT_WARN_LIMIT	–255.75	255.75	0	
52	UT_WARN_LIMIT				Not Supported
53	UT_FAULT_LIMIT				Not Supported
54	UT_FAULT_RESPONSE				Not Supported
55	VIN_OV_FAULT_LIMIT				Not Supported
56	VIN_OV_FAULT_RESPONSE				Not Supported
57	VIN_OV_WARN_LIMIT				Not Supported
58	VIN_UV_WARN_LIMIT				Not Supported

Table 70. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
59	VIN_UV_FAULT_LIMIT				Not Supported
5A	VIN_UV_FAULT_RESPONSE				Not Supported
5B	IIN_OC_FAULT_LIMIT				Not Supported
5C	IIN_OC_FAULT_RESPONSE				Not Supported
5D	IIN_OC_WARN_LIMIT				Not Supported
5E	POWER_GOOD_ON	0	See comment	0	Depends on VOUT_MODE
5F	POWER_GOOD_OFF	0	See comment	0	Depends on VOUT_MODE
60	TON_DELAY	0	3276	0	
61	TON_RISE				Not Supported
62	TON_MAX_FAULT_LIMIT	0	3276	0	
63	TON_MAX_FAULT_RESPONSE				See FAULT_RESPONSES command
64	TOFF_DELAY	0	3276	0	
65	TOFF_FALL				Not Supported
66	TOFF_MAX_WARN_LIMIT	0	3276 or 0x7FFF	0	0x7FFF is a special value meaning there is no limit. See section 16.7 of the PMBus Specification.
67	Reserved				
68	POUT_OP_FAULT_LIMIT				Not Supported
69	POUT_OP_FAULT_RESPONSE				Not Supported
6A	POUT_OP_WARN_LIMIT				Not Supported
6B	PIN_OP_WARN_LIMIT				Not Supported
6C-77	Reserved				
78	STATUS_BYTE				Read Only
79	STATUS_WORD				Read Only
7A	STATUS_VOUT				Read Only
7B	STATUS_IOUT				Read Only
7C	STATUS_INPUT				Not Supported
7D	STATUS_TEMPERATURE				Read Only
7E	STATUS_CML				Read Only
7F	STATUS_OTHER				Not Supported
80	STATUS_MFR_SPECIFIC				Not Supported
81	STATUS_FANS_1_2				Read Only
82	STATUS_FANS_3_4				Read Only
83-87	Reserved				
88	READ_VIN				Not Supported
89	READ_IIN				Not Supported
8A	READ_VCAP				Not Supported
8B	READ_VOUT				Read Only
8C	READ_IOUT				Read Only
8D	READ_TEMPERATURE_1				Read Only
8E	READ_TEMPERATURE_2				Read Only
8F	READ_TEMPERATURE_3				Not Supported
90	READ_FAN_SPEED_1	0	32767	0	Read Only
91	READ_FAN_SPEED_2	0	32767	0	Read Only
92	READ_FAN_SPEED_3	0	32767	0	Read Only
93	READ_FAN_SPEED_4	0	32767	0	Read Only
94	READ_DUTY_CYCLE				Not Supported
95	READ_FREQUENCY				Not Supported
96	READ_POUT				Not Supported
97	READ_PIN				Not Supported
98	PMBUS_REVISION				Read Only

Table 70. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
99	MFR_ID	n/a	n/a	See comment	The default is an empty string, all zeros
9A	MFR_MODEL	n/a	n/a	See comment	The default is an empty string, all zeros
9B	MFR_REVISION	n/a	n/a	See comment	The default is an empty string, all zeros
9C	MFR_LOCATION	n/a	n/a	See comment	The default is an empty string, all zeros
9D	MFR_DATE	n/a	n/a	See comment	The default is an empty string, all zeros
9E	MFR_SERIAL	n/a	n/a	See comment	The default is an empty string, all zeros
9F	Reserved				
A0	MFR_VIN_MIN				Not Supported
A1	MFR_VIN_MAX				Not Supported
A2	MFR_IIN_MAX				Not Supported
A3	MFR_PIN_MAX				Not Supported
A4	MFR_VOUT_MIN				Not Supported
A5	MFR_VOUT_MAX				Not Supported
A6	MFR_IOUT_MAX				Not Supported
A7	MFR_POUT_MAX				Not Supported
A8	MFR_TAMBIENT_MAX				Not Supported
A9	MFR_TAMBIENT_MIN				Not Supported
AA-AF	Reserved				
B0-BF	USER_DATA_00 -USER_DATA_15				Not Supported
C0-CF	Reserved				
D0	SEQ_TIMEOUT(MFR_SPECIFIC_00)	0	3276	0	
D1	VOUT_CAL_MONITOR (MFR_SPECIFIC_01)	See comment	See comment	0	Depends on VOUT_MODE (Note this parameter is treated as a SIGNED variable)
D2	SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)	n/a	n/a	0	
D3	SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)	n/a	n/a	0	
D4	SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)	n/a	n/a	0	
D5	MONITOR_CONFIG (MFR_SPECIFIC_05)	n/a	n/a	0	
D6	NUM_PAGES (MFR_SPECIFIC_06)	0	Device dependent	0	Read Only
D7	RUN_TIME_CLOCK (MFR_SPECIFIC_07)	n/a	n/a	0	
D8	RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)	n/a	n/a	0	
D9	ROM_MODE (MFR_SPECIFIC_09)	n/a	n/a	n/a	Write Only
DA	USER_RAM_00 (MFR_SPECIFIC_10)	0	255	0	
DB	SOFT_RESET (MFR_SPECIFIC_11)	n/a	n/a	n/a	Write Only
DC	RESET_COUNT (MFR_SPECIFIC_12)	0	65535	0	
DD	PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)	n/a	n/a	0	
DE	RESEQUENCE (MFR_SPECIFIC_14)	0	0xFFFF	n/a	Write Only
DF	CONSTANTS (MFR_SPECIFIC_15)	n/a	n/a	n/a	Read Only
E0	PWM_SELECT (MFR_SPECIFIC_16)	0	12	0	
E1	PWM_CONFIG (MFR_SPECIFIC_17)	n/a	n/a	0	
E2	PARM_INFO (MFR_SPECIFIC_18)	n/a	n/a	0	Index is checked to verify that it points to a valid base address
E3	PARM_VALUE (MFR_SPECIFIC_19)	n/a	n/a	0	

Table 70. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
E4	TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)	–1638	1638	0	
E5	TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)	–255.75	255.75	0	
E6	(MFR_SPECIFIC_22)				
E7	FAN_CONFIG_INDEX (MFR_SPECIFIC_23)	0	3	0	
E8	FAN_CONFIG (MFR_SPECIFIC_24)	n/a	n/a	0	
E9	FAULT_RESPONSES (MFR_SPECIFIC_25)	n/a	n/a	0	
EA	LOGGED_FAULTS (MFR_SPECIFIC_26)	n/a	n/a	n/a	Only valid write is all zeroes.
EB	LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)	0	Device dependent	0	
EC	LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)	n/a	n/a	0	Read Only
ED	LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)	n/a	n/a	0	Only valid write is all zeroes.
EE	LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)	n/a	n/a	0	Only valid write is all zeroes.
EF	LOGGED_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)	n/a	n/a	See comment	All logging is enabled by default
F0	EXECUTE_FLASH (MFR_SPECIFIC_32)	n/a	n/a	0	Write Only
F1	SECURITY (MFR_SPECIFIC_33)	n/a	n/a	See comment	Default password is 0xFFFFFFFFFFFF - security is disabled
F2	SECURITY_BIT_MASK (MFR_SPECIFIC_34)	n/a	n/a	n/a	Default bit mask is to have no commands secured.
F3	MFR_STATUS (MFR_SPECIFIC_35)	n/a	n/a	0	
F4	GPI_FAULT_RESPONSES (MFR_SPECIFIC_36)	n/a	n/a	0	
F5	MARGIN_CONFIG (MFR_SPECIFIC_37)	n/a	n/a	0	
F6	SEQ_CONFIG (MFR_SPECIFIC_38)	n/a	n/a	0	
F7	GPO_CONFIG_INDEX (MFR_SPECIFIC_39)	0	12	0	
F8	GPO_CONFIG (MFR_SPECIFIC_40)	n/a	n/a	0	
F9	GPI_CONFIG (MFR_SPECIFIC_41)	n/a	n/a	0	
FA	GPIO_SELECT (MFR_SPECIFIC_42)	0	n/a	0	
FB	GPIO_CONFIG (MFR_SPECIFIC_43)	n/a	n/a	0	
FC	MISC_CONFIG (MFR_SPECIFIC_44)	n/a	n/a	0	
FD	DEVICE_ID (MFR_SPECIFIC_45)	n/a	n/a	Device dependent	
FE	Mfr_Specific_Extended_Command				Not Supported
FF	PMBUS_Extended_Command				Not Supported

12 Glossary

Term	Description	Behavior
ACK	Acknowledge	Indicates that the PMBus has received the message correctly.
ADC	Analog-to-digital converter	Converts analog voltages to digital counts that may be used for monitoring or control.
DAC	Digital-to-analog converter	
DFlash	Data Flash memory	Nonvolatile memory used for storing PMBus settings. The values in DFlash are automatically copied to RAM during wakeup.
FPWM	Fast pulse width modulation pin	These pins are capable of a higher frequency than the other PWM pins.
GPI	General-purpose input	
GPIO	General-purpose input/output	
GPO	General-purpose output	
NACK	Non-acknowledge	An error has occurred in the PMBus message transfer.
PFlash	Program Flash memory	Nonvolatile memory used for the UCD90xxx main firmware.
PMBus	Power management bus	An open-standard protocol that defines a means of communicating with power conversion devices using an I^2C physical interface.
PWM	Pulse width modulation or pulse width modulator	
RAM	Random access memory	Volatile memory used to hold PMBus settings and internal variables. PMBus settings are lost after a reset unless they are stored to Data Flash.
ROM	Read-only memory	Nonvolatile memory used for the UCD90xxx boot algorithms and some common data tables.

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