



Product Change Notification / SYST-23RZAZ634

Date:

24-Nov-2021

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAM L22 Datasheet

Affected CPNs:

[SYST-23RZAZ634_Affected_CPN_11242021.pdf](#)

[SYST-23RZAZ634_Affected_CPN_11242021.csv](#)

Notification Text:

SYST-23RZAZ634

Microchip has released a new Product Documents for the SAM L22 Datasheet of devices. If you are using one of these devices please read the document located at [SAM L22 Datasheet](#).

Notification Status: Final

Description of Change:1. General:

- The SPI, I2S, and I2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.
- This revision contains numerous typographical updates, and formatting updates. Large sections of this data sheet were rewritten to conform to updated standards.
- Updated the Product Identification System to remove an erroneous table.

2. Pinout:

- Updated the UFBGA100 Pinout by replacing VSW0 with VDDOUT

3. Power Supply and Startup Considerations

- Updated numerous cross references to point to the correct chapters or sections
- Added notes to the figures in Typical Powering Schematic

4. Memories- Updated numerous cross references to point to the correct chapters or sections
- Updated the table in NVM Software Calibration Area Mapping

5. PAC
- Updated numerous cross references to point to the correct chapters or sections

6. DSU- Updated numerous cross references to point to the correct chapters or sections

7. Clock System- Updated numerous cross references to point to the correct chapters or sections- Updated the 14.1. Clock Distribution converting DPLL to FDPLL

8. GCLK- Updated numerous cross references to point to the correct chapters or sections
- Updated the PCHCTRLM Register with new information for bitfield output

9. MCLK
- Updated numerous cross references to point to the correct chapters or sections
- Updated the following registers with new reset values or bitfield information:
– INTFLAG
– CPUDIV
– APBAMASK
– APBCMASK

10. FREQM
- Updated numerous cross references to point to the correct chapters or sections

11. RSTC
- Updated numerous cross references to point to the correct chapters or sections

12. OSCCTRL
- Updated numerous cross references to point to the correct chapters or sections
- Updated Features with missing information regarding Clock Failure Detection

13. OSC32KCTRL
- Updated numerous cross references to point to the correct chapters or sections

14. SUPC
- Updated numerous cross references to point to the correct chapters or sections
- Updated Sleep Mode Operation with new text and links
- Updated the following registers with new reset values:
– INTFLAG
– STATUS

15. WDT
- Updated numerous cross references to point to the correct chapters or sections
- Updated the following Registers:
– CTRLA
– CONFIG
– EWCTRL

16. RTC
- Updated numerous cross references to point to the correct chapters or sections- Added new line items to Features for Backup Registers and Tamper Detection
- Updated Events with new information for TAMPER
- Updated Interrupts with new information for TAMPEV
- Updated Sleep Mode Operation with a new paragraph
- Updated the following Registers with proper naming conventions or new notes:
– COUNT32 Mode COUNT
– COUNT32 Mode GPn

- COUNT32 Mode 24.8.16. BKUPn
- COUNT16 Mode COMPn
- COUNT16 Mode 24.8.16. BKUPn
- COUNT16 Mode GPn
- Clock mode BKUPn
- Clock mode GPn

17. DMAC

- Updated numerous cross references to point to the correct chapters or sections
- Updated the following Registers:
 - DSTADDR
 - SRCADDR

18. EIC

- Updated numerous cross references to point to the correct chapters or sections
- Updated the CONFIGn register with a naming correction

19. NVMCTRL

- Updated numerous cross references to point to the correct chapters or sections
- Updated the Block Diagram with a new image

- The following Registers had updates to the Register reset values, minor textual updates, or reset values for the bitfields within:
 - CTRLB
 - PARAM
 - STATUS
 - LOCK

20. PORT

- Updated numerous cross references to point to the correct chapters or sections
- Updated the Functional Description with a new diagram for Overview of the PORT, and added a new note

- The following registers were updated with new naming:
 - PMUXn
 - PINCFGn

- The following registers were updated with new notes:
 - DIR - DIRCLR
 - DIRSET
 - DIRTGL
 - OUT
 - OUTCLR
 - OUTSET
 - OUTTGL
 - IN
 - CTRL
 - WRCONFIG
 - EVCTRL
 - PMUXn
 - PINCFGn

21. EVSYS

- Updated numerous cross references to point to the correct chapters or sections

22. SERCOM

- Updated numerous cross references to point to the correct chapters or sections

- 23. SERCOM SPI- Updated numerous cross references to point to the correct chapters or sections

24. SERCOM I²C

- Updated numerous cross references to point to the correct chapters or sections
- Updated the bitfield accesses in the following registers:
 - CTRLB

25. TCC

- Updated the text in Double Buffering to better describe the PATT, PER and CCx Registers
- Updated TCCx to read TCC0 throughout the chapter
- Corrected non-functional cross references throughout the chapter
- Updated the naming of the CCBUFn Register

26. TRNG

- Updated the bitfield access for the DATA register

27. AES

- Updated the register naming in GCM Operation
- Updated the naming for the following registers:
 - KEYWORDn
 - INTVECTVn
 - HASHKEYn
 - GHASHn
 - CIPLN

28. CCL

- Updated the Block Diagram
- Updated the Event Input Selection figure and the Linked LUT Input Selection figure in Truth Table Inputs Selection
- Updated the naming for the following registers:
 - SEQCTRLn
 - LUTCTRLn

29. ADC

- Updated Interrupts with new text for the RESRDY and WINMON bitfields

30. AC

- Updated VDD Scaler with new text
- Updated the VDD Scaler Diagram with new values for MUXPOS and MUXNEG

31. PTC

- Added in Analog-to-Digital Converter section

32. Electrical Characteristics

- Updated the Maximum Peripheral Clock Frequencies table with minor typographical corrections
- Updated the Active Current Consumption table in Power Consumption with a new Ta column
- Removed an erroneous equation from the Single-Ended Mode table in Analog-to-Digital (ADC) Characteristics

33. Schematic Checklist

- Added the External Reset Circuit Schematic (EFT Immunity Enhancement) figure and a new note to External Reset Circuit

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 24 Nov 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[SAM L22 Datasheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATSAML22G16A-AUT
ATSAML22G16A-MUT
ATSAML22G17A-AUT
ATSAML22G17A-MUT
ATSAML22G17A-UUT
ATSAML22G17A-UUTA0
ATSAML22G17A-UUTA1
ATSAML22G17A-UUTA2
ATSAML22G18A-AUT
ATSAML22G18A-MUT
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ATSAML22N18A-CFUT