CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7131/CMX7141 Digital PMR Processor dPMR® Mode 1, 2 and 3

D/7131/7141_FI7.x/5 September 2013

DATASHEET

Advance Information

7131/7141FI-7.x: dPMR® Baseband Data Processor with Auxiliary System Clocks, ADCs and DACs

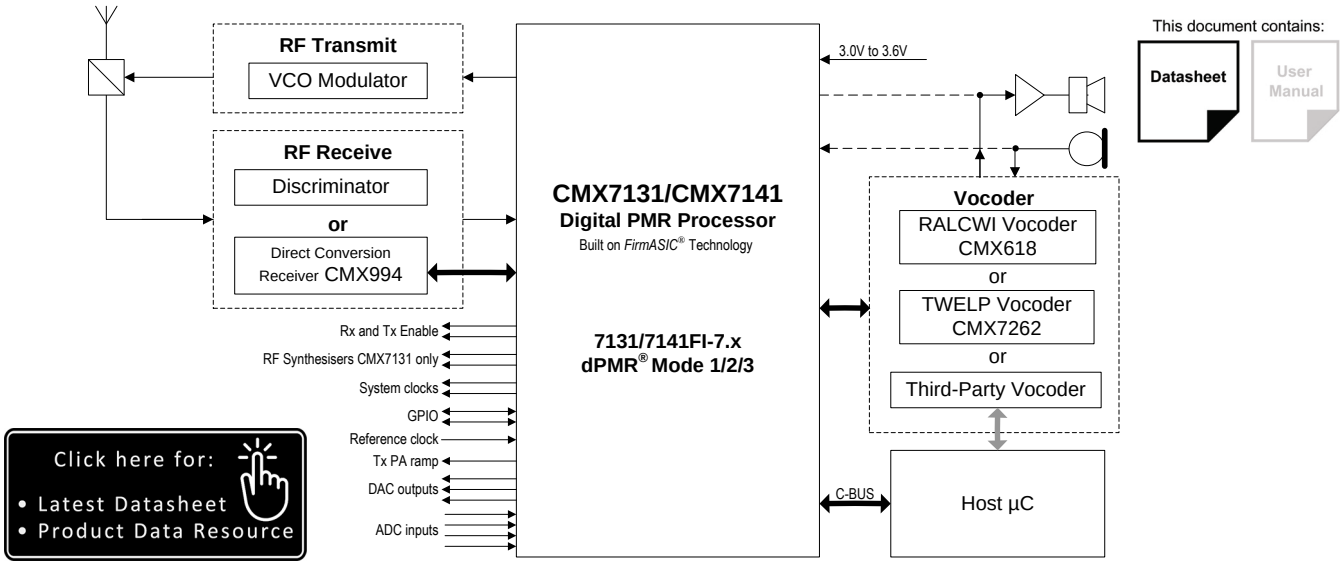
Features

- Digital PMR
  - dPMR® (ETSI TS 102 658) Compliant
  - Air Interface Physical Layer (Layer 1)
  - Air Interface Data Link Layer (Layer 2)
  - Mode 1: peer-to-peer mode *
  - Mode 2: peer-to-peer mode with repeater operation *
  - Mode 3: trunked mode support *
    - * Voice supported in all modes
    - * Type 1, Type 2 and Type 3 Data modes
- Tx Sequencer – automatic execution of transmit actions when the device is placed in Tx mode.
- 4FSK Modem
  - 4.8kbps Data Rate
  - Soft-decision Data Output Option
  - AFSD (Automated Frame Sync Detection)

Additional Features

- 2 Auxiliary ADCs (4 Multiplexed Inputs)
- 4 Auxiliary DACs
- 2 Auxiliary System Clock Outputs
- Tx Outputs for Two-point or I/Q Modulation
- Rx Inputs for CMX994 Direct Conversion (I/Q) Receiver
- C-BUS serial interface to CMX994 transceiver
- 2 RF Synthesisers (CMX7131 only)

- Vocoder Connectivity
  - Vocoder Management and Control
  - FI-7.2.x: RALCWI Vocoders CMX608/618
  - FI-7.3.x: TWELP Vocoder CMX7262
- Voice Codec supports External Vocoder (SPI/PCM/I²S compatible - e.g. AMBE3000)
- C-BUS Serial Interface to Host micro
- Flexible Powersave Modes
- Low-power (3.3V) Operation
- Available in LQFP or VQFN Packages



1 Brief Description

The 7131/7141FI-7.x Function Image™ (FI) implements a half-duplex 4FSK modem and a large proportion of the dPMR® Air Interface, Data Link and Call Control layers. In conjunction with a suitable host and a limiter/discriminator-based RF transceiver or CMX994 Direct Conversion (I/Q) Receiver, a compact, low-cost, low-power digital PMR radio conforming to ETSI's dPMR® standard TS 102 658 can be realised. The 7131/7141FI-7.x has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default and is compatible with 7131/7141FI-7.0 for conventional limiter/discriminator receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. Dual mode, analogue/digital PMR operation can also be achieved with the CMX7131/CMX7141 by re-loading the device with 7031/7041FI-1.x for LD RF designs or 7131/7141FI-8.x for radios using I/Q interfacing.

The embedded functionality of the CMX7131/CMX7141 (7131/7141FI-7.x), managing voice and data systems autonomously, including CMX6x8 or CMX7262 Vocoder control (via the Auxiliary SPI/C-BUS interface), minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a dPMR® radio. The CMX7131/CMX7141 can also provide audio codec functionality for vocoders under direct host control.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host microcontroller over the built-in C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7131/7141FI-7.x.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). Additionally the CMX7131 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover.

The CMX7141 is identical in functionality to the CMX7131 with the exception that the two on-chip RF synthesisers have been deleted, which enables it to be supplied in a smaller package. This document refers to both parts, unless otherwise stated.

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This datasheet is the first part of a two-part document comprising datasheet and user manual: the user manual can be obtained by registering your interest in this product with your local CML representative.

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Table Page

Figure Page

History

Version	Changes	Date
5	• Support CMX7262 control • Add Tx Level Adjust to $C3:2xxx • Added note on BOOTEN pins for CMX994 operation • Corrected errors in Figures 1 and 6, Table 3 tidied up. • Added support for Type-3 Packet Data • Added Tx Test Mode “repeated word” using $C1 = $0062	Sept 2013
4	• CMX994 Pass-through mode added in section 6.6.19. • Changed the operation of the Repeat Headers function to use the Tx_AuxData register, to allow more flexibility in specifying the MI field of the Header Block. Applicable to FI-7.1.2.x onwards. • Updated for FI-7.1.2.x, which improves the support for an I/Q interface. • Updated RAMDAC, tone generator and AGC I/Q Mode descriptions, see Figure 6 and sections 5.2.7, 8.1.4 and 8.2.3. • Added RSSI - signal strength graph for I/Q mode and section 5.2.8. • Updated data formats in section 6.7.3. • Various typographical and editorial changes	Mar 2013
3	• Datasheet/User Manual updated for FI-7.1.x which adds support for an I/Q interface to existing functionality.	Sept 2012
2	• Further clarification on Mode 3 operation added • Information on Receive Pass-through mode added to section 6.6.14 • Information on support for I^2S mode added to section 6.5.2 • Various typographical and editorial changes	June 2012
1	• Original document	Feb 2012

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

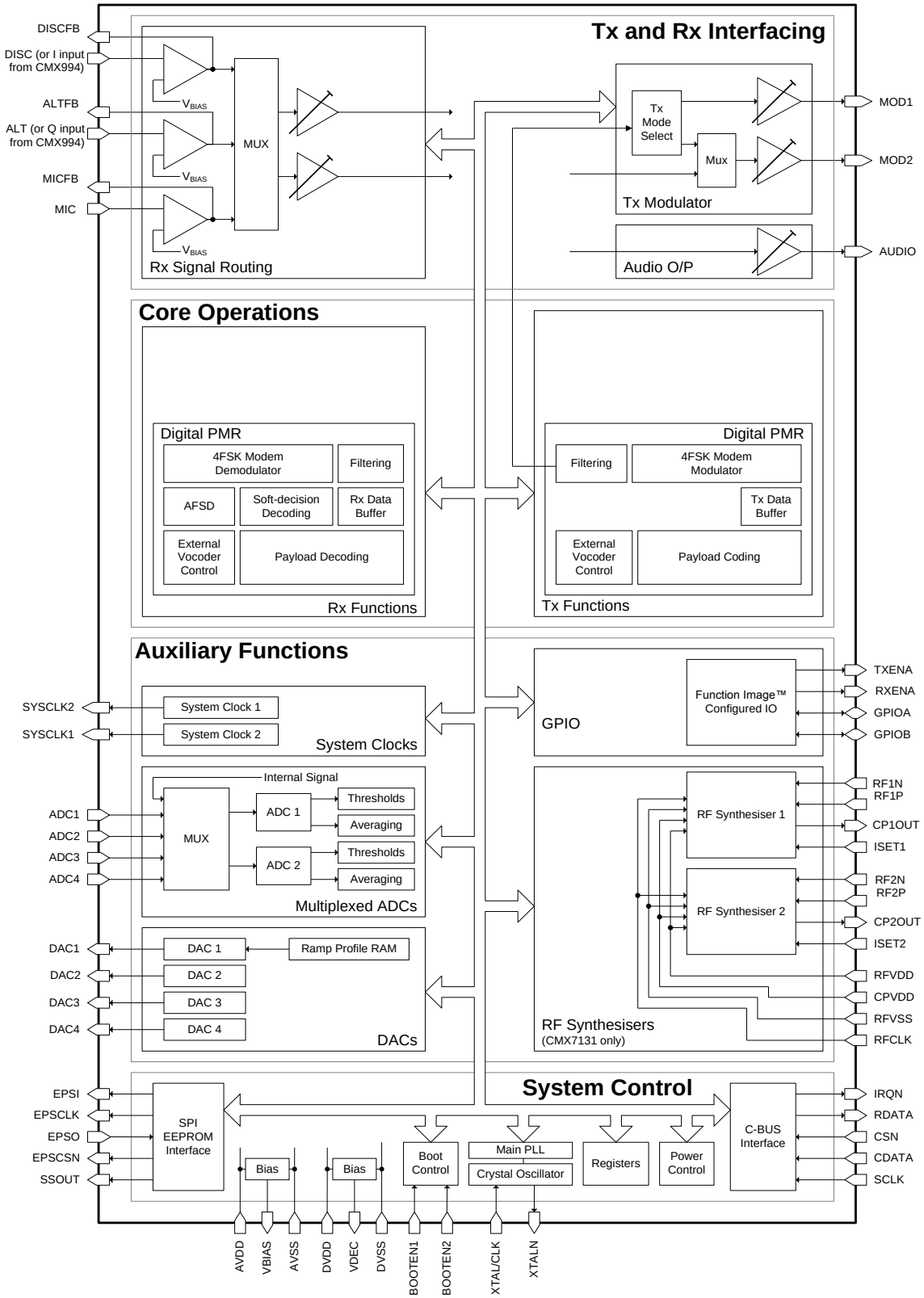


Figure 1 Block Diagram

3 Signal List

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser 1 Negative Input
3	-	RF1P	IP	RF Synthesiser 1 Positive Input
4	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 1
5	-	CP1OUT	OP	RF Synthesiser 1 Charge Pump output
6	-	ISET1	IP	RF Synthesiser 1 Charge Pump Current Set input
7	-	RFVDD	PWR	The 2.5V positive supply rail for both RF Synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser 2 Negative Input
9	-	RF2P	IP	RF Synthesiser 2 Positive Input
10	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 2
11	-	CP2OUT	OP	RF Synthesiser 2 Charge Pump output
12	-	ISET2	IP	RF Synthesiser 2 Charge Pump Current Set input
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF Synthesiser charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both RF Synthesisers)[1]
15	**11**	GPIOA	OP	General Purpose I/O pin
16	**12**	GPIOB	OP	General Purpose I/O pin
17	-	-	NC	*Reserved* – do not connect this pin
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1
21	**14**	DVSS	PWR	Digital ground
22	-	-	NC	*Reserved* – do not connect this pin
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISC	IP	Discriminator inverting input or I input from CMX994
25	**17**	DISCFB	OP	Discriminator input amplifier feedback
26	**18**	ALT	IP	Alternate inverting input or Q input from CMX994

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLK input.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description	
27	**19**	ALTFB	OP	Alternate input amplifier feedback	
28	**20**	MICFB	OP	Microphone input amplifier feedback	
29	**21**	MIC	IP	Microphone inverting input	
30	**22**	AVSS	PWR	Analogue ground	
31	**23**	MOD1	OP	Modulator 1 output	
32	**24**	MOD2	OP	Modulator 2 output	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	Audio Output in SPI-Codec mode	
35	**27**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 6.10 for details.
36	**28**	ADC2	IP	Auxiliary ADC input 2	
37	**29**	ADC3	IP	Auxiliary ADC input 3	
38	**30**	ADC4	IP	Auxiliary ADC input 4	
39	**31**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
41	**33**	DAC2	OP	Auxiliary DAC output 2	
42	**34**	AVSS	PWR	Analogue ground	
43	**35**	DAC3	OP	Auxiliary DAC output 3	
44	**36**	DAC4	OP	Auxiliary DAC output 4	
-	**37**	DVSS	PWR	Digital Ground	
45	**38**	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
48	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS Command Data: Serial data input from the µC	
50	**43**	RDATA	TS OP	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	
51	-	-	NC	*Reserved* – do not connect this pin	

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
53	**44**	SSOUT	OP	SPI bus Chip Select/Frame Sync (used for CMX6x8 or CMX7262)
52	**45**	DVSS	PWR	Digital ground
54	**46**	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	**48**	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input
57	-	-	NC	*Reserved* – do not connect this pin
58	**1**	EPSI	OP	CMX994 or Serial Memory Interface: Output; SPI bus Output
59	**2**	EPSCLK	OP	CMX994 or Serial Memory Interface: Clock; SPI bus Clock
60	**3**	EPSO	IP+PD	CMX994 or Serial Memory Interface: Input; SPI bus Input
61	**4**	EPSCSN	OP	CMX994 or Serial Memory Interface: Chip Select
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program
64	**7**	DVSS	PWR	Digital ground
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pullup **/** pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{DD}	RFVDD	Power supply for RF circuits
RFV_{SS}	RFVSS	Ground for RF circuits
CPV_{DD}	CPVDD	Power supply for charge pump circuits

4 Component and PCB Recommendations

4.1 Recommended External Components

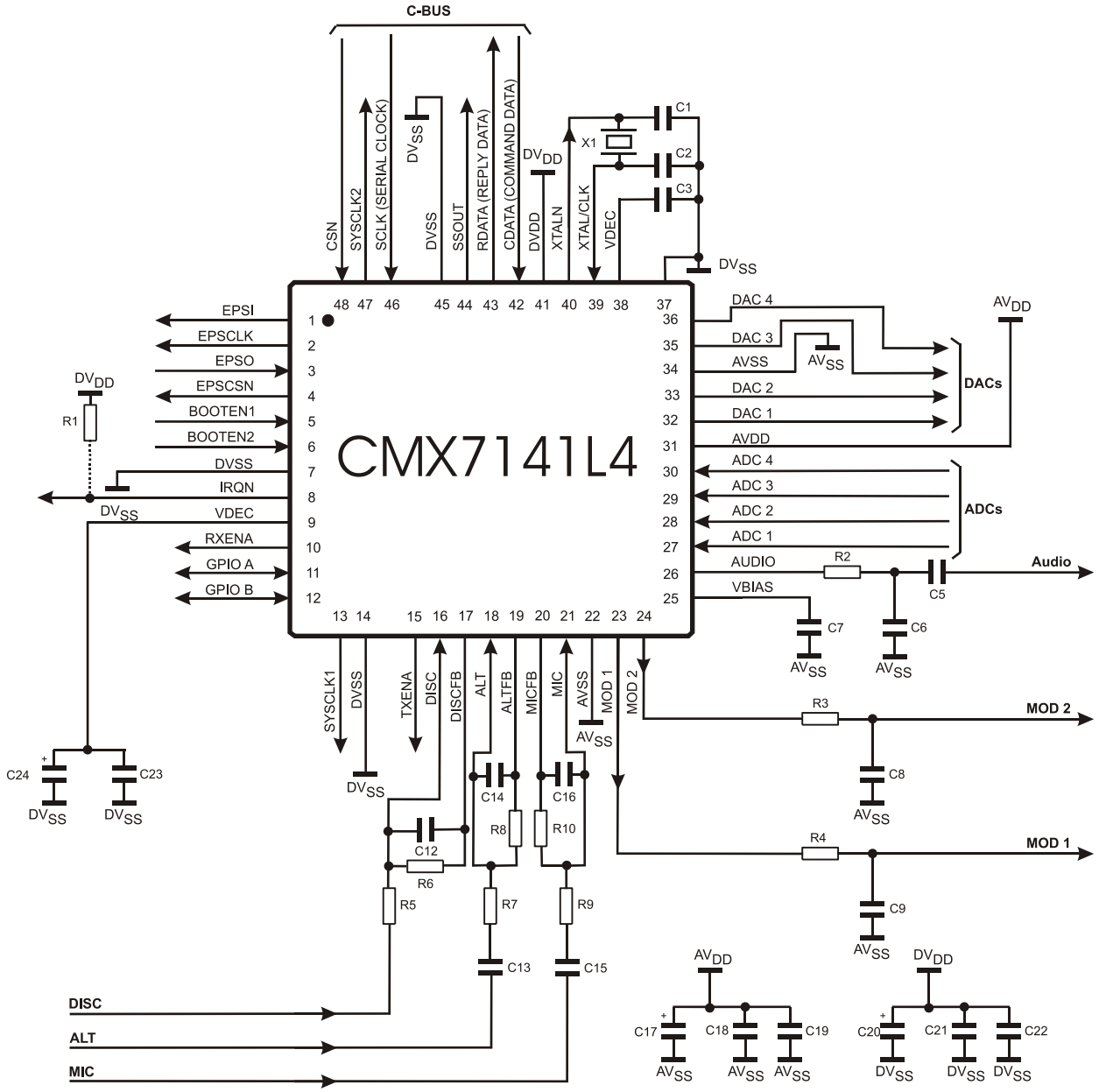


Figure 2 CMX7141 (L4 and Q3) Recommended External Components

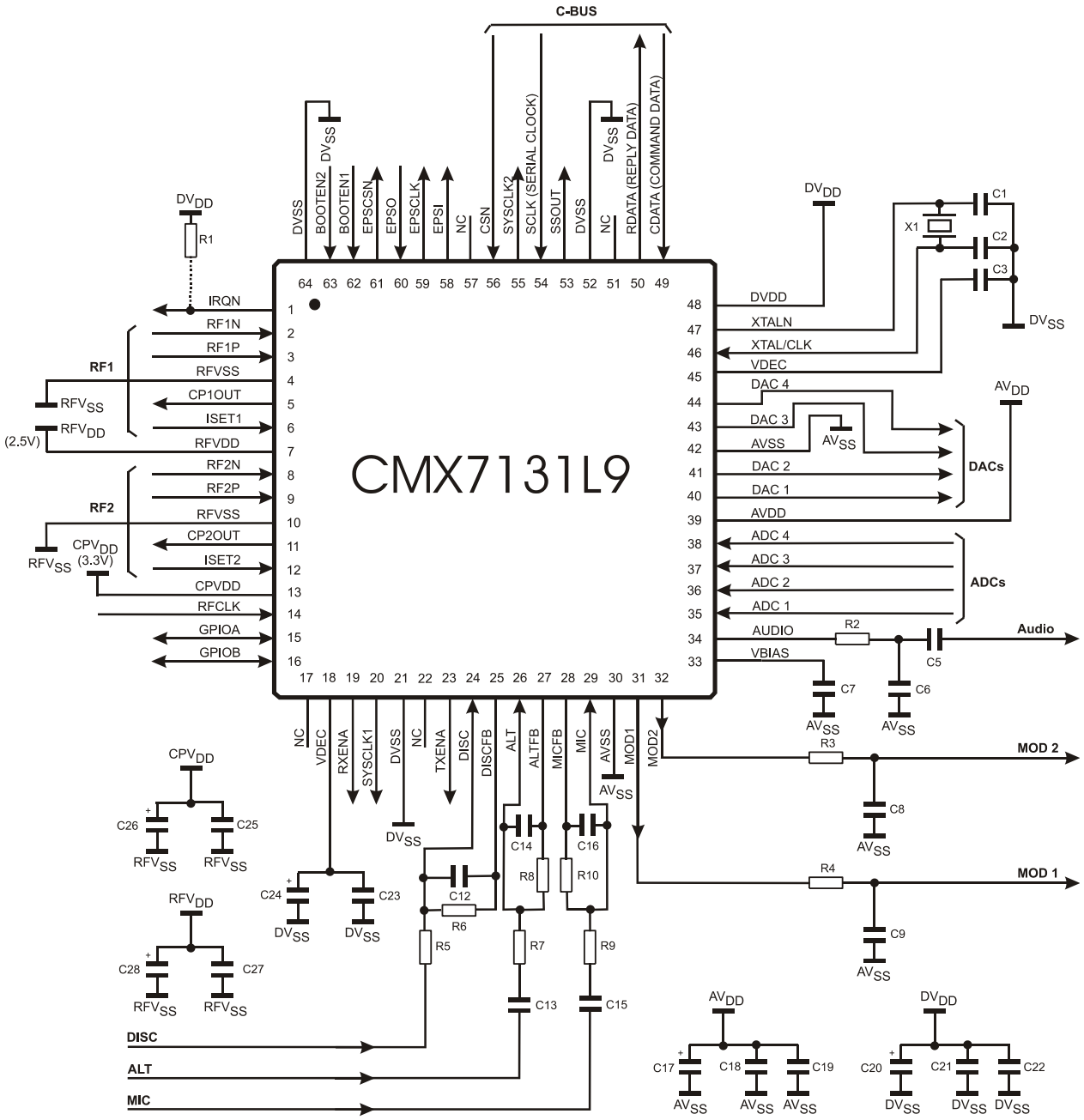


Figure 3 CMX7131 (L9 and Q1) Recommended External Components

Table 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	20kΩ	C2	18pF	C12	100pF	C22	10nF
R3	20kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	20kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	200pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	6.144MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 6.14.2. For 4FSK modulation, this signal should be dc coupled from the Limiter/ Discriminator output.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.14.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.14.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC and ALT inputs as follows:

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$
$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. AUDIO output is used when SPI-Codec mode has been selected.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

4.2 PCB Layout Guidelines and Power Supply Decoupling

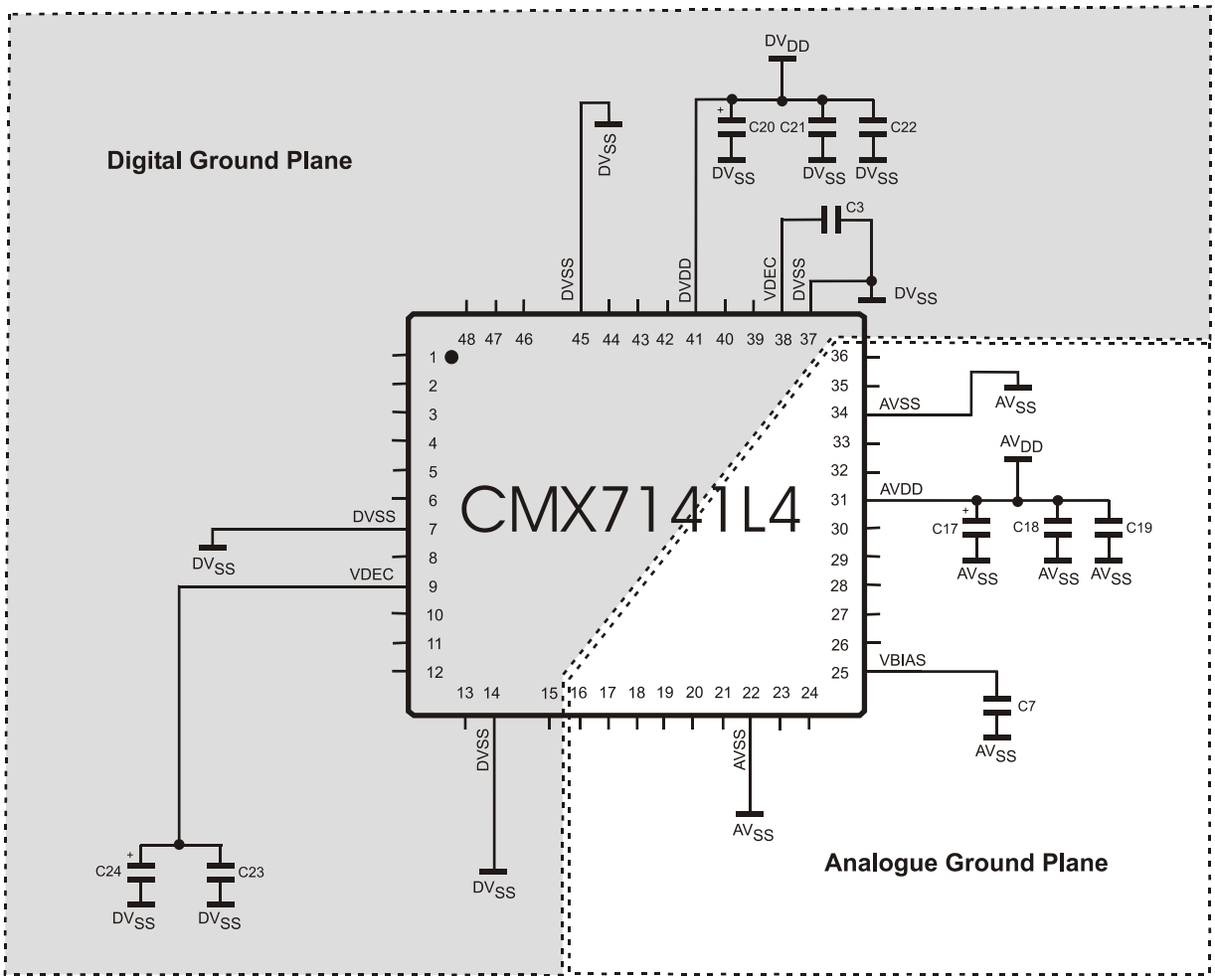


Figure 4 CMX7141 (L4/Q3) Power Supply and De-coupling

Component Values as per Figure 2

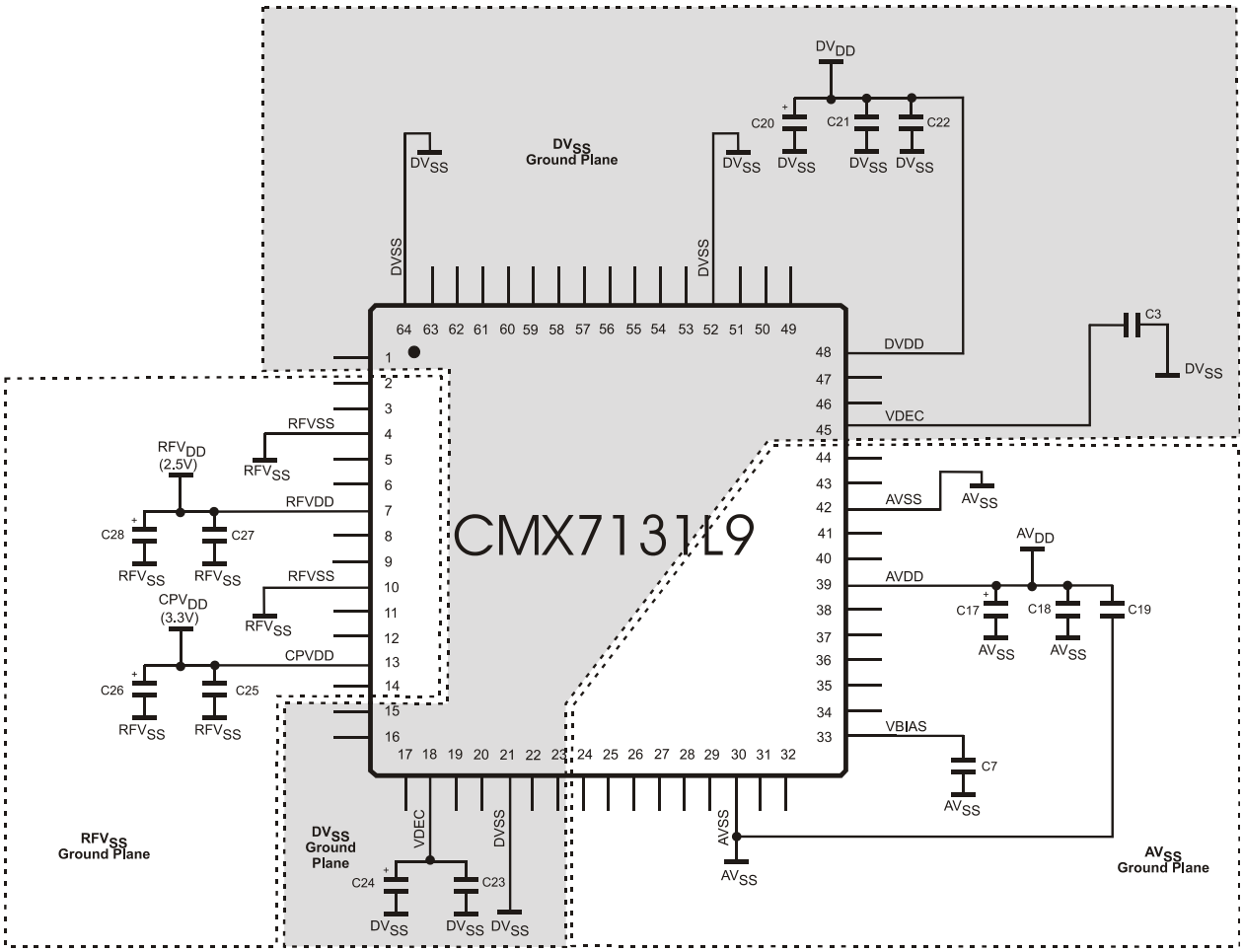


Figure 5 CMX7131 (L9/Q1) Power Supply and De-coupling

Component Values as per Figure 3

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7131/CMX7141 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7131/CMX7141. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7131/CMX7141, with provision to make links between them, close to the CMX7131/CMX7141. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it should be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

4.3 CMX994 Interface

When operating the 7131/7141FI-7.x in I/Q mode, the interface to the CMX994 shown in Figure 6 should be used. Component values are shown in Table 3, where values are not shown then refer to the CMX994 datasheet.

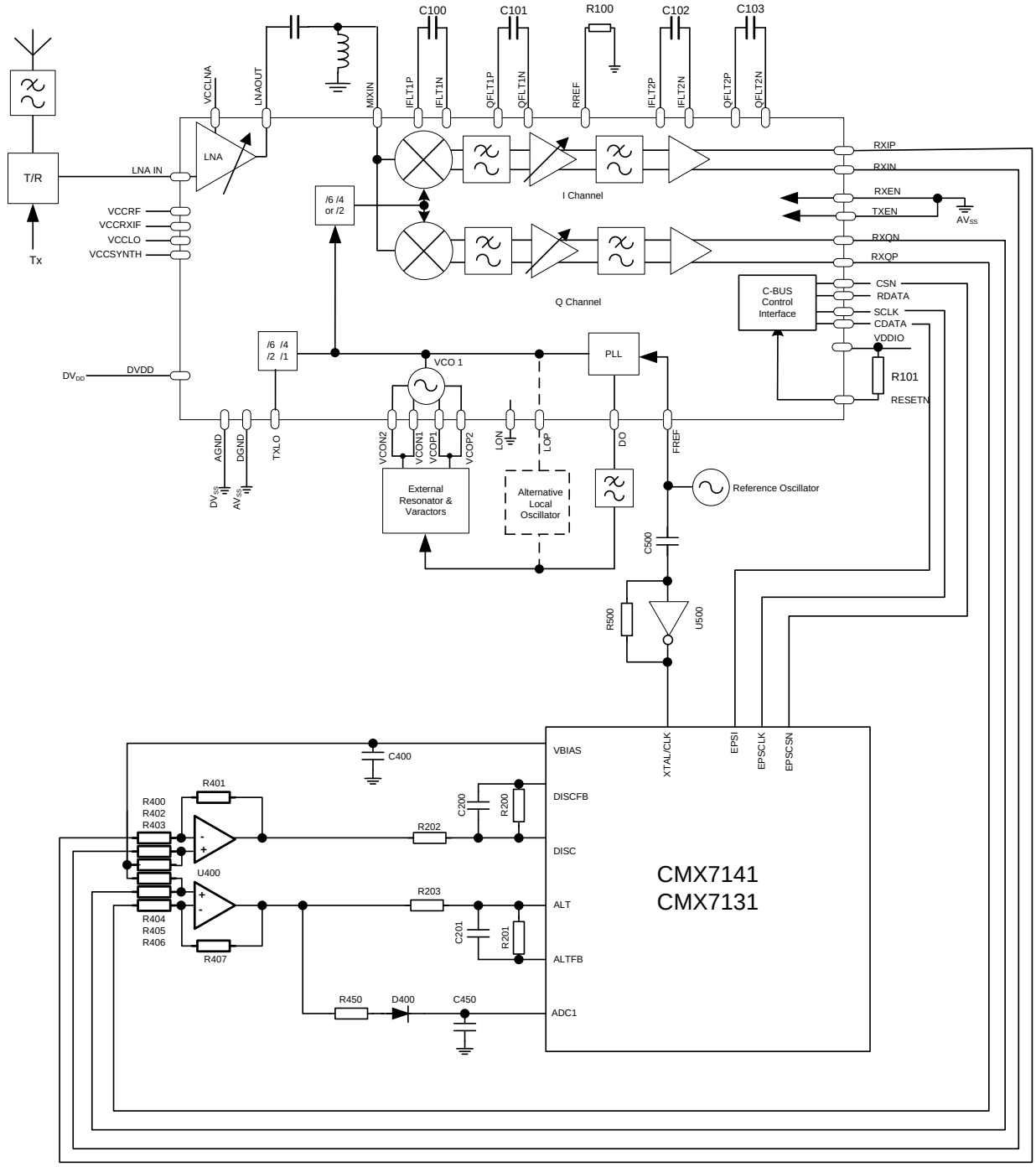


Figure 6 CMX994 Interface

Table 3 Recommended External Components when using CMX994

	R100	10kΩ	C100	1.5nF	D400 MMBD1503A
	R101	100kΩ	C101	1.5nF	
	R200	100kΩ	C102	3.9nF	U400 e.g. LM6132
	R201	100kΩ	C103	3.9nF	U500 e.g. SN74AHC1G04DRL
	R202	100kΩ	C201	100pF	
	R203	100kΩ	C202	100pF	
R400 to	R407	10kΩ	C400	100nF	
	R450	22kΩ	C450	3.3pF	
	R500	100kΩ	C500	1nF	

5 General Description

5.1 7131/7141FI-7.x Features

The 7131/7141FI-7.x Function Image™ is intended for use in half duplex digital PMR equipment using 4FSK modulation at 4.8kbps suitable for 6.25kHz channels.

Much of the dPMR® ETSI TS 102 658 standard Air Interface protocol is embedded in the 7131/7141FI-7.x Function Image™ operation namely:

Air Interface Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting

Air Interface Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame and superframe building and synchronising
- Burst and parameter definition
- Link addressing (source and destination)
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic Own-ID and Group-ID detection

Mode 1 – Peer-to-peer direct communication network (without repeaters or infrastructure), using a single frequency channel.

Mode 2 – Centralised repeater network. Includes the functionality of Mode 1, and introduces compatibility with repeaters and infrastructure whereby all communication between devices is via a repeater/base station.

Mode 3 – Managed centralised repeater network. Fully-managed access mode which includes functionality of Modes 1 and 2 but is also compatible with multi-channel and multi-site trunked networks using multiple repeaters/base stations. Note that, for Mode 3 operation, the host must be capable of handling the Beacon Channel and associated messages used by this mode. The Beacon Channel is a separate channel from the traffic channels (which carry control frames, speech and data payload). The Beacon Channel carries beacon messages which are continuously monitored by the listening devices, and SYScast broadcasts which are used to control call set up.

The 7131/7141FI-7.x has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default and is compatible with 7131/7141FI-7.0 for conventional limiter/discriminator receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. The transmitter can provide a conventional output suitable for 2-point modulation or for an I/Q interface.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1. The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

Other Functions Include:

- Automatic Tx sequencer simplifies host control
- RAMDAC operation
- TXENA and RXENA hardware signals
- Two-point or I/Q modulation outputs
- Hard or soft data output options.

Auxiliary Functions:

- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC
- Two RF PLLs (CMX7131 only).

Interface:

- Optimised C-BUS (4 wire high speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Auxiliary SPI/C-BUS interface to CMX618/CMX608/CMX7262 with pass-through mode from host
- SPI bus interface for speech codec to support third-party vocoders
- Two GPIO pins
- Serial memory boot mode
- C-BUS (host) boot mode.
- Auxiliary C-BUS interface to CMX994 Direct Conversion Receiver.

5.2 System Design

A number of system architectures can be supported by the device. The most highly-integrated solution uses a CMX618 or CMX7262 Vocoder under full control of the CMX7131/CMX7141, relieving the host of all vocoder management duties. In this mode audio codec functions are provided by the vocoder chip. Other architectures using third-party vocoders are supported using SPI-Codec mode in which the CMX7131/CMX7141 acts as an external audio codec attached to the vocoder. In this mode the host must issue all control commands to the vocoder, and also transfer coded data packets between the vocoder and CMX7131/CMX7141.

The configuration of the auxiliary SPI/C-BUS port is controlled by the SPI-Codec enable bit ($B1 bit 0).

SPI-Codec $B1:0	Port Mode	
0	C-BUS	Connect to CMX6x8 or CMX7262 C-BUS port (default)
1	SPI	Connect to CMX608 or third-party vocoder SPI codec port

In SPI-Codec mode 16-bit PCM audio samples are transferred at 8ksps. When this mode is selected:

in Tx: the CMX7131/CMX7141 microphone input should be routed from MIC to Input2. The input signal is lowpass filtered, converted to 16-bit linear PCM at 8ksps and then output on the EPSI pin of the SPI-Codec port for the external vocoder to process.

in Rx: the CMX7131/CMX7141 audio output should be routed to Output1. 16-bit linear PCM samples are read from the EPSO pin of the SPI-Codec port, then filtered and output via the Audio Output Attenuator.

5.2.1 Implementation using the CMX6x8 or CMX7262

Figure 7 shows the configuration using the CMX618 RALCWI Vocoder or the CMX7262 TWELP Vocoder where all control and data is handled by the CMX7131/CMX7141 with minimal host CPU involvement. See also section 6.4.1. Note that CMX6x8 support is provided in FI7.2.x and CMX7262 support is provided in FI7.3.x.

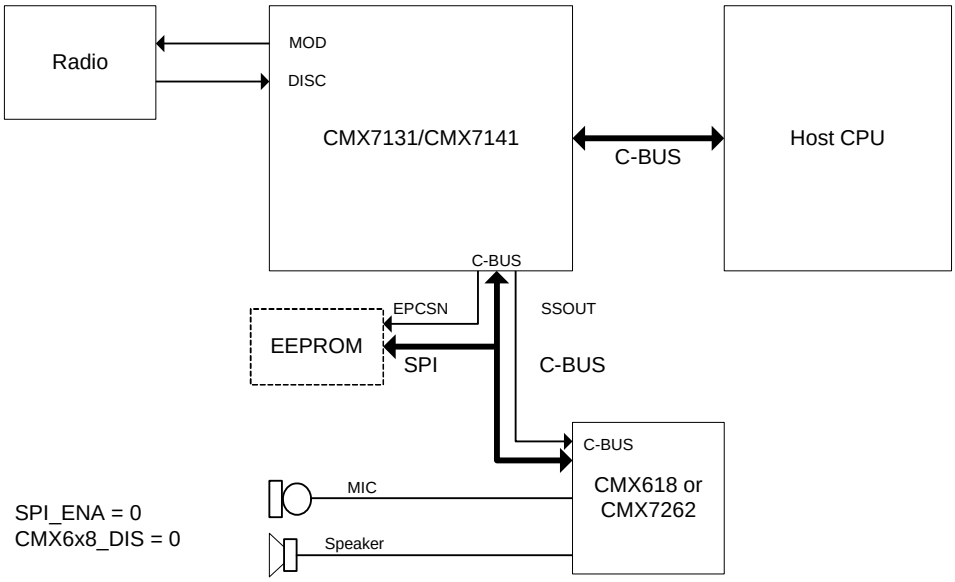


Figure 7 CMX618/CMX7262 Vocoder Connection

If the CMX608 is to be used then there are two possible architectures available. If an external audio codec is available then the CMX7131/CMX7141 (7131/7141FI-7.2.x) can take full control over the CMX608 as in Figure 7. Otherwise the audio codecs within the CMX7131/CMX7141 can be used at the expense of additional host activity. In this case, all channel data (control, addressing and payload) is transferred from the CMX7131/CMX7141 to the host over the main C-BUS interface, and the host must then transfer the voice payload (TCH) data to the CMX608 using another C-BUS interface, as shown in Figure 8.

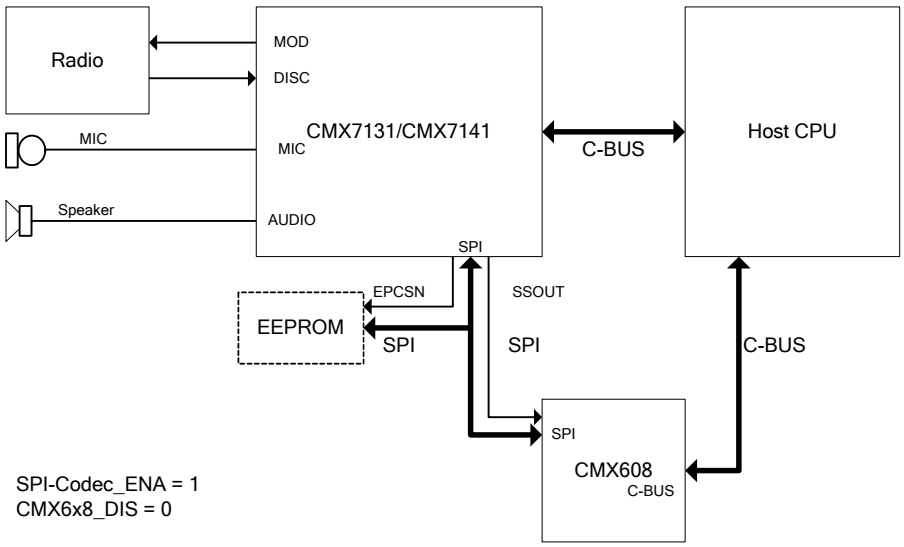


Figure 8 CMX608 Vocoder Connection

5.2.2 Implementing with Third-party Vocoders

As an alternative to the integrated architecture using the CMX618 or CMX7262, it is possible to use a third-party vocoder by routing all payload data (including voice traffic channel data) through the main C-BUS to the host. The host can then transfer it to/from the third party vocoder over a suitable port supported by the chosen vocoder. Typically these vocoders do not include audio Digital-to-Analogue and Analogue-to-Digital converters, so the CMX7131/CMX7141 can be configured to use its auxiliary C-BUS as an SPI interface and use its built-in DAC/ADCs as audio converters. This architecture is shown in Figure 9. See also section 6.5.

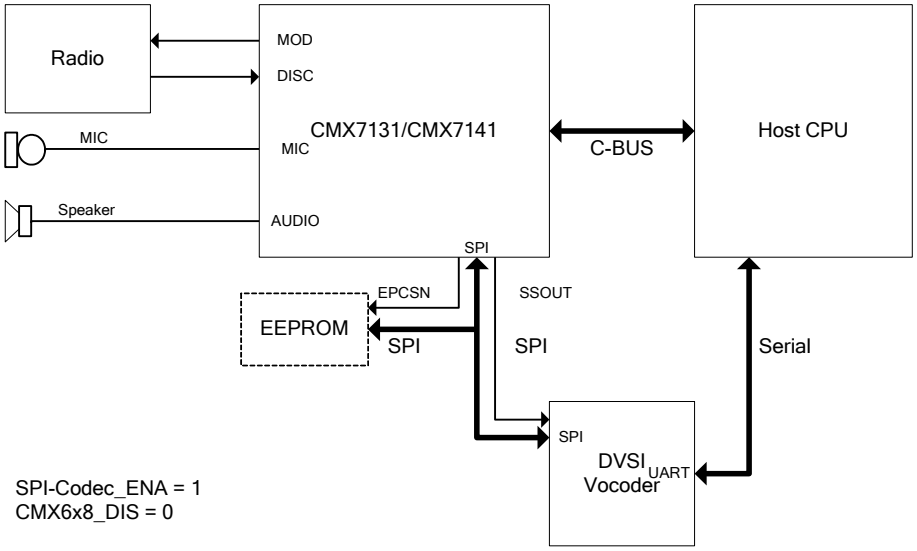


Figure 9 DVSI Vocoder Connection

5.2.3 Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The CMX7131/CMX7141 can then format and transmit that data while at the same time loading in the following data blocks from the host or vocoder chip.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the CMX7131/CMX7141 filters, demodulates and decodes the output data before presenting it to the host or vocoder chip directly. For best performance, voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format compatible with the CMX618/CMX608/CMX7262 and other third-party vocoders, although this mode increases the data transfer rate over C-BUS by a factor of four.

5.2.4 RSSI Measurement (LD Mode)

The AuxADC provided by the CMX7131/CMX7141 can be used to detect the Squelch or RSSI signal from the RF section while the device is in Rx or Idle mode. This allows a significant degree of powersaving within the CMX7131/CMX7141 and avoids the need to wake the host up unnecessarily. The host programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.2.5 Serial Memory Connection (LD Mode only)

In all cases, the auxiliary C-BUS/SPI-Codec bus is shared with the serial memory bus which may be used to hold the contents of the Function Image™. Bus conflicts are avoided by the use of an additional Chip Select signal (SSOUT). If this feature is not used, the EPCSN pin should be left unconnected. Serial Memory may not be used in I/Q interface mode.

5.2.6 CMX994 Connection (I/Q Mode)

The CMX994 can be connected via the C-BUS connection in place of the serial memory (Table 4). This allows the CMX994 to be using along with either the CMX6x8, CMX7262, DVSI vocoder or other third party vocoder.

Note that the data and clock connections to the CMX994 are common with the Vocoder so the data traffic on the interface is a potential source of noise / interference in the radio.

Table 4 CMX994 Connections

CMX7131/CMX7141 Pin	CMX994 Pin
EPSCSN	CSN
EPSI	CDATA
EPSCLK	SCLK.
No connection	RDATA

The operation of the CMX994 is generally automatic, however specific data may be written to CMX994 registers using the pass-through mode available using register $C8. For example if the CMX994 PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994 PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception.

5.2.7 Hardware AGC – AuxADC1 Connection

In I/Q mode the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components (shown in Figure 6). This function provides a broadband signal detector which is used in the AGC process. This is required to prevent the DISC/ALT ADC inputs limiting internally in the presence of alternate channel signals, which are attenuated by the inherent filtering of the ADC.

This functionality is enabled by setting:

- Program Block P2.0:b8=1 (enable hardware AGC)
- Program Block P3.0 = $F002 (AuxADC1 averaging = 2)
- $CD = $4205 (hi threshold)
- $CD = $0200 (lo threshold)
- $A7 = $0030 (turn AuxADC1 on)

Note that threshold levels may need adjustment to suit particular hardware implementations.

5.2.8 RSSI Measurement (I/Q Mode)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 10 shows a typical response.

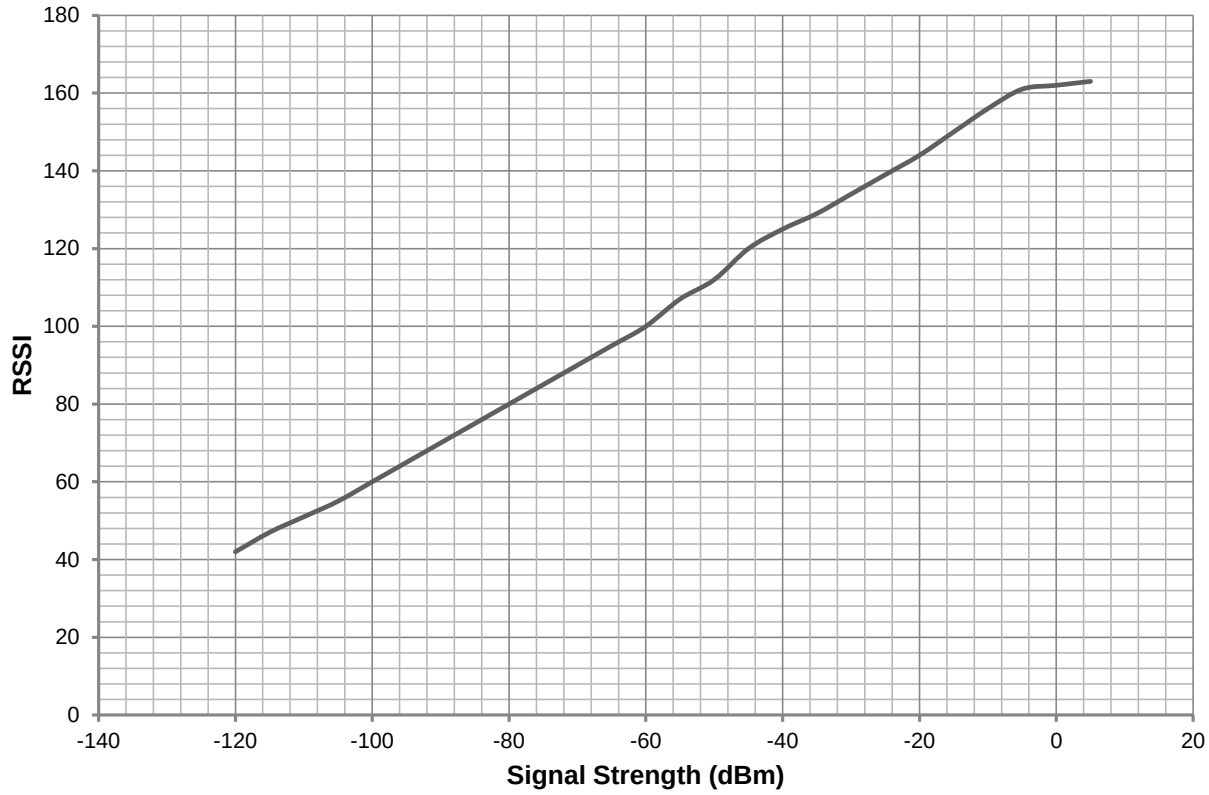


Figure 10 RSSI in I/Q Mode

5.3 dPMR® Modem Description

This modem can run at 4.8kbps occupying a 6.25kHz bandwidth RF channel. It has been designed such that, when combined with suitable RF, host controller, CMX618/CMX608 or CMX7262 Vocoder and appropriate control software, it meets the requirements of the EN 301 166 standard. See www.etsi.org for details of these standards.

TS 102 658 is available on the ETSI web site (www.etsi.org) which describes a 6.25kHz channel spacing FDMA dPMR® system. This standard uses a 4FSK modulation scheme with an over-air bit rate of 4800bps (i.e. 2.4ksymbols/s). With respect to dPMR® formatted modes of operation, this document should be read in conjunction with the ETSI standard. TS 102 658 Mode 1 is largely compatible with (but not identical to) TS 102 490 (dPMR® peer-to-peer mode for license-free operation) in CSF mode. TS 102 658 Mode 2 introduces repeater operation, whilst Mode 3 covers a fully-featured trunked mode. The additional features in Mode 2 and Mode 3 operation require significantly more host processing than Mode 1, so the data interface is different when compared with FI-1.x or FI-5.x. For example, for Mode 3 operation the device must monitor the beacon channel for incoming frame types which are specific to trunked networks. This is described in more detail in section 6.7.

The dPMR® standard does not specify a voice coding algorithm, but the CMX618, CMX608 or CMX7262 (also available from CML) are suitable devices for this purpose.[2].

[2] In the rest of this document these CMX608 and CMX618 devices are referred to generically as the CMX6x8. The only significant difference between them is the inclusion of an on-chip audio codec in the CMX618 while the CMX608 requires an external Audio Codec

The CMX6x8 uses the RALCWI algorithm whilst the CMX7272 uses the high performance TWELP algorithm. Both can be directly controlled by the CMX7131/CMX7141 with minimal host involvement.

Alternatively, the device can be configured to act as an external Audio Codec for a third-party Vocoder (such as DVSI AMBE-3000).

Note that the TS 102 658 (dPMR® standard is NOT compatible with the TS 102 361 (DMR) 12.5kHz/9600baud TDMA system).

5.3.1 Modulation

The dPMR® 4FSK modulation scheme operates in a 6.25kHz channel bandwidth with a deviation index of 0.29 and has an over-air bit rate of 4.8kbps (2.4ksymbols/s). RRC filters are implemented in both Tx and Rx with a filter 'alpha' of 0.2. The maximum frequency error is +/-625Hz and the CMX7131/CMX7141 can adapt to the maximum time-base clock drift of 2ppm over the duration of a 180-second burst. Figure 13 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

Figure 11 and Figure 12 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36k span and zero-span mode, having been two-point modulated using a suitable RF transmitter.

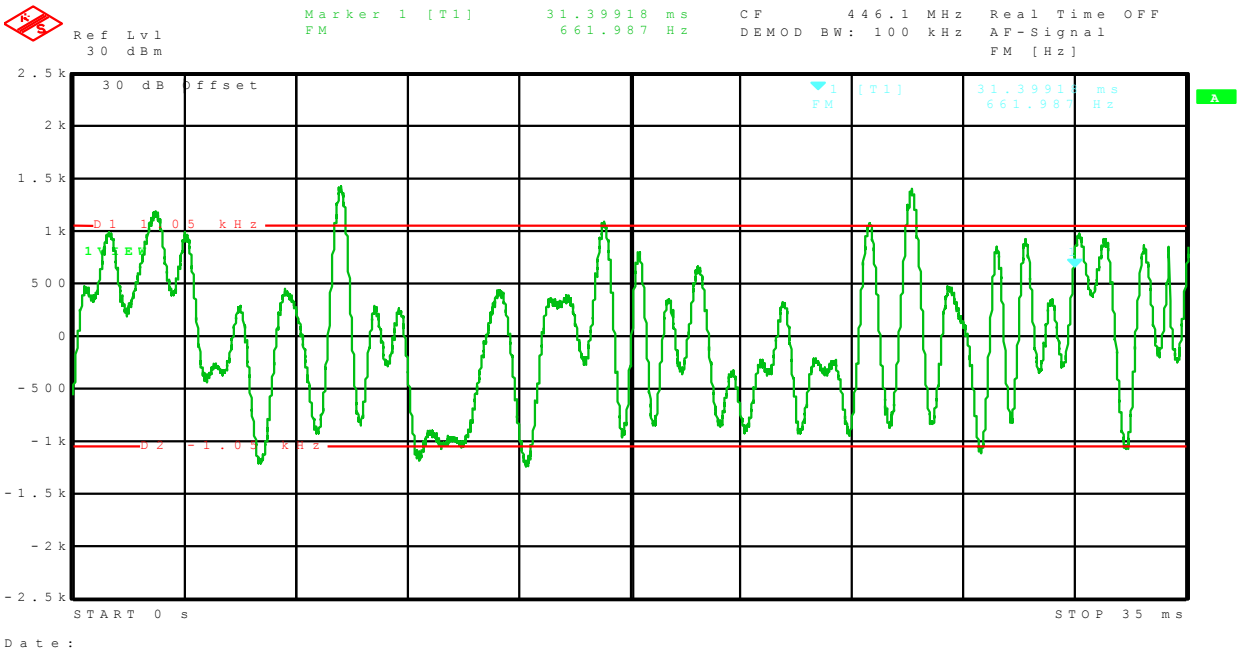


Figure 11 4FSK PRBS Waveform - Modulation

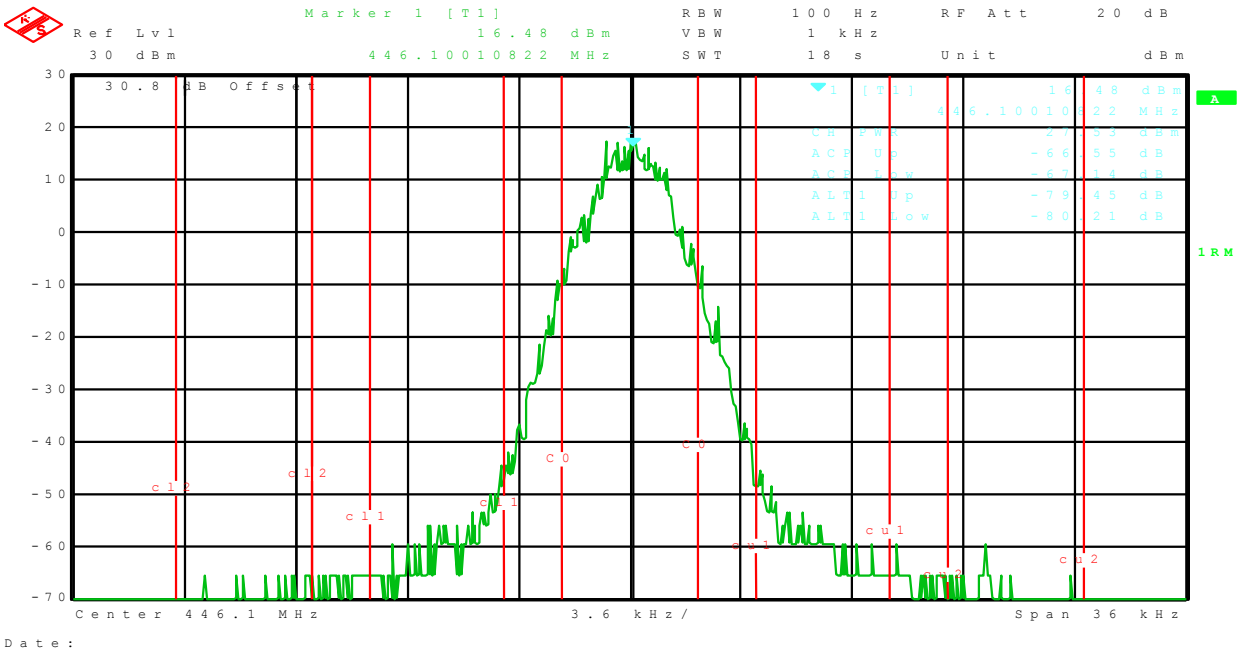
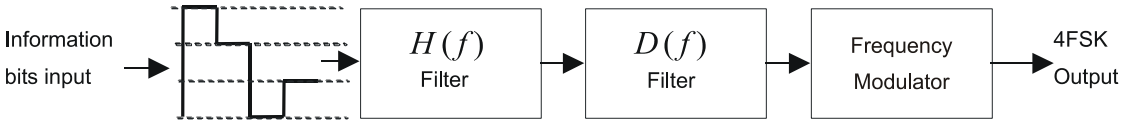


Figure 12 4FSK PRBS Waveform - Spectrum

Tx Baseband Filter



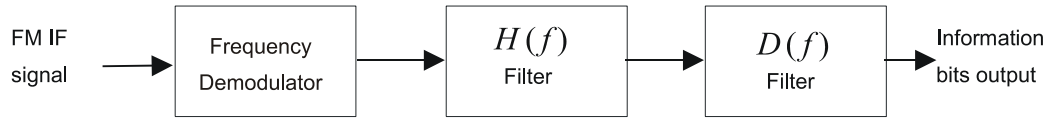
$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\sin(\pi fT)}{\pi fT}$$

4FSK Deviation		
Di-bit	Symbol	Deviation
01_2	+3	+1 050Hz
00_2	+1	+350Hz
10_2	-1	-350Hz
11_2	-3	-1050Hz

Rx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\pi fT}{\sin(\pi fT)}$$

Figure 13 dPMR® Modulation Characteristics

5.3.2 Internal Data Processing

The CMX7131/CMX7141 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power Idle mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 14. Additional processing in I/Q Mode is shown in Figure 15.

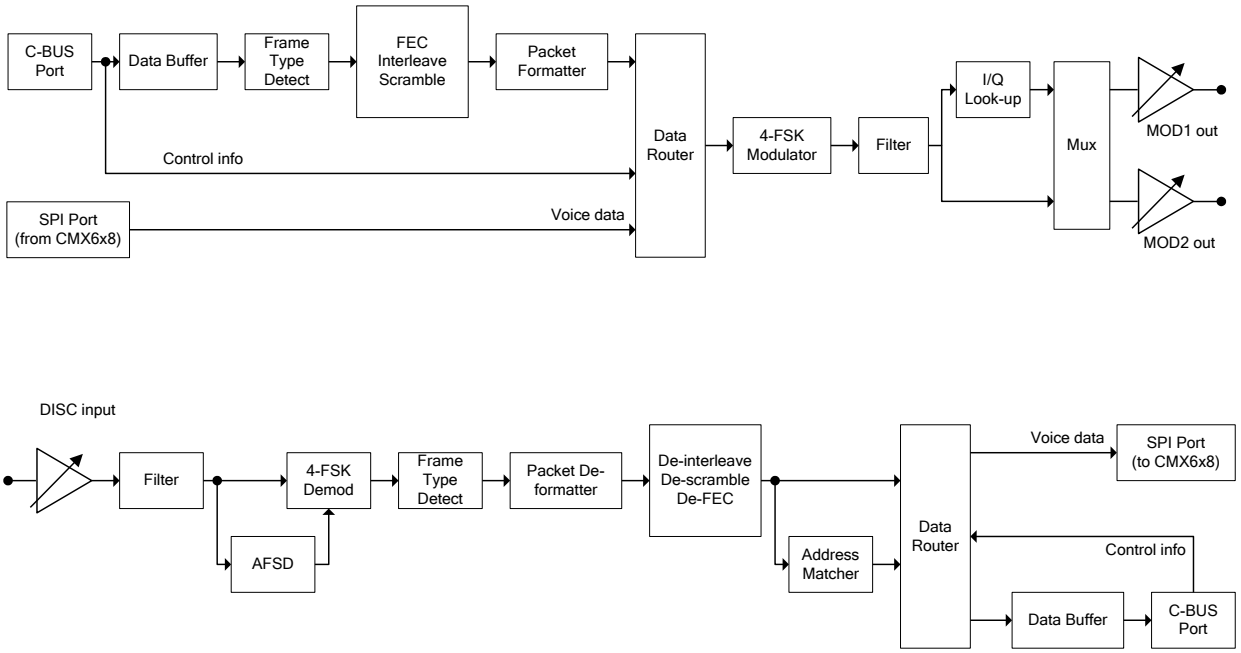


Figure 14 Internal Data Processing Blocks (LD Mode)

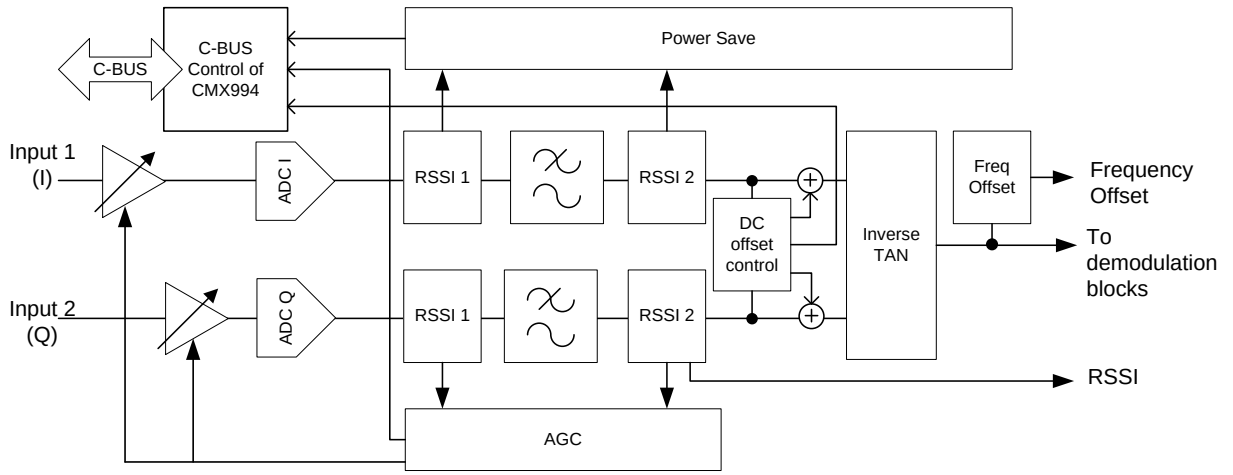


Figure 15 Additional Internal Data Processing in I/Q Mode

5.3.3 Frame Sync Detection and Demodulation

The analogue signal from the receiver may be from either a CMX994 I/Q interface or a limiter/discriminator (LD) output. The signal(s) from the RF section should be applied to the CMX7131/CMX7141 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx). The signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the CMX7131/CMX7141 Input Gain settings. In LD mode the signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the data-processing sections that follow are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. The

CMX7131/CMX7141 can detect the end of a burst by scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

In I/Q mode filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before RRC filtering, after which the signal chain is then the same as the LD case. In I/Q mode the CMX7131/CMX7141 provides measurements of frequency error and RSSI (which are not available in LD mode).

A dPMR® burst begins with a 72-bit or longer preamble sequence followed by a 80ms Header Frame, which contains a 48-bit frame sync (FS1 or FS4). Payload frames contain either a 24-bit frame sync (FS2) or a 24-bit Colour Code. The CMX7131/CMX7141 can scan for all dPMR® frame syncs concurrently. It uses FS1 to detect the start of a transmission, and can optionally use FS2 to perform 'late entry' into an existing burst. The short length of FS2 gives a high probability of false detects, so the CMX7131/CMX7141 only accepts an incoming burst from an FS2 detect if a second FS2 is received at the correct frame spacing. Frame sync detects are reported with an FS Detect IRQ and a code in the Modem Status register ($C9).

When frame synchronisation has been achieved, the 4FSK demodulator is enabled, frame sync detection is switched off and subsequent frame sync sequences embedded in the received frames are not reported.

Table 5 and Table 6 show an example of typical call setup sequence in Mode 1 (peer-to-peer or direct mode). Mode 2 (repeater mode) is similar; however different RF frequencies may be used by the Rx and Tx paths. Call set-up in Mode 3 (trunked mode) is more complex as the trunking controller manages the data transactions over the RF channels.

Mode 3 (trunked) operation differs significantly from Modes 1 and 2 by the use of a Control/Signalling channel (the Beacon Channel) which conveys signalling and system information to the terminals using the SYScast frame types. The 7131/7141FI-7.x includes support for receiving and decoding these additional frame types (which is not available in FI-1.x or FI-5.x).

Table 5 dPMR® Frame Format - Call set-up, no ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

Table 6 dPMR® Frame Format - Call set-up with ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
End	Tx	FS3	End Flag														
Ack	Rx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

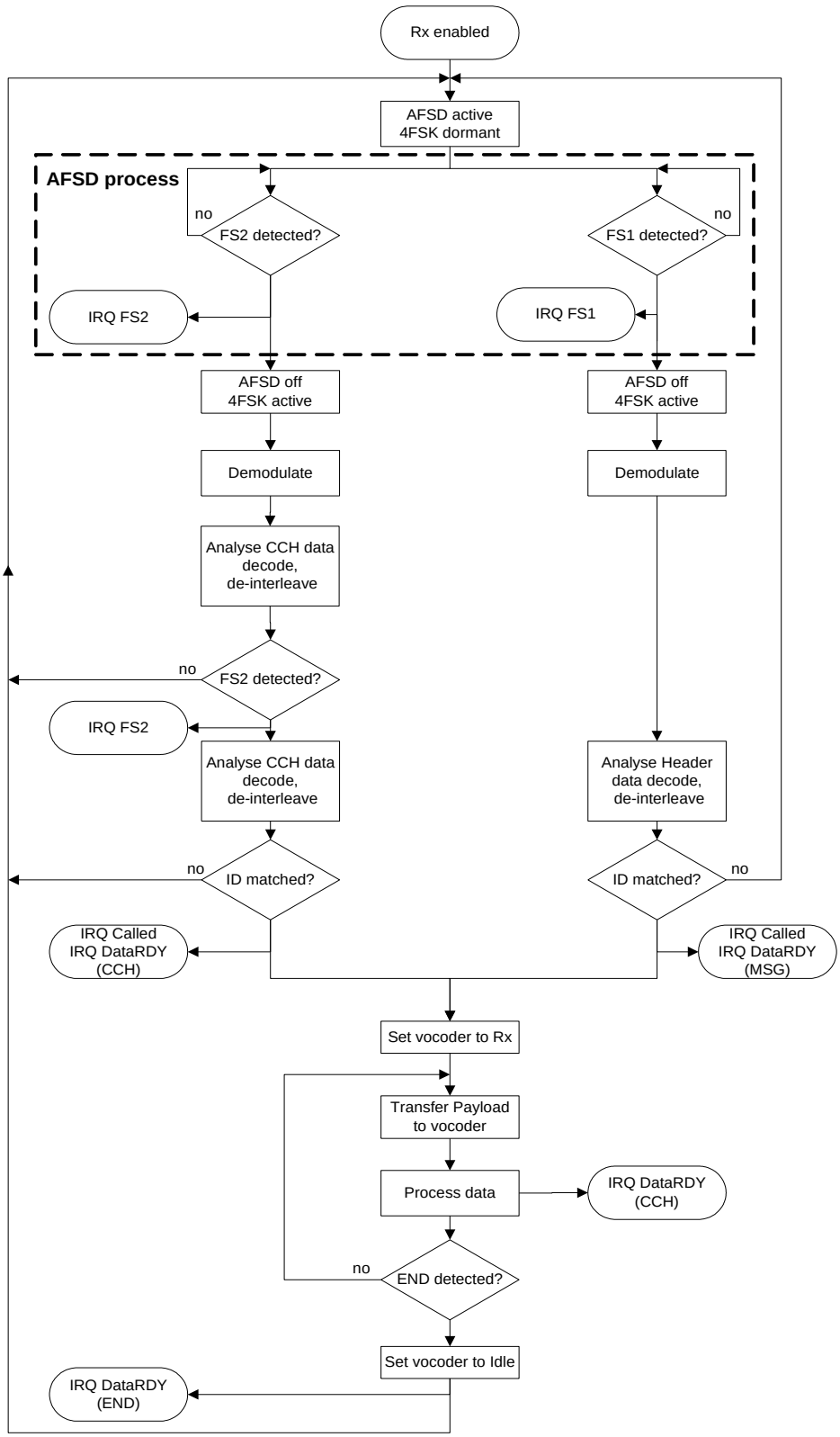


Figure 16 FS Detection

5.3.4 FEC and Coding

The CMX7131/CMX7141 implements all CRCs, Hamming codes, interleaving and scrambling required by the dPMR® standard. Any CRC failures in control channel fields or coded data blocks are indicated when transferring the decoded fields or data to the host. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7131/CMX7141.

The dPMR® Message Frame format contains duplicate copies of all control channel fields (in the MI0 and MI1 Message Information blocks) but only one MI block is transferred to/from the host. On receiving a Message Frame the CMX7131/CMX7141 decodes both MI blocks, checks both CRCs and can accept the call if either block is valid.

5.3.5 Voice Coding

A CML CMX618 or CMX608 RALCWI vocoder or CMX7262 TWELP vocoder can be used under the control of the CMX7131/CMX7141. The CMX7131/CMX7141 provides an auxiliary SPI/C-BUS port (shared with the boot serial memory) which is used to issue control commands and transfer voice payload data directly to the vocoder chip, minimising the loading on the host controller during voice calls. In order to support the CMX618/CMX608 the CMX7131/CMX7141 should be loaded with FI-7.2.x while to support a CMX7262 vocoder the CMX7131/CMX7141 should be loaded with FI-7.3.x.

Alternatively, the CMX7131/CMX7141 can support any third-party vocoder by routing voice payload data over the main C-BUS interface and through the host. In this mode, all vocoder control and data transfers must be managed by the host.

Voice data transferred to a directly controlled CMX vocoder in Rx mode always uses soft decision (4-bit log-likelihood ratio) format. This option is also available for voice payload data routed to the host, although it increases the required data transfer rate over C-BUS by a factor of four.

5.3.6 Radio Performance Requirements

In LD mode, for optimum performance, the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.

In I/Q mode the recommended interfacing to the CMX994 should be used, see section 4.3. The CMX7131/CMX7141 includes digital filters to provide adjacent channel rejection while compensating for the in-band response of the CMX994 I/Q filters.

Further information and application notes can be found at http://www.cmlmicro.com .

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7131/CMX7141 is designed to work with an external frequency source of 19.2MHz. If this default configuration is not used, then Program Register Block 3 must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency.

A table of common values can be found in Table 7. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24MHz can be used.

The register values in Table 7 are shown in hex, the default settings are shown in bold and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 7 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
			3.579	6.144	9.216	12.0	12.8	16.368	16.8	**19.2**
P3.2	Idle	GP timer	*$017*	$018	$018	$019	$019	*$018*	$019	**$018**
P3.3		VCO output and AUX clk divide	*$085*	$088	$08C	*$10F*	*$110*	*$095*	*$115*	**$099**
P3.4	Rx or Tx	Ref clk divide	*$043*	$040	$060	$07D	$0C8	$155	$15E	**$0C8**
P3.5		PLL clk divide	*$398*	$200	$200	$200	$300	$400	$400	**$200**
P3.6		VCO output and AUX clk divide	*$140*	$140	$140	$140	$140	$140	$140	**$140**
P3.7		Internal ADC/DAC clk divide	*$008*	$008	$008	$008	$008	$008	$008	**$008**

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7131/CMX7141 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.6.2.

The CMX7131/CMX7141 will monitor the state of the C-BUS registers that the host has written-to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

6.2.1 C-BUS Operation

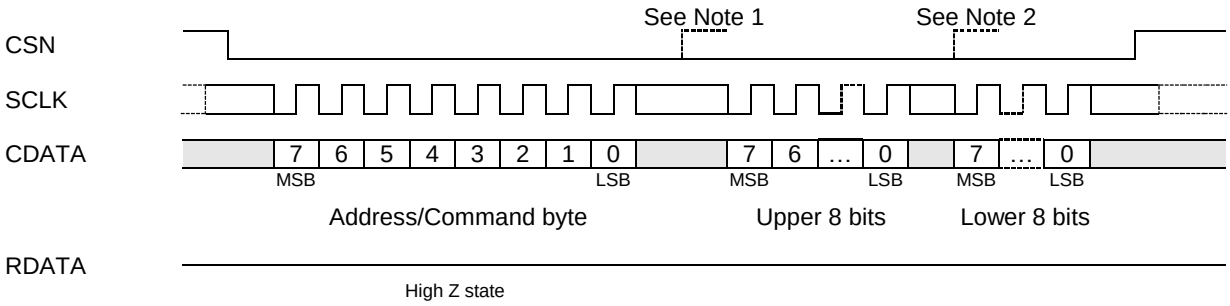
This block provides for the transfer of data and control or status information between the CMX7131/CMX7141's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7131/CMX7141's Write Only Registers, or one or more data byte(s) read out from one of the CMX7131/CMX7141's Read Only Registers, as shown in Figure 17.

Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7131/CMX7141 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7131/CMX7141 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high

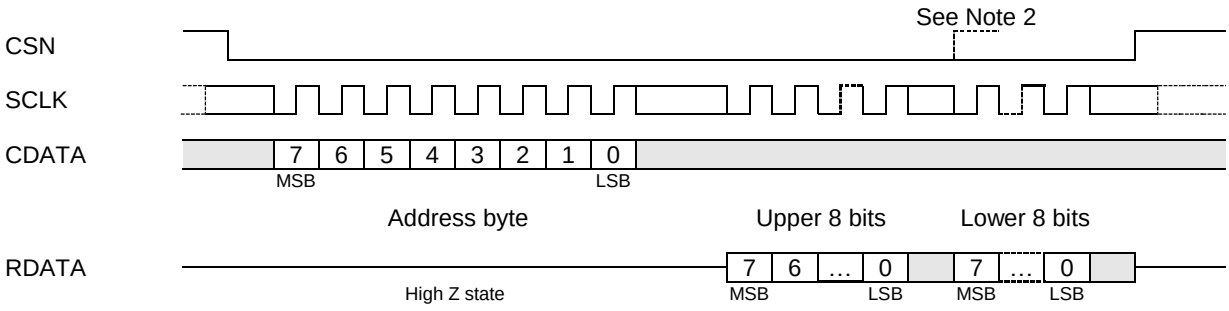
between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 17 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

NOTE: Function Image™ loading from serial memory is not supported when FI-7.x is used in I/Q mode (because the serial memory interface is used for CMX994 control) or with FI-7.3.x (which requires an additional FI to be loaded into the CMX7262).

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. If the CMX994 is to be used, then the BOOTEN pins MUST both be held high once the FI load has completed, otherwise they are ignored by the CMX7131/CMX7141 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220k resistor (see Figure 18).

For serial memory load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the serial memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 8). The serial memory interface is shared with the Auxiliary C-BUS port which controls the CMX6x8 Vocoder using a separate chip select (SSOUT) pin. During boot operations, the SSOUT will be disabled. Once the boot operation has completed, the serial memory chip select (EPCSN) will be disabled and the SSOUT will become operational.

Once the FI has been loaded, the CMX7131/CMX7141 performs these actions:

(1) The product identification code ($7141 or $7131) is reported in C-BUS register $C5
(2) The FI version code is reported in C-BUS register $C9
(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) Once activated, the device initialises fully, enters idle mode and becomes ready for use, and the Programming flag (bit 0 of the Status register) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power-cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 8 BOOTEN Pin States

	BOOTEN2	**BOOTEN1**
C-BUS Host load	1	1
Reserved	1	0
Serial Memory load	0	1
No FI load	0	0

Note: Following a General reset, reloading of the Function Image is strongly recommended.
Note: For operation with the CMX994, BOOTEN1 and BOOTEN2 MUST be held high at all times.

6.3.1 Loading FI-7.2.x from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7131/CMX7141 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7131/CMX7141 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7131/CMX7141.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.

Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (IRQ Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to the Programming register has been accepted. The PRG flag state can be determined by polling the IRQ Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

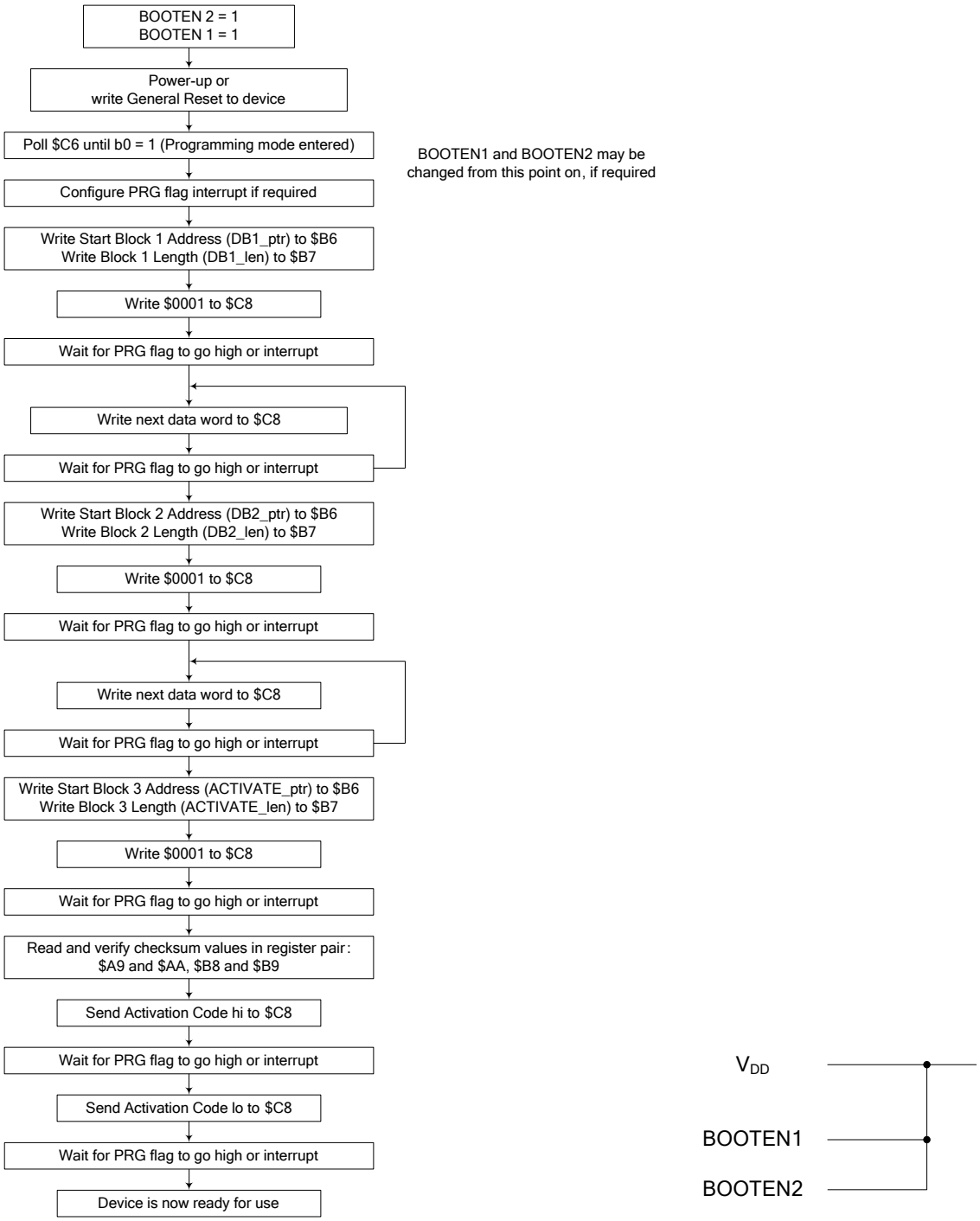


Figure 18 FI Loading from Host

6.3.2 Loading FI-7.3.x from Host Controller

When using the CMX7262 under direct control of the CMX7131/CMX7141 it is necessary to also load the CMX7262 with its own FI. This can be accomplished by providing the CMX7262 with its own serial flash storage locally (see the CMX7262 Data Sheet for details), or over the host C-BUS connection after completing the initial CMX7131/CMX7141 FI load by making use of an additional download mode which is only available in FI-7.3.x. This is enabled by changing the Block 3 ACTIVATE_ptr from $4010 to $400E. In

this mode any further data blocks received are transferred through the CMX7131/CMX7141 to the connected CMX7262.

Following the download of the modified activation block pointer the boot checksums may be verified to confirm that the CMX7141 Function Image™ was correctly transferred. Following this the next blocks may be transferred across the CBUS interface in a similar manner – these will be the sections from the CMX7262 Function Image™. Upon receiving the 2nd Activation Pointer (that of the CMX7262) the boot checksums will be available to be read. They will be read from the CMX7141 registers $AA:$A9 and $B9:$B8 but will be the checksums of the CMX7262 Function Image™ blocks which were transferred.

Upon successful read-back of the checksums the host may proceed to load the CMX7141 activation codes.

Alternatively, a combined Function Image maybe supplied as a single .h file suitably pre-formatted for download – contact CML Application Support for details.

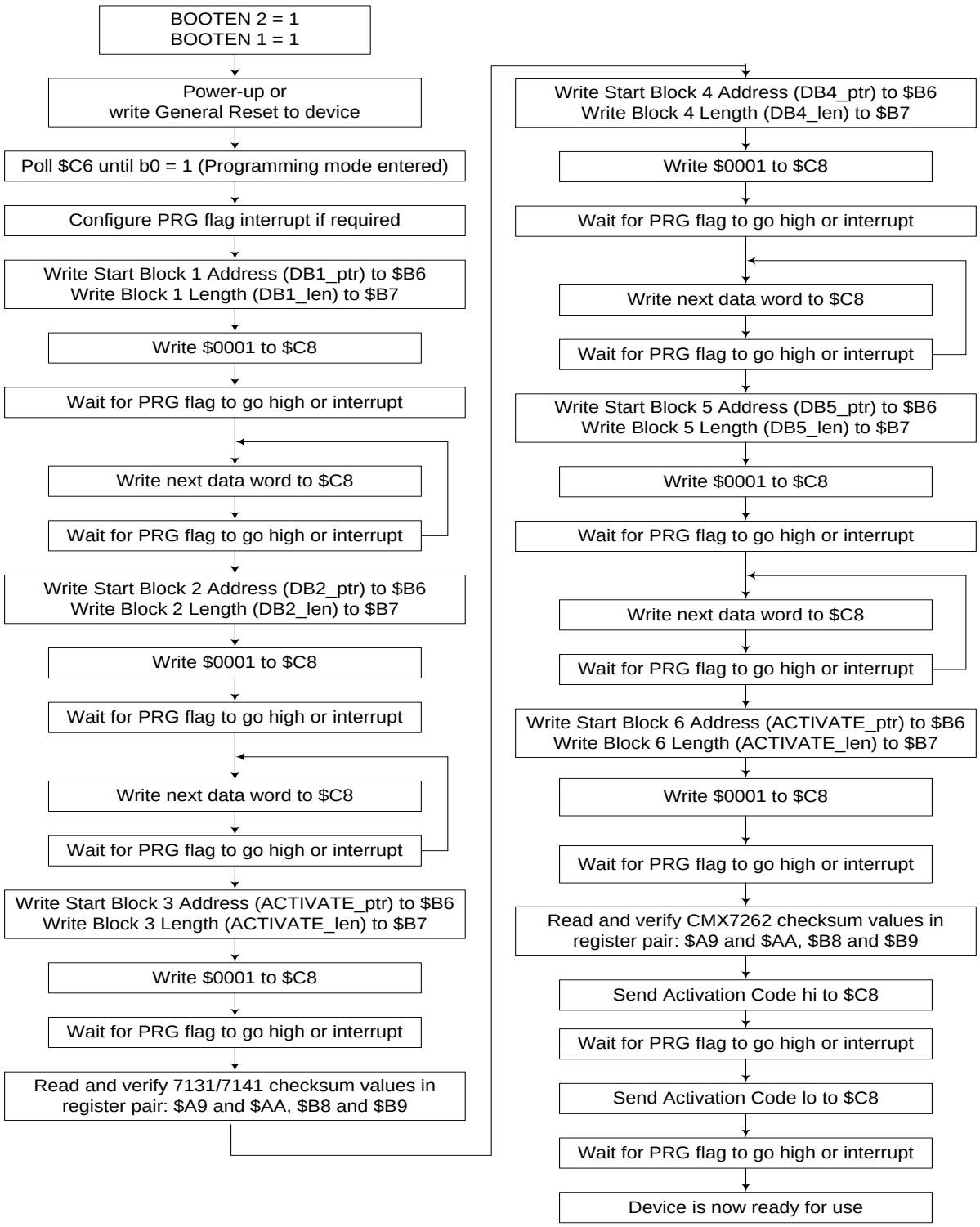


Figure 19 FI Loading (including CMX7262 using SPI boot loader mode)

Blocks 1,2,3 are provided from the CMX7131/CMX7141-FI7.3.x file, but with Block 3 ACTIVATION_ptr set to $400E.

Blocks 4,5,6 are provided from the CMX7262-FI1.x file with the Block 6 ACTIVATION_ptr set to $4010.

6.3.3 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The CMX7131/CMX7141 needs to have the BOOTEN pins set to serial memory load, and then on power-on, or following a C-BUS General Reset, the CMX7131/CMX7141 will automatically load the data from the serial memory without intervention from the host controller.

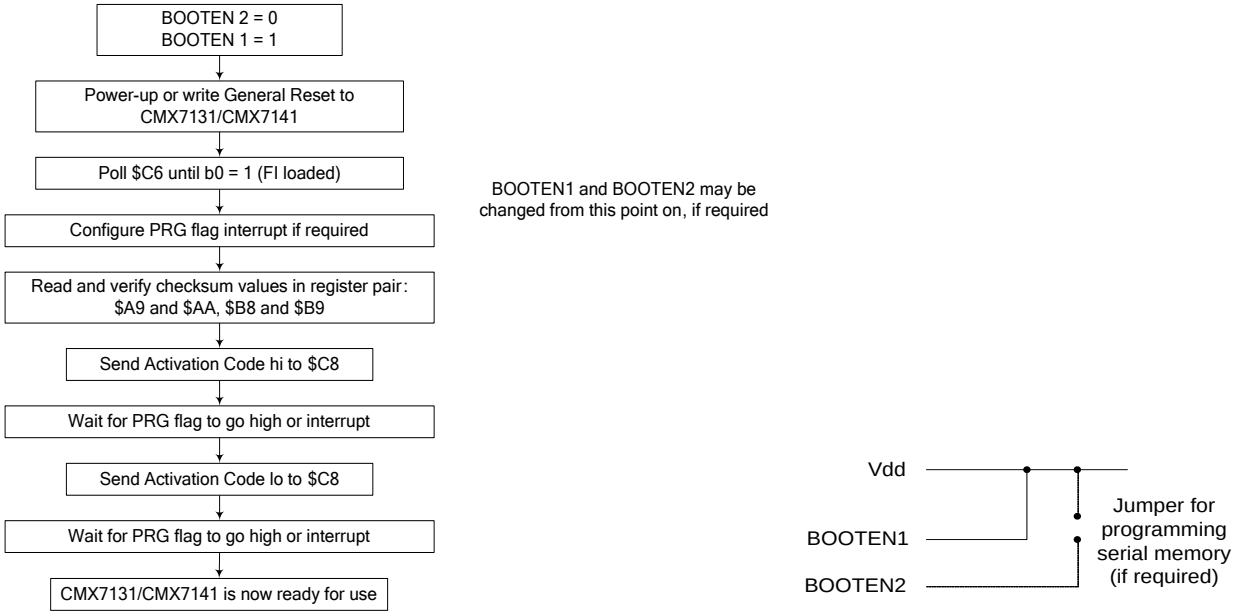


Figure 20 FI Loading from Serial Memory

The CMX7131/CMX7141 has been designed to function with an Atmel AT25HP512 serial EEPROM and the AT25F512 Flash EEPROM devices[3], however other manufacturers' parts may also be suitable. The time taken to load the FI is dependent on the Xtal frequency, with a 6.144MHz Xtal, it should load in less than 1 second.

NOTE: FI loading from serial memory is not supported when FI-7.x is used in I/Q mode.

6.4 Direct Vocoder Control Interface

6.4.1 CMX618/CMX608/CMX7262 Interface

An auxiliary SPI/C-BUS interface is provided which allows the CMX6x8 or CMX7262 to be directly controlled by the CMX7131/CMX7141 without the need for the host to intervene. This is accomplished by re-using the serial memory SPI interface with an additional Chip Select pin (SSOUT). The serial memory Data Out pin MUST NOT drive the signal line when the chip is not enabled, otherwise the Vocoder will not be able to return its data to the CMX7131/CMX7141. The CMX7131/CMX7141 Auxiliary SPI/C-BUS interface bus should be connected to the C-BUS interface on the Vocoder using the SSOUT pin as the CSN signal for the CMX6x8/CMX7262 running in C-BUS mode (this is the default setting of the SPI-Codec ENA pin, $B1 bit 0). Following receipt of the Activation Codes at power-on, the Function Image™ will automatically select C-BUS mode and poll the interface to see if a CMX6x8/CMX7262 is connected on its C-BUS port.

[3] Note that these two devices have slightly different addressing schemes. 7131/7141FI-7.1.x is compatible with both schemes.

The initialisation and operational settings of the CMX6x8/CMX7262 should be programmed by the host into the CMX7131/CMX7141 Program Block 1 on power-up. These values will be written to the defined registers in the Vocoder at:

- Initialisation
- Idle mode
- Rx mode
- Tx mode

Mic Gain and Speaker Gain commands may be sent to the Vocoder whenever the CMX7131/CMX7141 is in Rx or Tx mode.

The DTX and VAD modes of the CMX6x8 are not supported in 7131/7141FI-7.2.x. DTMF Mode 1 (transparent) is supported.
The default settings for the CMX6x8 (using FI-7.2.x) are:

- 4-frame packet (80ms) with FEC no STD, no DTMF
- 2.4kbps with FEC
- Internal sync
- Throttle = 1
- Internal Audio codec
- IRQ disabled
- Soft-coded data bits.

The default settings for the CMX7262 (using FI-7.3.x) are:

- 4-frame packet (80ms) with FEC
- 2.4kbps with FEC
- Internal sync
- IRQ disabled
- Soft-coded data bits
- Internal Audio codec.

The connections for the Vocoder are shown Table 9.

Table 9 CMX6x8/CMX7262 Vocoder Connections

CMX7131/CMX7141 Pin	CMX6x8/CMX7262 Pin
SSOUT	CSN
EPSI	CDATA
EPSO	RDATA
EPSCLK	CLK
No connection	IRQN (tied to V_{DD} via 100kΩ resistor).

Figure 21 shows one possible implementation of the CMX7141 combined with a CMX618, a host microcontroller and suitable RF sections to provide a digital PMR radio. The bold lines show the active signal paths in Rx and Tx respectively.

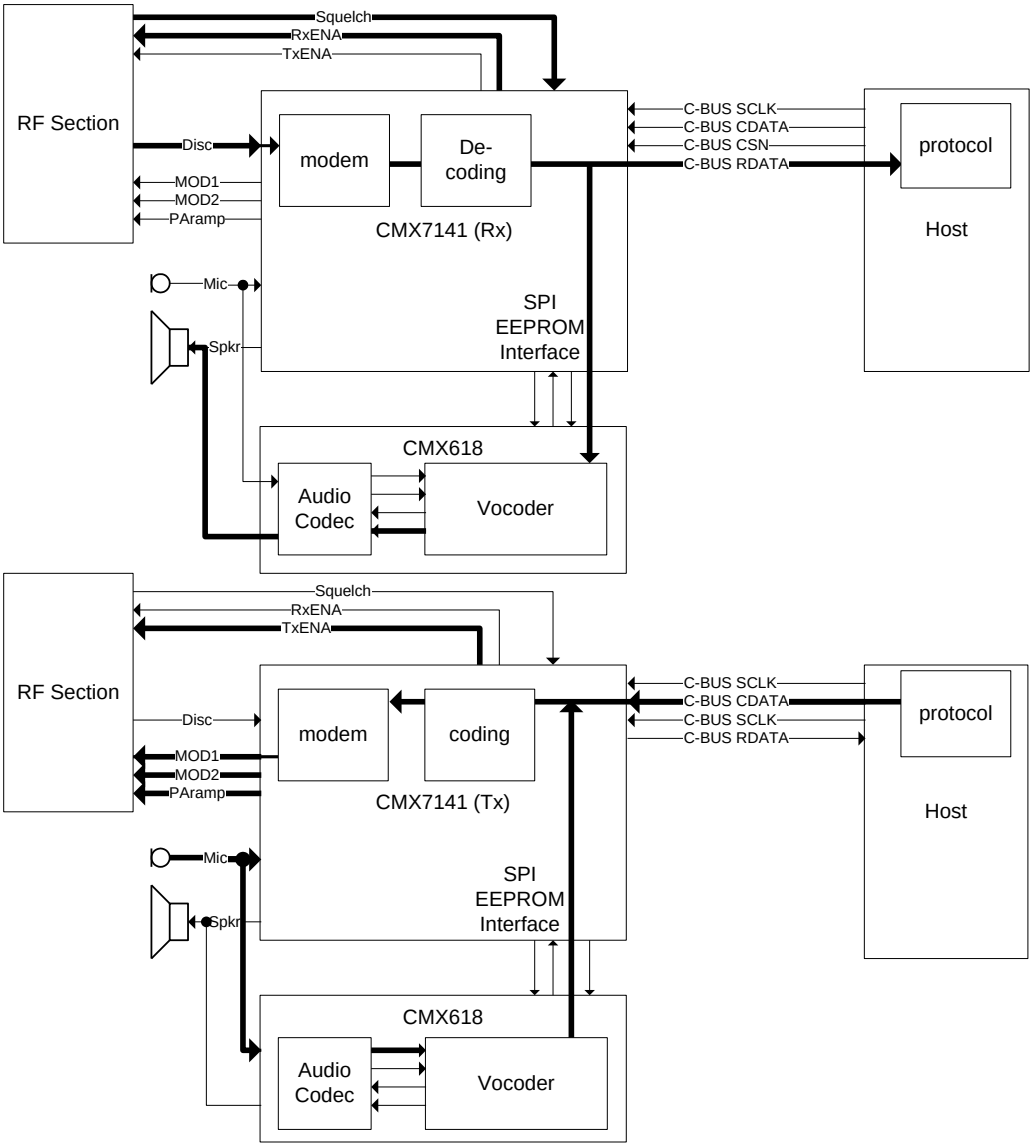


Figure 21 Digital Voice Rx and Tx Blocks

The paralleling of the microphone and speaker connections between the CMX618 and the CMX7131/CMX7141 is only required if the CMX7131/CMX7141 is also to provide analogue PMR functionality. Otherwise, the microphone and speaker should be connected to the CMX618 only. The CMX618 RALCWI Vocoder provides an on-chip audio and voice codec, but alternatively a CMX608 device could be used along with an external audio codec. Voice payload data is transferred directly from and to the CMX618 by the CMX7131/CMX7141. Note that the CMX618 Audio output does not have a high impedance mode, therefore an external analogue switch is required if the Analogue 7031/7041FI-1.x or 7131/7141FI-8 is to be used on the device to isolate it.

The interface to the CMX7262 is the same as that for the CMX618 if the internal Audio codecs are to be used, or as the CMX608 if the Audio codec on the CMX7131/CMX7141 are to be used.

6.5 External Codec Support

6.5.1 DVSI Vocoder Interface

If the DVSI vocoder (or other third-party vocoder) is used all radio channel data will need to be transferred over the main C-BUS through the host. In this case the Vocoder Enable Program registers (P1.19 and P1.20) must be set appropriately to respond correctly to the incoming data fields and the SPI-Codec ENA bit ($B1 bit 0) should be set to 1. To speed the power-on process, the automatic presence check for the CMX6x8 may be skipped by setting the SPI-Codec ENA bit BEFORE the activation codes are loaded during the power-on sequence.

The connections for the DCR standard vocoder from DVSI are shown in Table 10.

Table 10 DCR Standard Vocoder Connections

CMX7131/CMX7141 Pin	AMBE3000 Pin
SSOUT	SPI_STE
EPSI	SPI_RX_DATA
EPSO	SPI_TX_DATA
EPSCLK	SPI_CLK and SPI_CLK_IN.

6.5.2 Support for I²S Mode

The device can support I²S interfaces in mono, 16-bit mode only, for transmitting and receiving audio codec data using the SPI bus. This mode is selected in block 1 of the Programming register (see section 8.2.2). Figure 22 shows typical transmit waveforms.

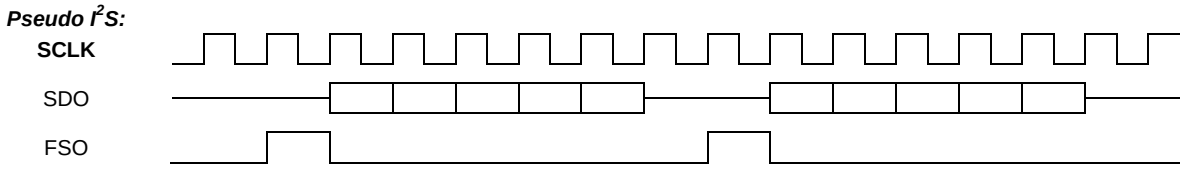


Figure 22 I²S Mode Support

6.6 Device Control

The CMX7131/CMX7141 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required signal routing and gain

(4) Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. This will also command the CMX6x8 to enter powersaving mode as well. Additional powersaving can be achieved by disabling any unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.

See:

- Power Down Control - $C0 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

6.6.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Modem Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- TxAuxData - $C2 write
- Vocoder Control - $C3 write.

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the CMX6x8 out of its powersave mode. Setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX7131/CMX7141 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

6.6.2 Interrupt Operation

The CMX7131/CMX7141 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit ($0 \rightarrow 1$) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write.

Continuous polling of the Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host IO pin and poll this pin instead.

6.6.3 Signal Routing

The CMX7131/CMX7141 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.

See:

- Input Gain and Signal Routing - $B1 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Programming registers in the CMX7131/CMX7141. The Mic. and Speaker gains are set by the vocoder chip, which is controlled through the Vocoder Control - $C3 write of the CMX7131/CMX7141.

See:

- Analogue Output Gain - $B0 write (MOD1 and 2)
- Input Gain and Signal Routing - $B1 write
- Vocoder Control - $C3 write (Vocoder Mic. and Speaker).

In common with other FIs developed for the CMX7131/CMX7141, this device is equipped with two signal processing paths. In LD mode input 1 should be routed to any of the three input sources (ALT, DISC or MIC) which should be connected to the radio's discriminator output. The internal signals Output 1 and

Output 2 are used to provide either two-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required. In I/Q mode input 1 should be routed to the DISC input source for the I channel input and input 2 should be routed to the ALT input source for the Q channel input.

It is important to correctly attach the signal from the CMX994 I/Q outputs to the CMX7141 DISC and ALT inputs. Crossing these connections will cause the CMX7141 dc offset calibration to fail, as attempted corrections to the I signal will be made to the Q signal and vice versa. Crossed connections can be swapped using the Input Gain and Signal Routing register ($B1:b5-2). Likewise, it is important that the sense of connection is correct between the CMX994 and CMX7141. If the input signals are inverted then attempts by the CMX7141 to remove the dc offset will, in fact, increase the dc offset. The inputs may be inverted by using the 'Input Invert' bit in the Analogue Output Gain register ($B0:b7). When demodulating the received signal (internally to the CMX7141), it is possible that the signal could be inverted, resulting in no framesync detection and, in effect, inverted data. Often this can be corrected by swapping the I and Q signals (changing the signal that leads in phase to the one that lags). However, the relationship between the I/Q outputs of the CMX994 and the CMX7141 DISC and ALT inputs must be maintained, as described above. Therefore the demodulated signal can be inverted using the Programming register block 0, P0.10 b1 (IFD).

In dPMR® Formatted modes the microphone and speaker paths are automatically re-routed to the CMX6x8 Vocoder, when appropriate. This routing is controlled by the data field in the Header Block, which indicates whether the payload is speech data, and the Vocoder Disable bit in the Modem Configuration register, $C7.

6.6.4 Modem Control

The CMX7131/CMX7141 operates in one of these operational modes:

- Idle
- Rx
- Tx
- CMX6x8/CMX7262/CMX994 Pass-through
- Rx with CMX994 I/Q Cal.
- Rx with Powersave

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Modem Control - $C1 write.

GPIO1 and GPIO2 pins (RXENA and TXENA) reflect bits 0 and 1 of the Modem Control register, as shown in Table 11. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 11 Modem Mode Selection

Modem Control ($C1) b3-0	Modem Mode	GPIO2 - TXENA	GPIO1 - RXENA
0000	Idle – Low Power Mode	1	1
0001	Rx	1	0
0010	Tx	0	1
0011	*Reserved*	x	x
0100	CMX6x8/CMX7262/CMX994 Pass-through	1	1
0101	Rx with CMX994 I/Q Cal.(I/Q mode only)	1	0
1001	Rx with Powersave (I/Q mode only)	1	0
others	*Reserved*	x	x

The CMX6x8/CMX7262/CMX994 Pass-through mode is used to control and monitor the CMX6x8, CMX7262 or CMX994 directly. This cannot be accessed if the CMX7131/CMX7141 is in Rx or Tx modes. This mode will transfer data to/from the TxData0/RxData0 register to the CMX6x8 or CMX7262 C-BUS register address specified in the Programming register ($C8). See section 6.6.20. The Modem Control bits are ignored in this mode.

Table 12 Modem Control Selection

4FSK Modem Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx dPMR® Formatted	Tx dPMR® Formatted
0010	Rx Raw	*Reserved*
0011	Rx 4FSK EYE	Tx 4FSK PRBS
0100	Rx Pass-through Mode	Tx 4FSK Preamble
0101	*Reserved*	Tx 4FSK Mod Set-up
0110	Sync	Test
0111	Reset/Abort	Reset/Abort
1xxx	*Reserved*	*Reserved*

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

6.6.5 Tx Mode dPMR®

In Tx dPMR® mode operation ($C1, Modem Control = $0012), the host should write the initial Message Info data block to the C-BUS TxData registers and set the Modem Mode to dPMR® Formatted and the Mode bits to Tx. The preamble and frame sync are transmitted automatically followed by the coded Message frame contents. As soon as the Message Info data block has been read from the C-BUS TxData registers, the 'Data Ready' IRQ is asserted and the next block of control channel or payload data may be loaded. If the Message Info fields indicate that the burst is a voice call, and use of the CMX6x8 or CMX7262 vocoder has been enabled, encoded voice data will be taken from it directly for transmission over-air.

At the end of the burst after the last bit has left the modulator a 'Tx Done' IRQ will be issued. At this point it is now safe for the host to change the Modem Control and Modem Mode to Idle ($C1, Modem Control = $0000) and turn the RF transmitter off.

6.6.6 Tx Mode PRBS

In PRBS mode ($C1, Modem Control = $0032) the preamble and frame sync are transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para. 2.1) giving a 511-bit repeating sequence.

6.6.7 Tx Mode Preamble

In Preamble mode ($C1, Modem Control = $0042) the preamble sequence [+3 +3 -3 -3] is sent continually. This can be used to set up and adjust the RF hardware.

6.6.8 Tx Mode Mod Set-up

In Mod Set-up mode ($C1 = $0052) the output depends on the selected Tx modulation type. In two-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols is sent, and in I/Q mode a continuous sequence of +3 symbols is sent. This can be used to set up and adjust the RF hardware.

6.6.9 Tx Mode Test

In Test mode, simple test waveforms are generated (defined by the dPMR Association TWG). See section 8.1.22.

6.6.10 Tx Sequencer

If enabled, the Tx Sequencer will automatically start executing its sequence of transmit actions when the CMX7131/CMX7141 is placed in Tx mode. The timing values for each action can be set in P3.75 to P3.80 and are defined in increments of 250µs.

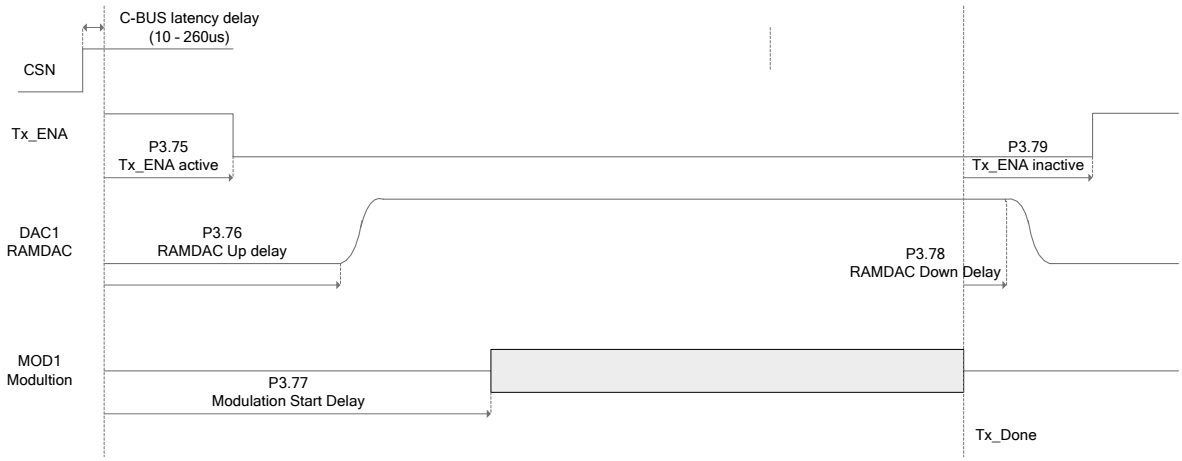


Figure 23 Automatic Tx Sequencer

6.6.11 Rx Mode dPMR®

In Rx dPMR® mode operation ($C1, Modem Control = $0011), the CMX7131/CMX7141 will automatically start searching for frame synchronisation. When a valid frame sync sequence is detected, an 'FS detect' IRQ is asserted and the data demodulator is enabled. If the burst is then accepted a 'Called' IRQ is asserted and the first Message Info or CCH Info block is loaded into the C-BUS RxData registers with a 'Data Ready' IRQ. If the control channel fields indicate that the burst is a voice call, and use of the CMX6x8 vocoder has been enabled, received payload data will be sent to it directly for decoding. Otherwise payload data is loaded into the C-BUS RxData registers with a 'Data Ready' IRQ to indicate when each new block is available. If 'soft' data mode has been selected, the payload data is encoded in 4-bit log-likelihood-ratio format and the host must be able to service the 'Data Ready' IRQs and RxData registers at four times the normal rate to avoid overflow.

6.6.12 Rx Mode Raw

Rx Mode Raw is included in this FI to facilitate BER measurements. In this mode ($C1, Modem Control = $0021), once a valid Frame Sync has been detected, all following data received is loaded directly into the C-BUS RxData registers. This continues until the end of the burst (even if there is no valid signal at the input). On exiting Rx Mode Raw, there may be a DataRdy IRQ pending which should be cleared by the host. Note that Raw Mode operation always requires the incoming data to be preceded with a valid Preamble and Frame Sync pattern in order to derive timing information for the demodulator. The device

will update the C-BUS RxData registers with Rx payload data as it becomes available. The host MUST respond to the DataRDY IRQ before the RxData registers are over-written by subsequent data from the modem.

6.6.13 Rx Mode Eye

In Rx 4FSK EYE mode ($C1 = $0031), the filtered received signal is output at the MOD1 pin as an 'eye' diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal. In I/Q mode, this includes I/Q dc calculation in RXDATA0, RXDATA1 and computed Powersave Levels 1,2,3 in RXDATA2-4.

6.6.14 Rx Pass-through Mode

Rx Pass-through mode ($C1 = $0041) is very similar to Rx Mode Eye as described in section 6.6.13. However the output at the MOD1 pin is the flat, unfiltered signal. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

Table 13 Frequency Response for Rx Pass-through Mode

300Hz	-0.6dB
1kHz	0dB (reference)
2kHz	-0.7dB
2.5kHz	-1.4dB
3kHz	-2.4dB
4kHz	-4.9dB
6kHz	-12.2dB

6.6.15 Rx Mode with CMX994 AGC (I/Q Mode only)

By default, when receiving in I/Q Mode the CMX7131/CMX7141 will control its internal analogue gain and the gain of the CMX994 in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P2.0 (I/Q AGC function), in which case any setup that the host has made of the CMX994 will determine its gain, with the input gain of the CMX7131/CMX7141 being controlled using the Input Gain and Signal Routing - $B1 write register.

It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994 as described in section 6.6.16.

6.6.16 Rx Mode with CMX994 I/Q Cal (I/Q Mode only)

When receiving, the CMX7131/CMX7141 will estimate and remove the dc error present in the I/Q signals from a CMX994 receiver. However, it is necessary to calibrate the CMX994 so that the magnitude of the dc offsets present is as small as possible. Selecting Rx mode with CMX994 I/Q Cal ($C1, Modem Control b3-0 = $5) causes the CMX7131/CMX7141 to measure the dc offset on the DISC and ALT input pins and to control the CMX994 receiver to minimise the dc offsets. The CMX7131/CMX7141 will then begin to receive normally – correcting the remaining dc offset internally.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994 is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Having calibrated the CMX994, the value written to the CMX994 dc offset correction register is available to read using the Aux Data and Status ($A9, $AA) registers. This means that having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time.

6.6.17 Rx Mode with Powersave (I/Q Mode only)

Selecting powersave mode ($C1, Modem Control b3-0 = $9) will cause the CMX7131/CMX7141 to control the CMX994, switching it into a low-power state for a short period of time. Once the powersave timer has expired then the CMX994 and the internal circuits of the CMX7131/CMX7141 will be powered-up, ready to receive.

On entering the powered-up state, the CMX7131/CMX7141 will monitor the received I/Q signals for energy in its sampled bandwidth and if there is no signal present it will return to the powersave state, powering down the CMX994. If sampled energy is found then the signal is passed through a channel filter and the resulting signal measured. If no signal is found the powersave state is selected once more. Finally, a squelch measurement is taken, by FM demodulating the received signal and measuring the energy above the expected signal bandwidth. If squelch indicates that the signal is a good FM modulated signal powersave mode is ended, leaving the CMX994 and CMX7131/CMX7141 on and in receive, until the mode register is written to.

Throughout the time that the receiver is on, the CMX7131/CMX7141 will search for a frame sync and start receiving the data following that frame sync, if found. However, dependent on the powersave period, it is possible that the frame sync at the start of a burst may be missed, in which case 'late entry' is possible.

Thresholds for comparison and timings for powersave mode may be adjusted, potentially improving powersaving by being powered down for a greater period of time, but at the expense of a slower reaction to a received signal. See the Aux Config $CD write register.

6.6.18 Reset/Abort

From each Rx or Tx mode, a Reset/Abort aborts the current state machine and drops into the corresponding (Rx or Tx) Idle mode. The only difference between this and going directly into the corresponding Idle mode is that all of the buffers and filters are flushed out first with Reset/Abort.

6.6.19 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred.

Table 14 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 and info	$B8	Rx data 0-7 and info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

Bits 7 and 6 hold the Transaction Counter, which is incremented modulo 4 on every read/write of the Data Block to allow detection of data underflow and overflow conditions. In Tx mode the host must increment the counter on every write to the TxData block, and if the CMX7131/CMX7141 identifies that a block has been written out of sequence, the Event bit (C-BUS register $C6, b14) will be asserted and an IRQ raised, if enabled. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (i.e. it should be the last register the host writes to in any block transfer). In Rx mode, the CMX7131/CMX7141 will automatically increment the counter every time it writes to the RxData block. If the host identifies that a block has been written out of sequence, then it is likely that a data overrun condition has occurred and some data has been lost. If a CRC failure has been detected when decoding the data block, an 'Event' IRQ is issued concurrently with the 'Data Ready' IRQ along with a status code in the Modem Status register ($C9).

6.6.20 CMX6x8/CMX7262/CMX994 Pass-through Mode

To allow the host to communicate directly with the CMX6x8, CMX7262 or CMX994 for test and configuration purposes, a pass-through mode is available which allows any CMX994 C-BUS register to be written or any CMX6x8 or CMX7262 C-BUS register to be read or written (as appropriate). This mode uses the TxData0, RxData0 and Programming registers on the CMX7131/CMX7141.

To write to the CMX6x8/CMX7262:

- Set the CMX7131/CMX7141 to CMX6x8/CMX7262/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8/CMX7262 data value to the TxData0 register ($B5)
- Write the CMX6x8/CMX7262 C-BUS address to the Programming register ($C8) with b15-13=$010_2$
- Wait for the Program Flag to be set ($C6 b0).

To read from the CMX6x8/CMX7262:

- Set the CMX7131/CMX7141 to CMX6x8/CMX7262/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8/CMX7262 C-BUS address to the Programming register ($C8) with b15-13=$110_2$
- Wait for the Program Flag to be set ($C6 b0)
- Read the CMX6x8/CMX7262 data value from the RxData0 register ($B8).

CMX6x8 and CMX7262 C-BUS addresses are all 8 bits long and should be written to bits 0-7 of the Programming Register. Bit 15 is the read/write flag (0 = read, 1 = write) and bit 14 is the register-size flag (0 = 16-bit, 1 = 8-bit). Unused bits should be cleared to zero. When an 8-bit register is read or written, the data occupies the lower 8 bits of the appropriate data register (TxData0 or RxData0).

To write to the CMX994:

- Set the CMX7131/CMX7141 to CMX6x8/CMX7262/CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994 data value to the TxData0 register ($B5)
- Write the CMX994 C-BUS address to the Programming register ($C8) with b15-13=$011_2$
- Wait for the Program Flag to be set ($C6 b0).

6.7 dPMR® Formatted Operation

The CMX7131/CMX7141 performs all frame building/splitting and FEC coding/decoding functions, which relieves the host controller of a significant processing load. During voice calls the CMX7131/CMX7141 can automatically enable and control the CMX6x8 or CMX7262, and transfer voice payload data from/to it without host intervention. In Rx mode, the CMX7131/CMX7141 can monitor Colour Codes and address fields in incoming transmissions and only accept calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or 'sleep' state until it is really necessary to wake up, extending the battery life of the final product design. For Mode 3 (trunked) operation the host may need to monitor ALL traffic on the Beacon channel.

6.7.1 Colour Codes

The standard defines 64 Colour Codes, which are 24-bit sequences sent in Message and Payload frames for RF channel or system identification purposes. The CMX7131/CMX7141 stores the full table internally and identifies Colour Codes using their 6-bit index in this table. In Tx mode the host should supply the index of the Colour Code to be sent in the Tx AuxData register ($C2). In Rx mode the CMX7131/CMX7141 reports the index of the detected Colour Code in the Rx AuxData register ($CC) and can optionally compare it against the Colour Code specified in the Tx AuxData register ($C2) before accepting the burst. Colour Code checking is enabled using b9 of the Modem Configuration register, $C7.

6.7.2 Addressing

The standard defines two addressing schemes: 24-bit binary or 7-digit BCD (binary-coded-decimal). Both addressing schemes are supported by the CMX7131/CMX7141, selected by b11 in the Modem Configuration register, $C7 (see User Manual section 8.1.27). The standard does not mandate BCD addressing unless the host implements the Standard User Interface, but the advantages of BCD addressing are direct mapping of user keypad entries to destination addresses and the option of wildcard digits to implement group calls. BCD addresses can include wildcard digits in any of the lower four digits, and there are ten BCD 'All-Call' addresses with wildcards in all six lower digits.

The host can load two Own IDs into Program Block 1 for use in Rx mode address checking, which is enabled using b10 of the Modem Configuration register, $C7. The CMX7131/CMX7141 then compares the 'Called ID' field from incoming bursts against each of its Own IDs, and will reject the burst if a valid ID match is not found. If b11 of the Modem Configuration register, $C7, is set the CMX7131/CMX7141 will perform BCD translation of the Own IDs and the received 'Called ID' field before comparing them, allowing group call matching using wildcards.

TS 102 658 also specifies a system-wide All Call facility using the 'Communication Format' field in Header Frames (TS 102 658 section 5.5.6). The normal setting for this field is 'Peer-to-Peer', but when set to 'Call ALL' the CMX7131/CMX7141 will always accept the call regardless of address settings. The host should take care not to transmit in All Call mode unless actually intended.

6.7.3 Data Formats

TS 102 658 defines the frame and data formats of the dPMR® system for both Traffic and Beacon channels. Mode 1 and 2 systems only use Traffic channels. Mode 3 systems also use Beacon channels to manage the radio network, and terminals move onto a traffic channel when a call is actually made. Channel type is selected using b12 of the Modem Configuration register, $C7.

The CMX7131/CMX7141 uses the TxData and RxData registers to transfer data to and from the host. The Block ID field in the TxData0 register informs the CMX7131/CMX7141 how to process each transfer. Payload may be Voice, Type 1, Type 2, Type 3 or UDT Appended Data as defined in the initial Header frame. Payload data transfers are made in 9-byte blocks except for Type-2 data which is transferred in 5-byte blocks.

Table 15 TxData0 Register – Block ID Field

b5-4	Block ID	over-air bits	un-coded bits
00	MSG – Message Data	120	72
01	PLD – Payload or UDT (Traffic Channel)	72	72/40
10	CCH – CCH data	72	41
11	END – End Data	36	17

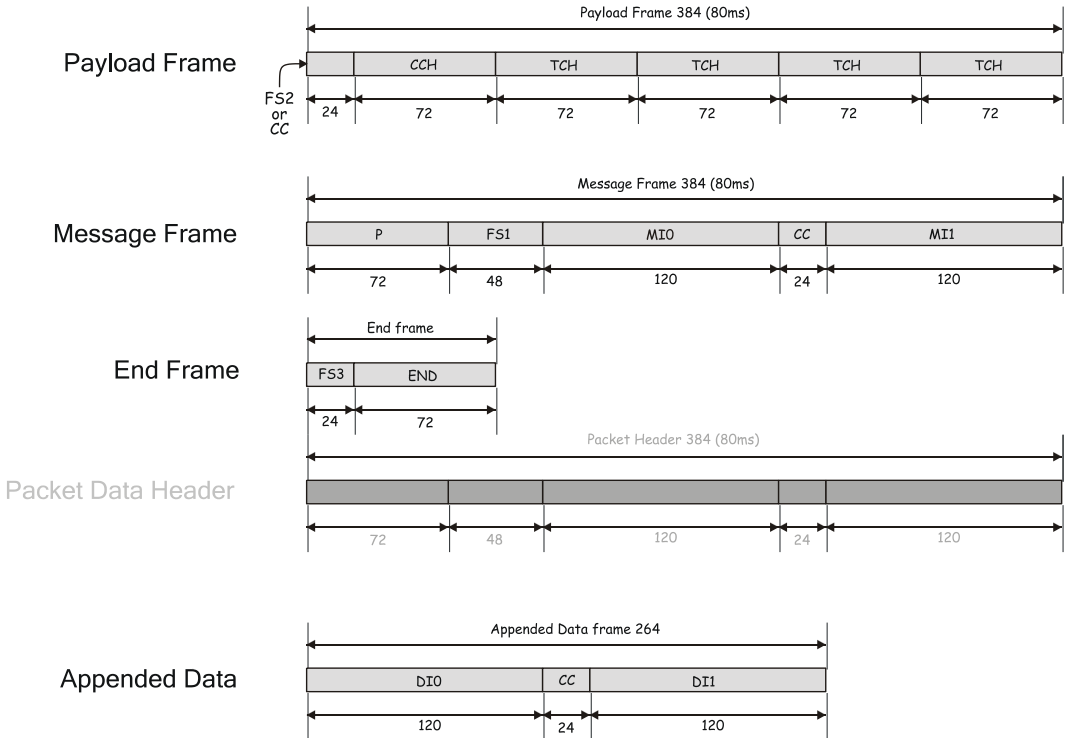


Figure 24 Traffic Channel Data Formats

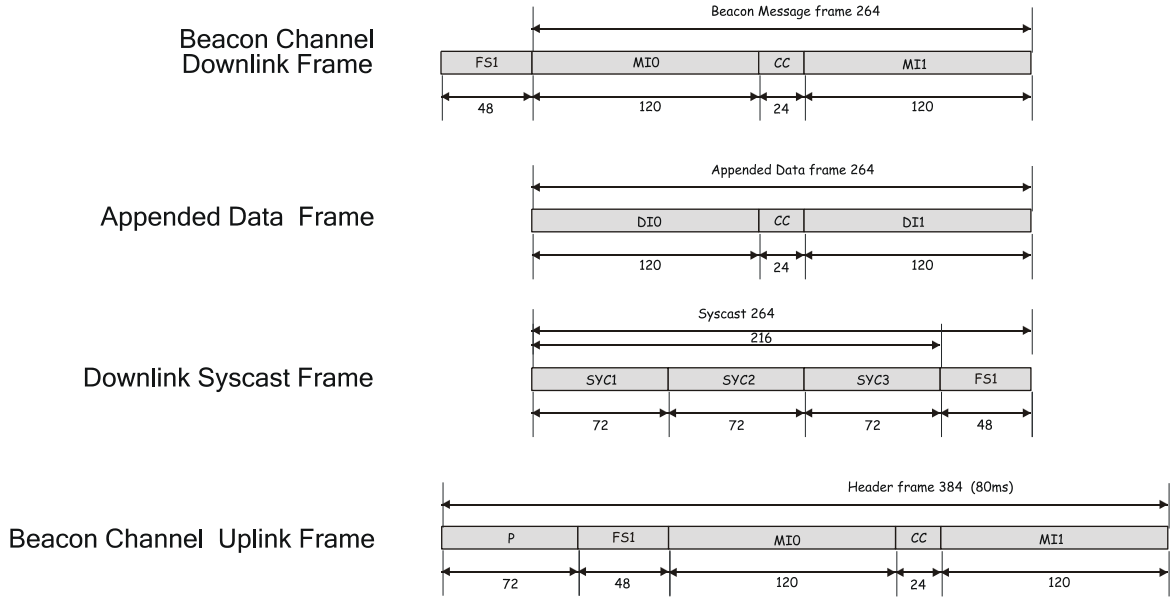


Figure 25 Beacon Channel Data Formats

Type-3 Message Data:

The occurrence of a Type-3 packet data burst is primarily signified by the presence of the FS4 sync pattern, rather than the FS1 used for all other bursts. It should be noted that FS4 is the logical inverse of FS1, so radio designs that inadvertently invert the demodulated waveform can erroneously report an FS4 when an FS1 would be expected – this should, however, be corrected in the design stage of the radio's development and should not occur in the field. The use of the FS4 enables the data contained in the Message/Header block to be formatted in a different manner, though, in practice, there a number of similarities. The subsequent burst format of the data is however, significantly different and requires a new handler for both Rx and Tx to be invoked.

Data Format:

The data formats of a Type-3 burst are shown in the following diagram as examples. It should be appreciated that ONLY the burst carrying the Type-3 data uses the FS4, any initial call-set-up or polling bursts to check for radio presence or routing utilise the standard FS1 style bursts that are already supported. The MI_detail field specifies the data length and the number of packets-per-burst. This is significantly different from the normal superframe format. In this implementation, as soon as an FS4 is detected, the burst which follows is assumed to be Type-3 data, irrespective of any other settings in the Message/Header block.

It should be noted that only two of the four possible values of pDs (data length) are supported – these being:

- pDs = 0 (288 bits)
- pDs = 3 (1440 bits)

See TS 102 658 section 9.4.

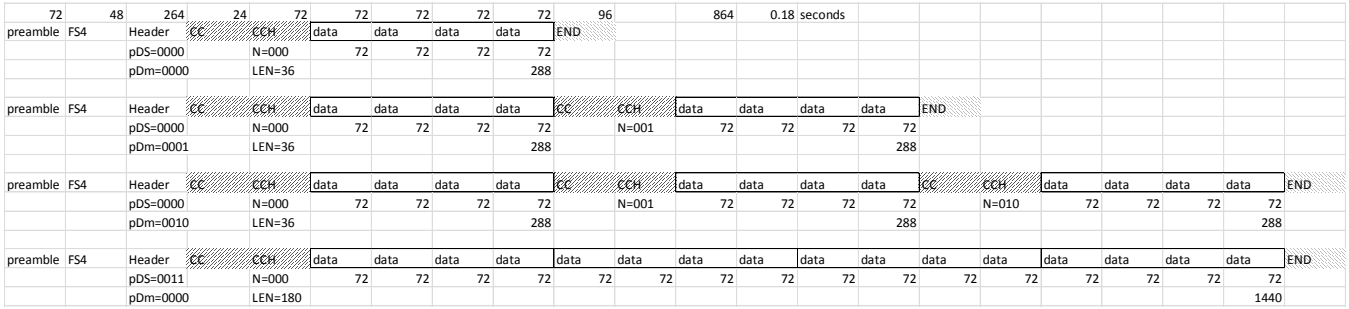


Figure 26 Type-3 Data Formats

Message/Header Block:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	3 Message Type 0				23 Called ID 20				T-Count		Blk ID=00		Byte Count=1001			
1	19 Called ID 4															
2	3 Called ID 0				23 Calling ID 12											
3	11 Calling ID 0												2 M 0			V(b1)
4	V(b0)	1 F 0		EP	PM	2 MI_TYPE 0			7 MI_DET 0							

Aux (Rx)	ID Match			x	Group ID Match				x	x	Colour Code
Aux (Tx)	Repeat Header Count				0	0	0	0	0	0	Colour Code

For the Type-3 Message/Header Block, the contents are:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	3	MT = 0000		0	23	Called ID		20	0	0	0	0	1	0	0	1
1	19	Called ID														4
2	3	Called ID		0	23	Calling ID										12
3	11	Calling ID						0	2	M = 100		0	V(b1)			
4	V(b0)	1	F	0	EP	PM	2	MI (011) 0	3	pDs (0000 - 0011)		0	3	pDm (0000 - 0111)		0

which results in the following data being transferred by the host (in hex):

TxData0	$0009
TxData1	$0000
TxData	$1000
TxData3	$0028
TxData4	$0330

The values for pDs and pDm should be set appropriately for the following data transfers. The value of the Communications Mode field should be set to 100_b, and Message_Info_Type to 011_b (See TS 102 658 5.5.7, 5.5.19.3 and Section 9).

Payload/UDT Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									T-Count		Blk ID=01		Count=0101 or 1001			
1																
2																
3																
4																

SYScast Data (Rx only):

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									T-Count		Blk ID=01		Byte Count=0011			
1										x	x	x	x	x	x	x
2	not used															
3	not used															
4	not used															

CCH Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									T-Count		Blk ID=10		Byte Count=0110			
1																
2																
3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
4	not used															

Aux	ID Match	x	Group ID Match	Colour Code

Type-3 CCH Data:

For the embedded CCH block, the contents are:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	2	N	0	7	LEN			3	0	0	1	0	0	1	1	0
1	2	LEN	0	dummy = 0												
2	0	15	CRC for DATA field													1
3	0	dummy = 0														
4	not used															

which results in the following data being transferred to the host (in hex):

TxData0	$0426	
TxData1	$8000	
TxData2	$091C	Note: an arbitrary CRC value is shown.
TxData3	$0000	
TxData4	not used	

The host MUST supply valid values for all fields in the CCH block as the transmission progresses. In particular, the values of N and the Data CRC field MUST be updated appropriately for each block. This is a significant difference from Type-1 and Type-2 formats (where the FI will do its best to auto-generate the contents of the CCH field, based on the information provided in the initial Message/Header block from the host). All the parameters provided by the host in the CCH block are passed directly “to air”, they are not validated or used internally.

End Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	ET	0	1	ARQ	0	3	Tx_WAIT	0	T-Count		Blk ID=11		Byte Count=011		
1	4	STAT	0	Reserved					x	x	x	x	x	x	x	
2	not used															
3	not used															
4	not used															

6.7.4 Tx Mode (dPMR® Formatted)

In Tx dPMR® Formatted mode ($C1, Modem Control = $0012), the CMX7131/CMX7141 implements all FEC coding, interleaving and scrambling functions for Message Information, UDT Appended Data, Control Channel Information, Payload and End Information blocks, and inserts Frame Sync and Colour Code sequences to generate the required frame formats for transmission. During voice calls the CMX7131/CMX7141 can automatically enable and control the CMX6x8, CMX7262 or SPI-Codec port, and transfer voice payload data from/to it without host intervention.

The host should load Message Information, Control Channel Information and End Information blocks into the TxData registers with fields packed in their over-air format as shown in TS 102 658.

At the start of a transmission the host should preload the TxData registers with the initial Message Information data block before placing the CMX7131/CMX7141 in Tx dPMR® Formatted mode. The device will then send the Preamble, FS1 and Message Frame and will read the ‘Message Type’ field to determine the following burst type that will follow. If the Tx_AuxData register‘ indicates that extended wake-up/repeat Headers are to be sent, the CMX7131/CMX7141 will do so automatically without reloading by the host[4].

[4] Note that this mode of operation was introduced with FI-7.1.2.x onwards to allow the MI field to be used for data transfer operation whilst still allowing the facility for repeated headers, which was not possible with earlier FI’s.

In payload bursts the Header fields are saved for re-use as Control Channel Information fields in the following Payload frames that follow, unless the host loads fresh Control Channel Information blocks during the call.

Unless the 'Message Type' field indicates the burst is a bare Message frame the CMX7131/CMX7141 will now expect the host to load a series of Payload Data, UDT Appended Data and/or End Data blocks as appropriate. For Disconnect bursts which contain a repeated Message/End Frame pair the host should only load single blocks of Header and End Data, and the CMX7131/CMX7141 will then resend the duplicate frames automatically. In Payload bursts the CMX7131/CMX7141 will automatically save and re-use the initial Header fields to build Control Channel Information blocks which are then inserted automatically into each Payload frame. However if Slow Data is being sent (or any other changes to the CCH fields are required) then the host must re-load all four CCH blocks in each super-frame in correct sequence between payload data transfers.

If the CMX6x8 or CMX7262 vocoder is enabled and the 'Communications Mode' field in the Header Frame indicates a voice call, the CMX7131/CMX7141 will automatically enable the vocoder chip microphone input and route payload data from the vocoder for transmission. Note that there is a finite time required to encode the incoming voice data, during which the CMX7131/CMX7141 will automatically insert 'silence' data into the payload frames. Alternatively, if SPI-Codec mode has been enabled, the device will automatically enable the Audio Codec and deliver audio PCM samples to the SPI-Codec port. The host can load an End Frame at any point to terminate the call.

At the end of all dPMR® transmissions the CMX7131/CMX7141 will issue a 'Tx Done' IRQ when it is safe for the host to place the device back into Idle mode ($C1, Modem Control = $0000).

In FI-7.2.0.0 / FI-7.3.0.0 onwards, for Tx (Type-3) packet data, the host must set the Message Type to 0000_b and the Communication Mode field to 100_b in the initial Message/Header block load. This will be intercepted by the FI, which will then route **all** following data transfers through to the Type-3 packet data handler. The host should then provide the appropriate data for the subsequent CCH and payload fields. The number of CCH and payload fields supplied by the host should match the values for pDs, pDm given in the initial message/header block data. Note that there is only limited checking performed on the ordering of the data transfers, so the host must ensure that the correct sequence of CCH and payload blocks is maintained.

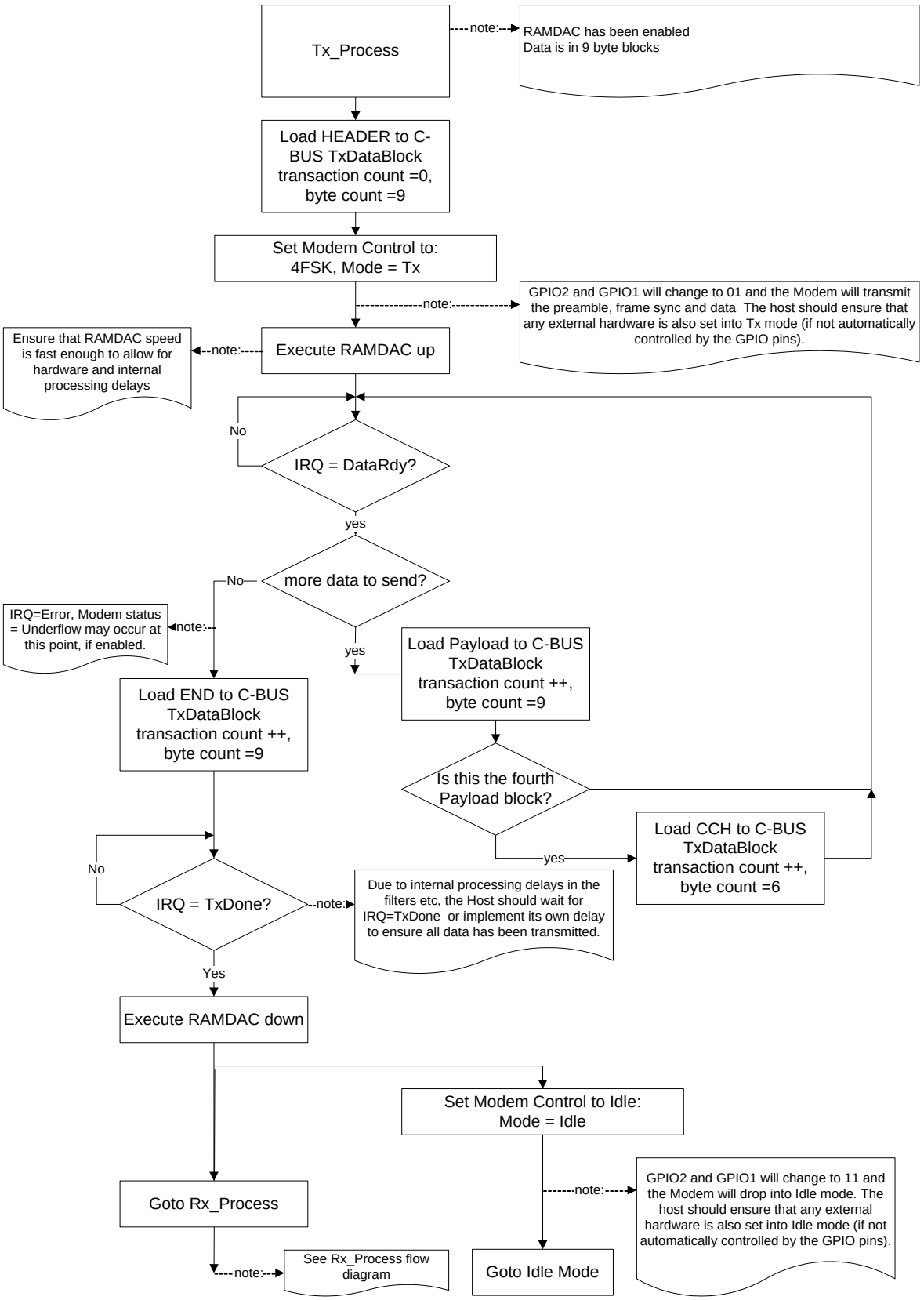


Figure 27 Tx Data Flow

6.7.5 Rx Mode (dPMR® Formatted)

In Rx dPMR® Formatted mode ($C1, Modem Control = $0011) the CMX7131/CMX7141 automatically splits incoming calls to extract Message Information, SYScast data, UDT Appended Data, Control Channel Information, Payload and End Information blocks and performs all the necessary de-scrambling, de-interleaving and FEC decoding functions. In voice calls the CMX7131/CMX7141 can automatically enable the CMX6x8/CMX7262 vocoder or SPI-Codec port when required and transfer received speech data without host intervention.

The RxData registers are used to transfer Message, SYScast, UDT Appended Data, CCH and End Data fields in addition to payload data. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The field layout in the RxData registers for the different transfer types is the same as for Tx dPMR® Formatted mode (section 6.7.3).

To receive a Beacon channel the host should set the BEACON bit (b12) in the Modem Configuration register ($C7) before placing the CMX7131/CMX7141 in Rx dPMR® Formatted mode. Otherwise if this bit is clear the CMX7131/CMX7141 processes incoming transmissions as Traffic channel calls.

When placed in Rx dPMR® Formatted mode the CMX7131/CMX7141 begins scanning for frame sync sequences in the received signal. In addition to detecting the 48-bit FS1 frame sync at the start of a burst, the CMX7131/CMX7141 can also perform 'late entry' into a voice call by detecting two successive copies of the 24-bit FS2 sequence at the correct two-frame spacing. When any valid frame sync sequence has been detected, an 'FS Detect' IRQ is issued and the data demodulator is enabled.

After detecting a frame sync the CMX7131/CMX7141 decodes the contents of the following Message Frame (after an FS1 detect) or Control Channel Information blocks (after an FS2 detect). The Message Information or CCH Information CRCs are checked and processing continues only if valid fields have been received. Message Frames contain two duplicate Message Information blocks and the CMX7131/CMX7141 checks both block CRCs, uses the first valid block and discards the other.

When repeated 'extended wake-up' Header Frames are received (see TS 102 658 section 11.1) the CMX7131/CMX7141 will decode the first valid Header Frame and then ignore all following repeat Headers. This maximises the time the host can be kept in powersave.

After an FS2 detect, if address checking is enabled the CMX7131/CMX7141 will wait to receive all four CCH blocks in a superframe and then repack the fields into the Message Information block format for transfer to the host. If address checking is not enabled the CMX7131/CMX7141 only requires a single valid CCH block to determine the payload type and will immediately start transferring the following CCH and Payload blocks without waiting for a full superframe. The host should collect the remaining address fields from the following CCH blocks as they are transferred.

Address and Colour Code checking can be enabled with b9 and b10 of the Modem Configuration register; otherwise the CMX7131/CMX7141 will accept all incoming calls. The Colour Code is checked first using the Colour Code index specified in the Tx AuxData register ($C2). If the received Colour Code does not match then the burst is rejected. Address checking now takes place depending on the addressing mode selected. Broadcast Messages and headers with the 'Communications Format' field set to 'Call ALL' are always accepted. Otherwise the 'Called ID' is checked against the device's Own IDs (programmed by the host into Program Block 1) and if a match is found the call is accepted. In any of these cases a 'Called' IRQ is issued to the host, otherwise the call is dropped with no further host notification and the CMX7131/CMX7141 returns to frame sync search.

Depending on the burst type the CMX7131/CMX7141 will decode the following Payload, SYScast, UDT Appended Data or End Frames and present their contents to the host or vocoder. If the CMX6x8/CMX7262 Vocoder is enabled and the 'Communication Mode' field in the Header Frame indicates a voice call, the CMX7131/CMX7141 will automatically enable the vocoder chip speaker output and route payload data there for decoding. In this mode, the data is transferred in 4-bit Log-Likelihood-Ratio format. Otherwise payload data is presented to the host in the RxData registers in soft or hard format as specified. When an End Frame is received the CMX7131/CMX7141 will report its contents to the host, disable the vocoder (if necessary) and return to frame sync search.

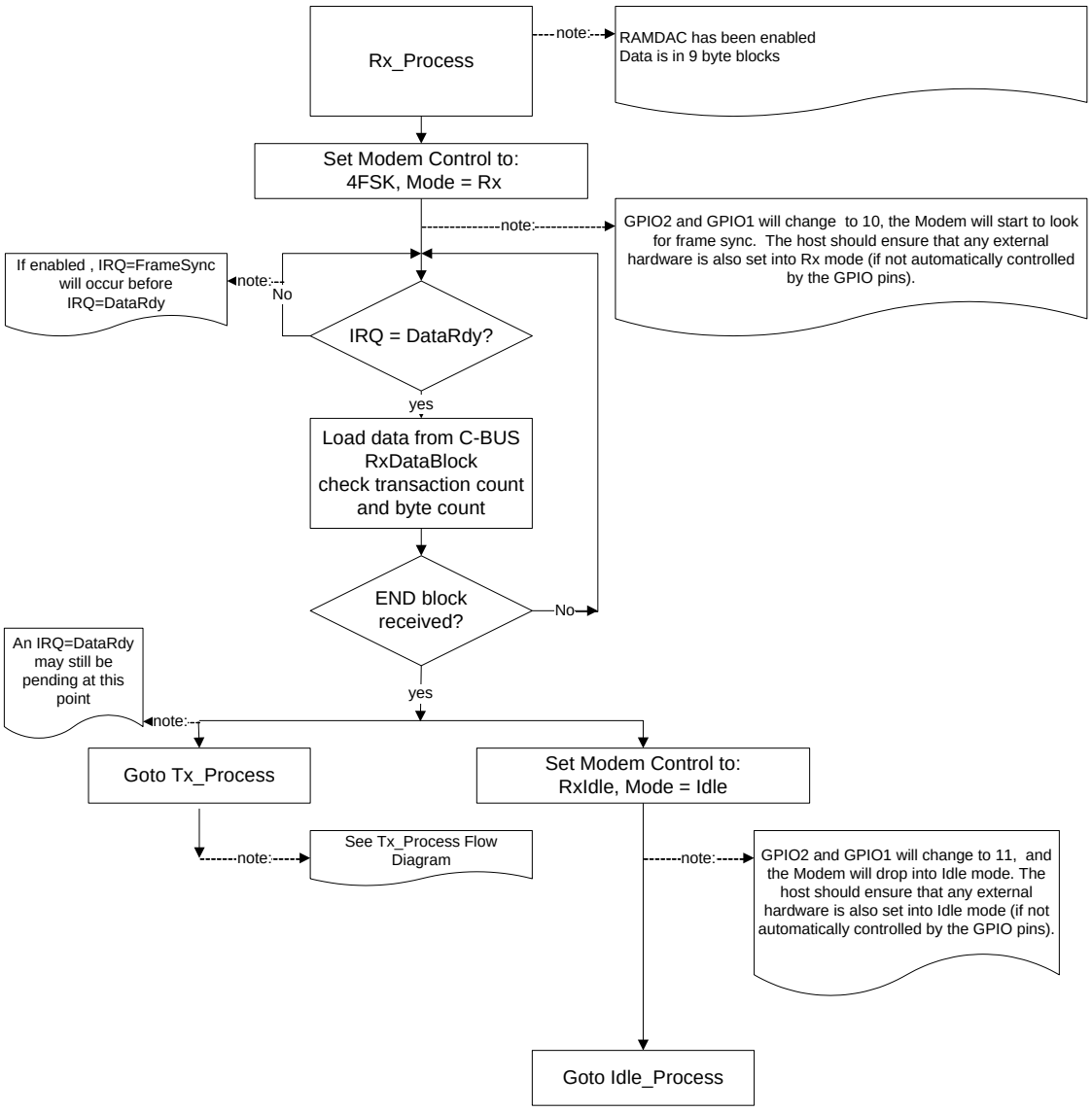


Figure 28 Rx Data Flow

All frame sync sequences, Colour Codes and CRCs contained in payload superframes are checked and an 'Event' IRQ is issued when any are received incorrectly. If all the frame sync sequences, Colour Codes and CRCs in a superframe are received incorrectly, the superframe is considered corrupt. The host can set a threshold for consecutive corrupt superframes (in Program Block 0) after which the CMX7131/CMX7141 will issue an 'Event' IRQ, drop the call and return to frame sync search.

See:

- RxData 0 - $B8 read
- RxAuxData - $CC read.

In Rx, the detection of FS4 has already been implemented. In FI-7.2.0.0 onwards, the protocol to support packet data has been added. In this FI, as soon as FS4 has been detected, the FI will report an FS4 to the host and then return data in the RxData registers using a DATA_IRQ and setting the "Block_type" bits appropriately for header, payload or CCH. Once an END frame has been detected, it will assume that the burst has completed. Unlike normal reception, all data will be transferred to the host until the END frame has been detected or the pDs / pDm counters expire. Any errors in the transmission should be detected by

the host (using the CRC field in each CCH block) and the appropriate ACK or NACK frame be returned to the originating unit after the full burst has completed (see TS 102 658 section 9.7)

6.7.6 Slow Data

The CCH Data block in each frame contains two 9-bit words of Slow Data which should be handled as necessary by the host. In Tx mode CCH Data block transfers are optional and if not reloaded the CMX7131/CMX7141 will re-use the CCH fields from the preceding superframe or Message frame. When fresh CCH Data blocks are supplied then all four CCH Data blocks in the current superframe must be reloaded. In Rx mode the received CCH Data blocks are always transferred to the host.

6.8 Squelch Operation

Many limiter/discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be routed directly to one of the CMX7131/CMX7141's GPIO pins or to the host. However with the CMX7131/CMX7141, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.

See:

- IRQ Status - $C6 read
- Modem Configuration - $C7 write.

Note: This functionality is not necessary in I/Q mode as squelch detection is within CMX7131/CMX7141 signal processing however the AuxADC functionality remains available.

6.9 GPIO Pin Operation

The CMX7131/CMX7141 provides four GPIO pins: GPIO1, GPIO2, GPIOA and GPIOB. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:

- Modem Configuration - $C7 write.

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7131/CMX7141. This is to allow the host sufficient time to load the relevant data buffers and the CMX7131/CMX7141 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is output, high level. When set for input, the values can be read back using the Modem Status register, $C9.

6.10 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Configuration register, $A7. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to 'off'. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Configuration register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,

1 = 25% of the current value will be added to 75% of the last average value,

2 = 12.5% etc.

The maximum useful value of this field is 9.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 29. The thresholds are programmed via the Aux Config register, $CD. See Figure 29.

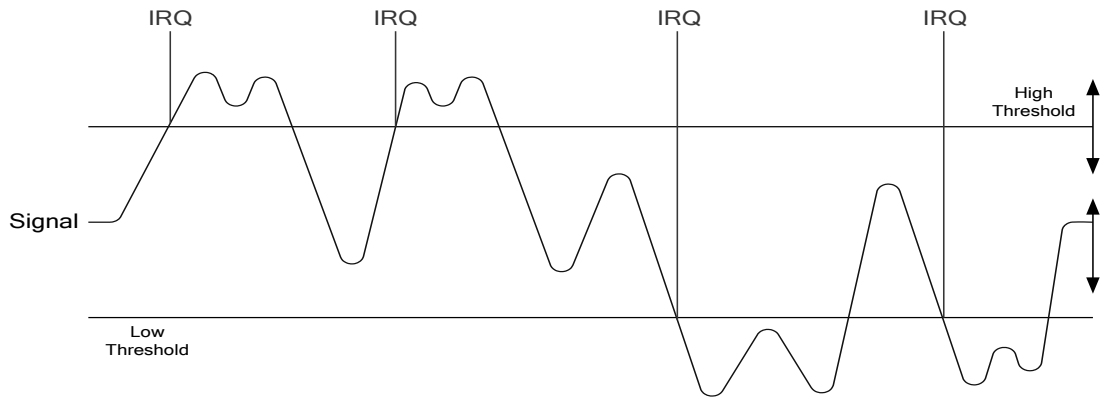


Figure 29 AuxADC IRQ Operation

Auxiliary ADC data is read back in the Aux 1 Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- AuxADC Configuration - $A7 write
- Aux 1 Data and Status - $A9 read
- Aux 2 Data and Status - $AA read
- Aux Config $CD write.

6.11 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Data/Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Data/Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 20), but this may be over-written

with a user-defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Data/Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

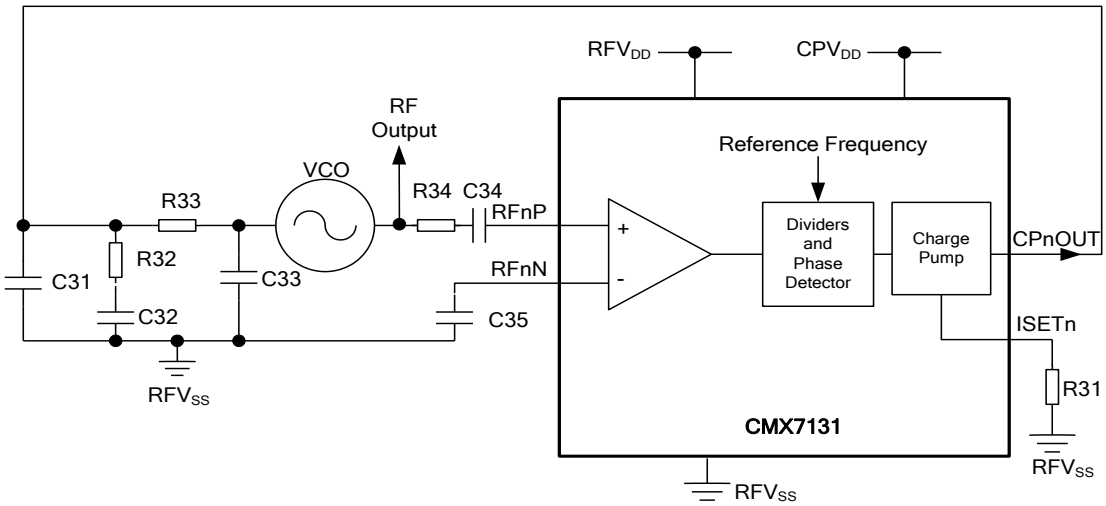
See:
- AuxDAC Data and Control - $A8 write.

6.12 RF Synthesiser (CMX7131 only)

The CMX7131 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Synthesiser Data - $B2 write
- RF Synthesiser Control - $B3 write
- RF Synthesiser Status - $B4 8-bit read.

External RF components are needed to complete the synthesiser circuit. A typical schematic for a 446MHz synthesiser (3.125kHz comparison frequency) is shown in Figure 30.



Note: n = 1 or 2 for Synthesiser 1 or 2

Figure 30 Example RF Synthesiser Components

R31	0Ω	C31	22nF
R32	5.6kΩ	C32	470nF
R33	10kΩ	C33	10nF
R34	100Ω	C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7131 is kept as short as possible. The loop filter components should be placed close to the VCO.

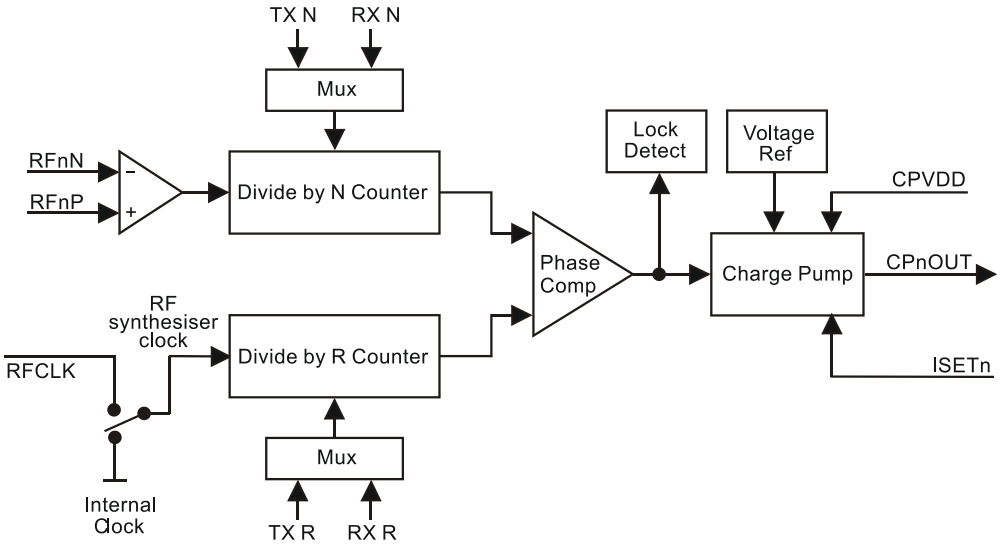


Figure 31 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 31 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL and the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both synthesisers. The charge pump supply (CP supply, CPVDD) is also common to both synthesisers. The RFnP and RFnN input pins, CPnOUT, ISETn and RFVSS pins are channel specific and designated as either RF1P, RF1N, CP1OUT, ISET1, RFVSS or RF2P, RF2N, CP2OUT, ISET2, RFVSS on the Signal List in section 3. The N and R values for Tx and Rx modes are synthesiser specific and can be set from the host µC via the C-BUS. Various synthesiser specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 30.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFVSS pin. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

gain bit set to 1: $R31\ (\text{in } \Omega) = (24/I_{CP}) - 9600$
gain bit cleared to 0: $R31\ (\text{in } \Omega) = (6/I_{CP}) - 9600$
where I_{CP} is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The 'gain bit' refers to either bit 3 or bit 11 in the RF Synthesiser Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N/R) \times F_{REF}$$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low)

Since the set-up for the PLLs takes four 'RF Synthesiser Data register' writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the 'RF Synthesiser Data register' on a PLL that is disabled, powersaved or selected to work from the alternate register set ('Tx' and 'Rx' are alternate register sets). There are no interlocks to enforce this intention. The names 'Tx' and 'Rx' are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (the RF synthesiser clock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Synthesiser Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a four-cycle tolerance is for the case where a high frequency reference oscillator would not forgive a small phase error.

RF Inputs

The RF inputs are differential and self-biased (when not powersaved). They are intended to be capacitatively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the 'P' and 'N' inputs capacitatively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitive and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14V/µs minimum.
- The RF Synthesiser 2.5V digital supply can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating.
- It is recommended that the RF Synthesisers are operated with maximum charge pump gain (i.e. ISET tied to RFVSS).
- The loop filter components should be optimised for each VCO.

6.13 Digital System Clock Generators

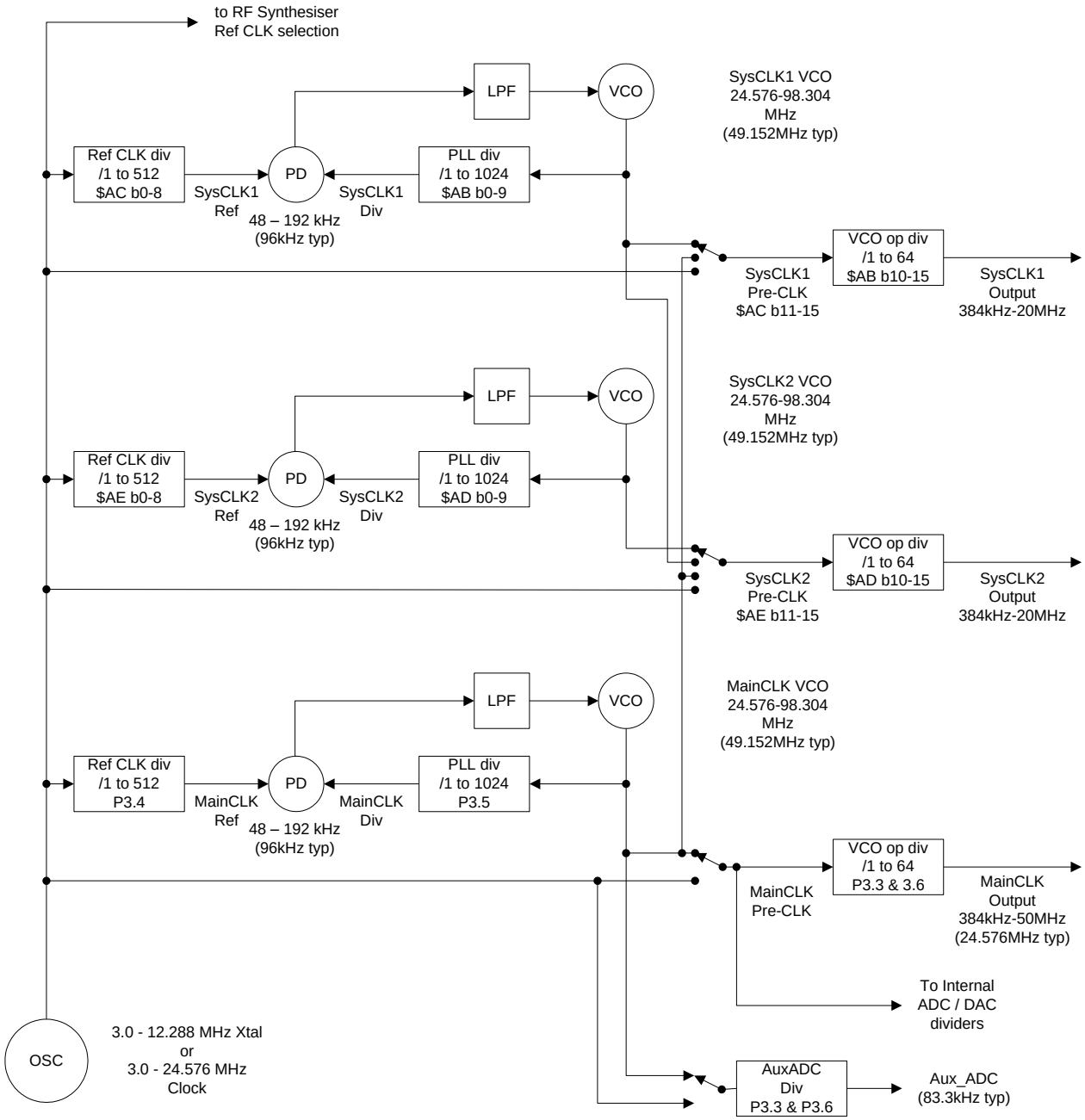


Figure 32 Digital Clock Generation Schemes

The CMX7131/CMX7141 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 4.2, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7131/CMX7141.

6.13.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7131/CMX7141. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7131/CMX7141 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.2 to P3.7 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 7.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control.

6.13.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 32. Note that at power-on, these pins are disabled.

See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC and $AE write.

6.14 Signal Level Optimisation

The internal signal processing of the CMX7131/CMX7141 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage.

6.14.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment ($C3) has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to +40.0dB and no gain.

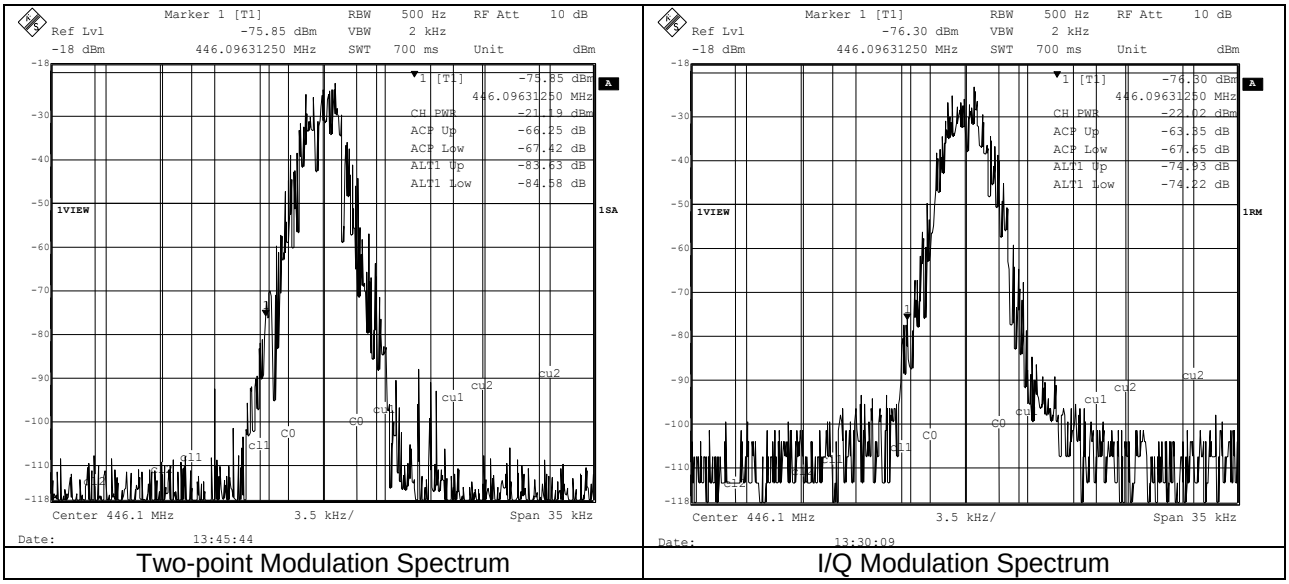
6.14.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4dB and no attenuation. In LD mode with the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mVrms. This signal level is an absolute maximum, which should not be exceeded.

In I/Q mode CMX7131/CMX7141 automatically manages the gain control settings to optimise signal levels.

6.15 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX7131/CMX7141 internal PRBS generator. Note that the I/Q mode is sensitive to variations in dc offset in the modulation path and these must be minimised.



Two-point Modulation Spectrum	I/Q Modulation Spectrum

Figure 33 Tx Modulation Spectra – 4.8kbps

6.16 C-BUS Register Summary

Table 16 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data and Control	16
$A9	R	Aux 1 Data and Status/Checksum 2 hi	16
$AA	R	Aux 2 Data and Status/Checksum 2 lo	16
$AB	W	SYSCLK 1 PLL Data	16
$AC	W	SYSCLK 1 Ref	16
$AD	W	SYSCLK 2 PLL Data	16
$AE	W	SYSCLK 2 Ref	16
$AF		*Reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*Reserved*	
$BD		*Reserved*	
$BE		*Reserved*	
$BF		*Reserved*	
$C0	W	Power Down Control	16
$C1	W	Modem Control	16
$C2	W	TxAuxData	16
$C3	W	Vocoder Control	16
$C4		*Reserved*	
$C5	R	Rx Data 4	16
$C6	R	IRQ Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	RxAuxData	16
$CD	W	Aux Config	16
$CE	W	Interrupt Mask	16
$CF		*Reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
CPV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS, CPVDD, RFVDD or RFVSS)	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD} (CMX7131 only)	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS} (CMX7131 only)	0	50	mV
AV_{SS} and RFV_{SS} (CMX7131 only)	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$ (CMX7131 only)		3.0	3.6	V
$RFV_{DD} – DV_{SS}$ (CMX7131 only)	3	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using an Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes:
1 Nominal XTAL/CLK frequency is 19.2MHz.
2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.
3 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2. Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} (CMX7131) = 3.0V to 3.6V; RFV_{DD} (CMX7131) = 2.25V to 2.75V.
V_{DEC} = 2.5V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with 7131/7141FI-7.1.x only. The use of other CMX7131/CMX7141 Function Images, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode (LD Mode)	22				
DI_{DD} (4.8kbps – search for FS)		–	4.7	–	mA
DI_{DD} (4.8kbps – FS found)		–	2.8	–	mA
AI_{DD}		–	1.6	–	mA
Rx Mode (I/Q Mode)	22				
DI_{DD} (4.8kbps – search for FS)		–	10.2	–	mA
DI_{DD} (4.8kbps – FS found)		–	7.4	–	mA
AI_{DD}		–	6.9	–	mA
Tx Mode	22				
DI_{DD} (4.8kbps – two-point)		–	4.3	–	mA
DI_{DD} (4.8kbps – I/Q)		–	5.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	–	mA
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
Additional Current for each RF Synthesiser	24				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA

Notes: *(see next page)*

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
'Off' State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:

21 T_{AMB} = 25°C: not including any current drawn from the device pins by external circuitry.

22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

24 When using the external components shown in Figure 30 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
System Clk 1/2 Outputs						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at dc.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured with respect to nominal V_{BIAS} output.

57 Measured at dc.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic 1	62	70%	–	–	RFV_{DD}
Input Logic 0	62	–	–	30%	RFV_{DD}
Frequency	64, 66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level		−15	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (I_{CP}) (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (I_{CP}) (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink-to-source match		–	5%	–	of I_{CP}

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. Below 150MHz, a square wave input may be required to provide a fast enough slew rate.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:

Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$.

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (e.g. RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (e.g. IF LO).

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2. Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V. Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal-to-Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-7.1.x only. The use of other CMX7131/CMX7141 Function Images can modify the parametric performance of the device.

dPMR® Modem	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		–	2400	–	symbols/s
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, two-point)	70	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	70	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	71, 73	-60	–	–	dB
Rx Sensitivity (1% BER, I/Q mode)	72, 74	–	-122	–	dBm
Rx Co-channel Rejection	71, 73	15	12	–	dB
Rx System Adjacent Channel Rejection (I/Q Mode)	74	–	63		dB
Rx Input Level		–	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD} - 0.5	V

Notes:
70 Transmitting continuous default preamble.
71 See user manual section 6.15.
72 Measured at baseband – radio design will affect ultimate product performance.
73 For a 6.25kHz/4.8kbps channel.
74 Combined performance of CMX7131/CMX7141 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201; measurement method from EN 301 166.

7.2 C-BUS Timing

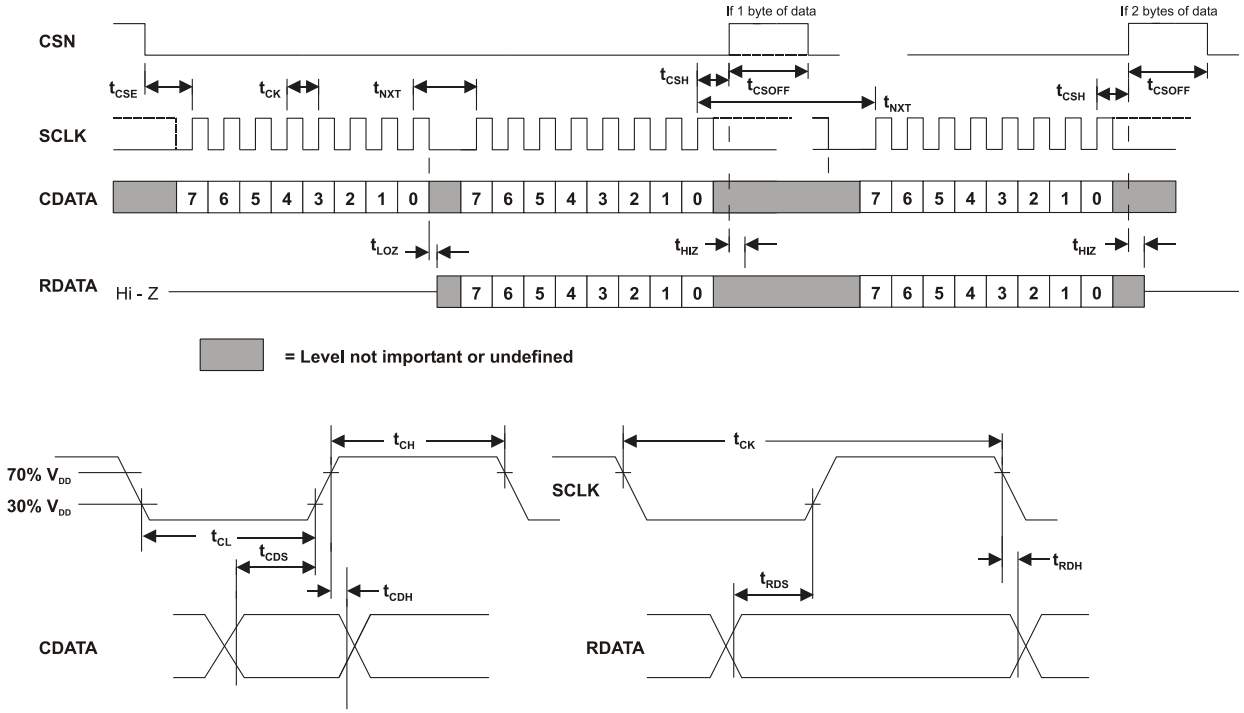


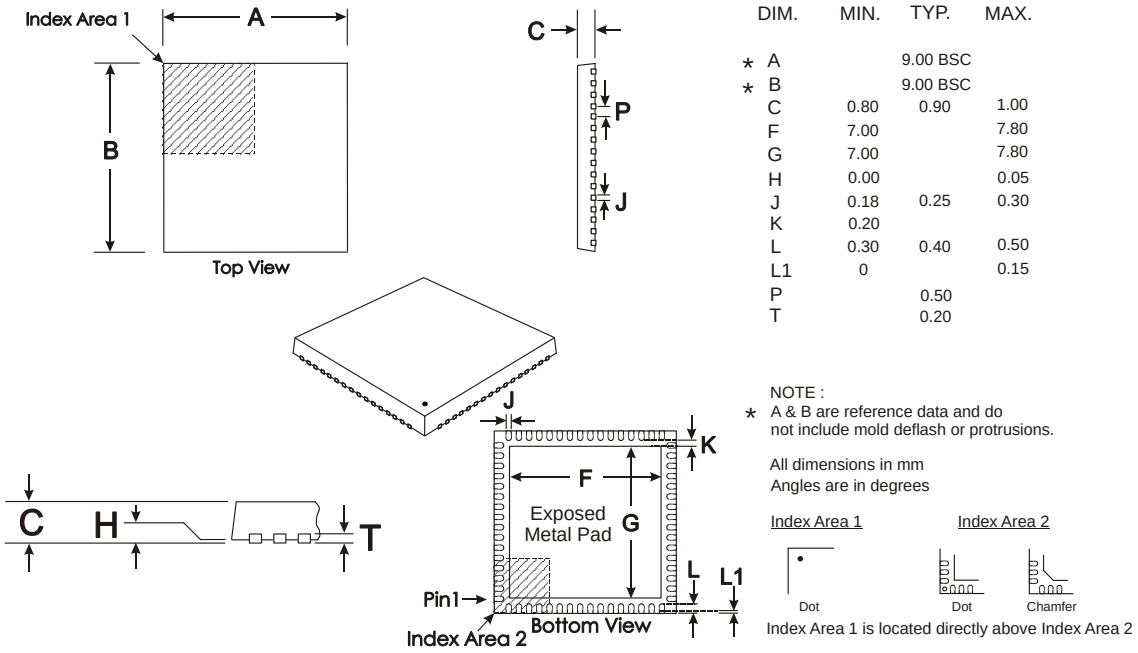
Figure 34 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7131/CMX7141 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

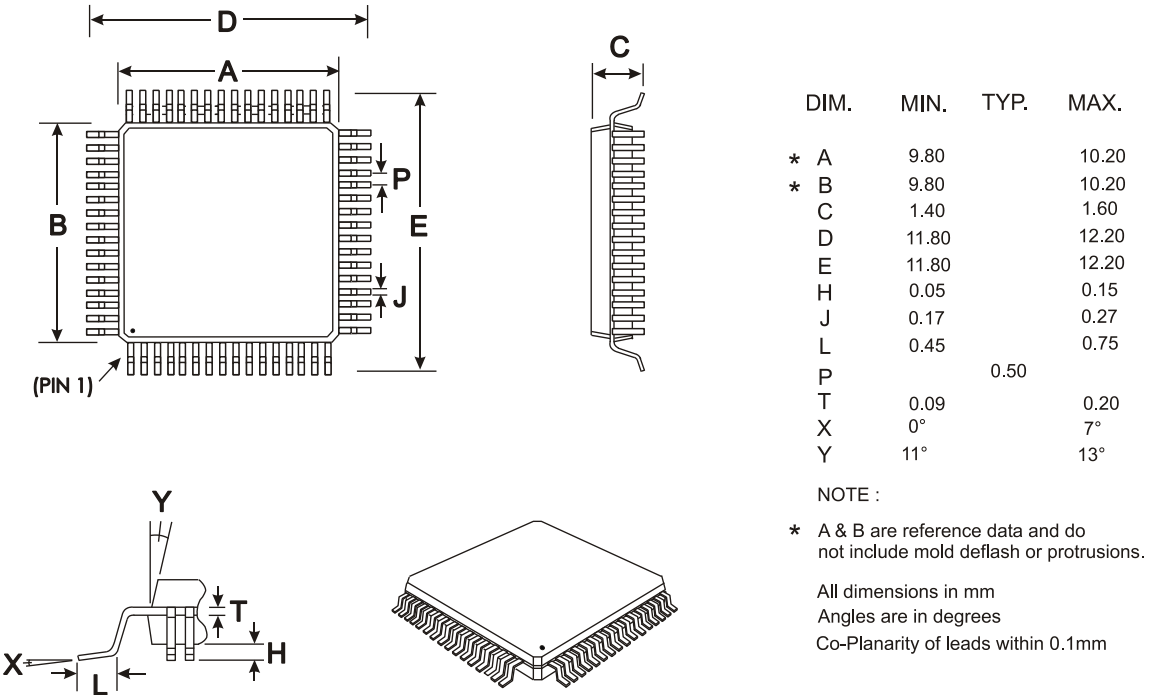
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 35 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7131Q1



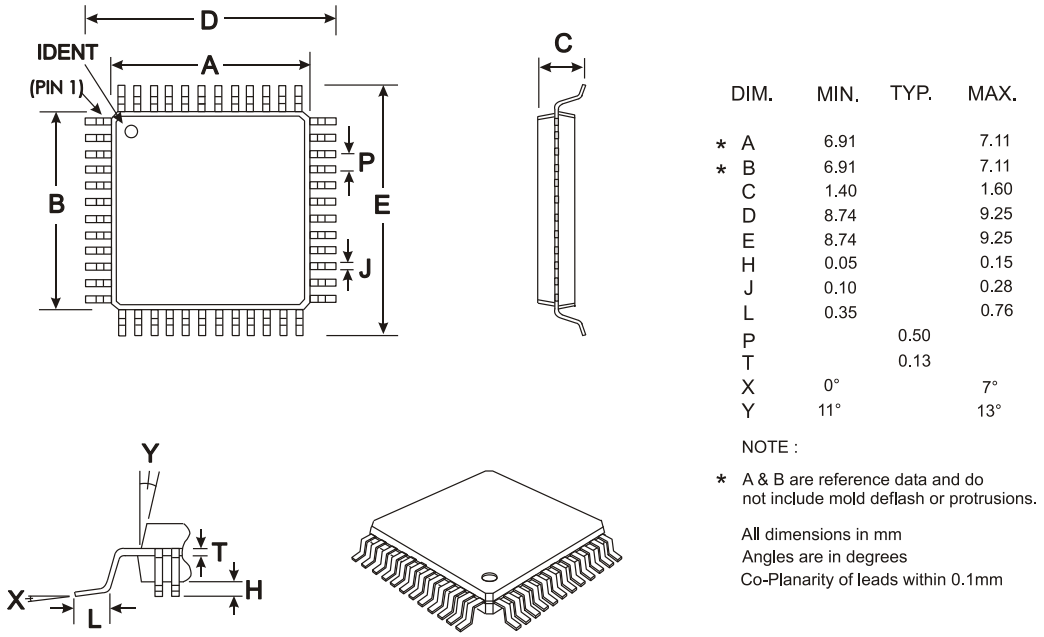
	DIM.	MIN.	TYP.	MAX.
*	A	9.80		10.20
*	B	9.80		10.20
	C	1.40		1.60
	D	11.80		12.20
	E	11.80		12.20
	H	0.05		0.15
	J	0.17		0.27
	L	0.45		0.75
	P		0.50	
	T	0.09		0.20
	X	0°		7°
	Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 36 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7131L9



	DIM.	MIN.	TYP.	MAX.
*	A	6.91		7.11
*	B	6.91		7.11
	C	1.40		1.60
	D	8.74		9.25
	E	8.74		9.25
	H	0.05		0.15
	J	0.10		0.28
	L	0.35		0.76
	P		0.50	
	T		0.13	
	X	0°		7°
	Y	11°		13°

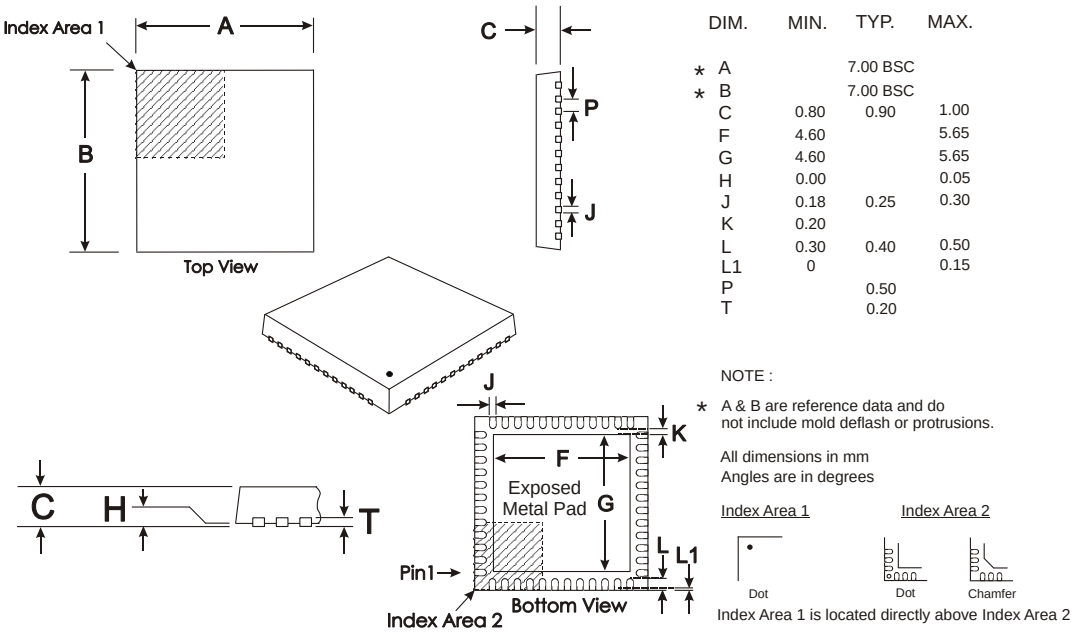
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 37 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7141L4



	DIM.	MIN.	TYP.	MAX.
*	A		7.00 BSC	
*	B		7.00 BSC	
	C	0.80	0.90	1.00
	F	4.60		5.65
	G	4.60		5.65
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 38 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7141Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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