CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

July 02, 2014

Dear Sir/Madam: PCN# 070214

Subject: Notification of Change to LTC2481 Datasheet

Please be advised that Linear Technology Corporation has made a change to the LTC2481 specification in order to improve device manufacturability. The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 4000kHz to 1000kHz . This is also noted in the text and in the graphs of performance vs. sample rate in Figures 20 to 27 of the attached datasheet. Performance degrades at high sample rates as shown in the figures, and an external oscillator frequency of 1000kHz is a more conservative maximum. In addition, the on-chip PTAT signal (Internal PTAT Signal) performance has been clarified as shown in the attached datasheet. No changes are being made to the circuit or the test methodology. Product shipped after September 3, 2014 will be tested to the new limit.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by email at JASON.HU@LINEAR.COM. If I do not hear from you by September 3, 2014, we will consider this change to be approved by your company.

Sincerely,

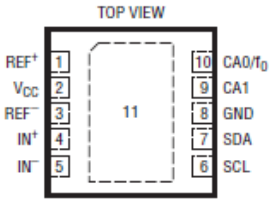
Jason Hu
Quality Assurance Engineer

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2481C..... 0°C to 70°C
LTC2481I .....–40°C to 85°C
LTC2481H .....–40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2481CDD#PBF	LTC2481CDD#TRPBF	LBPV	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2481IDD#PBF	LTC2481IDD#TRPBF	LBPV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2481HDD#PBF	LTC2481HDD#TRPBF	LBPV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1 ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)	●	16			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = $IN^–$ ≤ V_{CC} (Note 13)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = $IN^–$ ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF} 2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF} (H-Grade)	●			25 40	ppm of V_{REF} ppm
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, $IN^–$ = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, $IN^–$ = 0.75V_{REF}, IN^+ = 0.25V_{REF} 2.5V ≤ V_{REF} ≤ V_{CC}, $IN^–$ = 0.75V_{REF}, IN^+ = 0.25V_{REF} (H-Grade)	●			25 40	ppm of V_{REF} ppm
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, $IN^–$ = 0.75V_{REF}, IN^+ = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6) 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, GND ≤ $IN^–$ = IN^+ ≤ V_{CC} (Note 12)			0.6		μV_{RMS}
Internal PTAT Signal	T_A = 27°C		390	420	450	mV
~~Internal PTAT Temperature Coefficient~~				~~1.4~~		~~mV/°C~~
Programmable Gain	See Table 2a	●	1		256	

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	10		1000 ~~4000~~	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		50Hz Mode (H-Grade)	●	157.2	160.3	165.1	ms
		60Hz Mode	●	131.0	133.6	136.3	ms
		60Hz Mode (H-Grade)	●	131.0	133.6	137.6	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		Simultaneous 50Hz/60Hz Mode (H-Grade)	●	144.1	146.9	151.0	ms
		External Oscillator (Note 10)	●		41036/f_{EOSC}		ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		50Hz Mode (H-Grade)	●			82.7	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		60Hz Mode (H-Grade)	●			68.9	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		Simultaneous 50Hz/60Hz Mode (H-Grade)	●			75.6	ms
		External Oscillator (Note 10)	●		20556/f_{EOSC}		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for Both SDA and SCL Signals	(Note 14)	●	20+0.1C_B		300	ns
t_f	Fall Time for Both SDA and SCL Signals	(Note 14)	●	20+0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

$V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$, FS = 0.5$V_{REF}$/GAIN; $V_{IN} = IN^+ – IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the CA0/f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses the internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

Note 14: C_B = capacitance of one bus line in pF.

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

APPLICATIONS INFORMATION

In applications where the reference and input common mode voltages are different, extra errors are introduced. For every 1V of the reference and input common mode voltage difference ($V_{REFCM} - V_{INCM}$) and a 5V reference, each Ohm of reference source resistance introduces an extra $(V_{REFCM} - V_{INCM})/(V_{REF} \bullet R_{EQ})$ full-scale gain error, which is 0.074ppm when using internal oscillator and 60Hz mode. When using internal oscillator and 50Hz/60Hz mode, the extra full-scale gain error is 0.067ppm. When using internal oscillator and 50Hz mode, the extra gain error is 0.061ppm. If an external clock is used, the corresponding extra gain error is $0.24 \bullet 10^{-6} \bullet f_{EOSC}$ppm.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by V_{REF}^+ and V_{REF}^-, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±100nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 5µV maximum full-scale error.

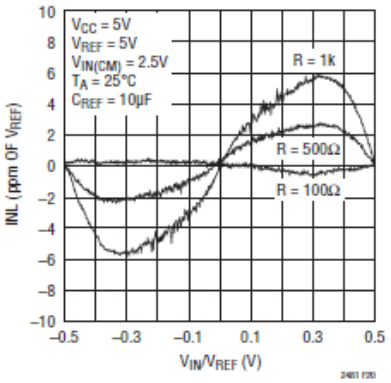


Figure 20. INL vs DIFFERENTIAL Input Voltage and Reference Source Resistance for C_{REF} > 1µF

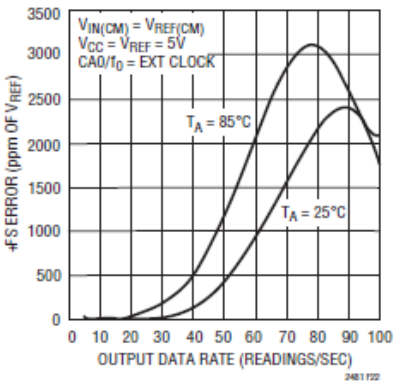


Figure 22. +FS Error vs Output Data Rate and Temperature

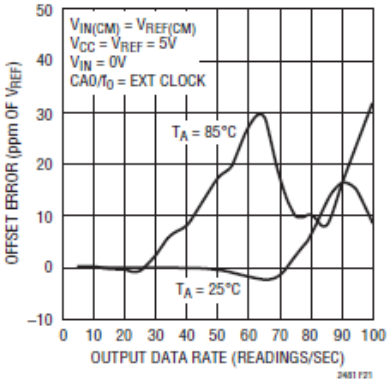


Figure 21. Offset Error vs Output Data Rate and Temperature

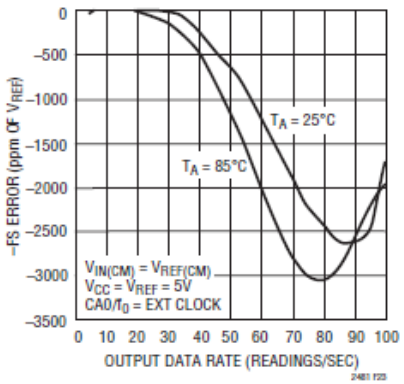


Figure 23. –FS Error vs Output Data Rate and Temperature

APPLICATIONS INFORMATION

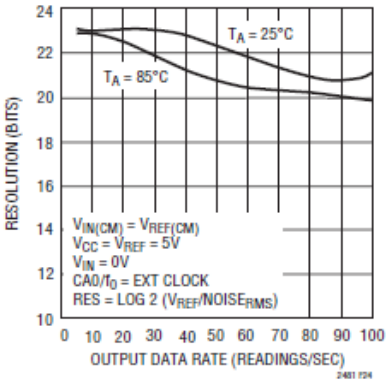


Figure 24. Resolution (Noise$_{RMS}$ ≤ 1LSB) vs Output Data Rate and Temperature

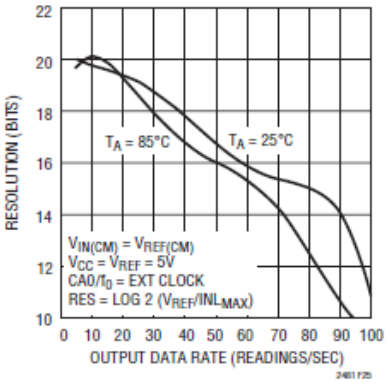


Figure 25. Resolution (INL$_{MAX}$ ≤ 1LSB) vs Output Data Rate and Temperature

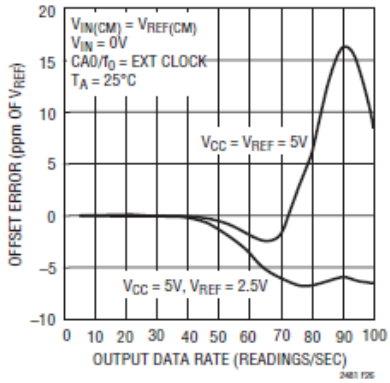


Figure 26. Offset Error vs Output Data Rate and Reference Voltage

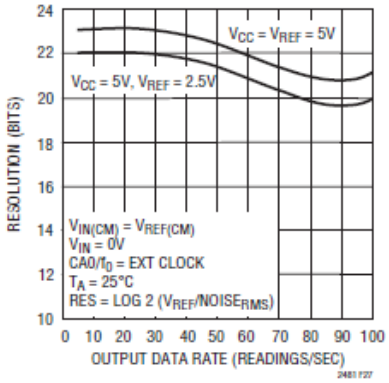


Figure 27. Resolution (Noise$_{RMS}$ ≤ 1LSB) vs Output Data Rate and Reference Voltage

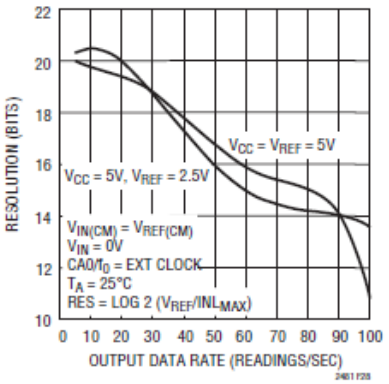


Figure 28. Resolution (INL$_{MAX}$ ≤ 1LSB) vs Output Data Rate and Reference Voltage

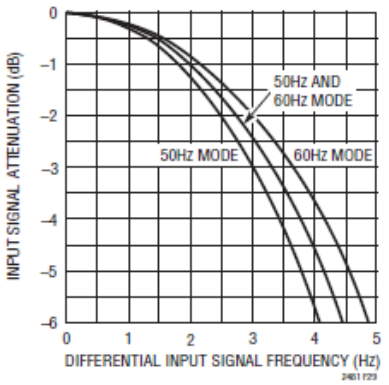


Figure 29. Input Signal Using the Internal Oscillator

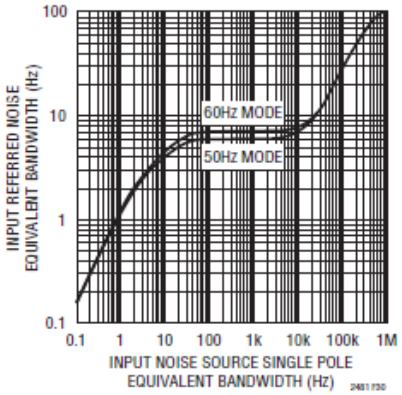


Figure 30. Input Referred Noise Equivalent Bandwidth of an Input Connected White Noise Source