

74ACQ373 • 74ACTQ373

Quiet Series™ Octal Transparent Latch with 3-STATE Outputs

General Description

The ACQ/ACTQ373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the HIGH impedance state.

The ACQ/ACTQ373 utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

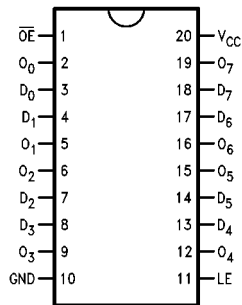
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch up immunity
- Eight latches in a single package
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC/ACT373

Ordering Code:

Order Number	Package Number	Package Description
74ACQ373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACQ373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACQ373PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001m 0.300" Wide
74ACTQ373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACTQ373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ373QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74ACTQ373PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001m 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

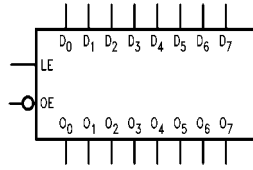


Pin Descriptions

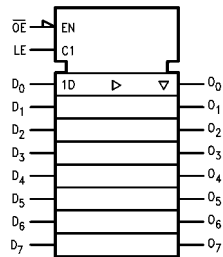
Pin Names	Description
D_0 - D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O_0 - O_7	3-STATE Latch Outputs

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Logic Symbols



IEEE/IEC



Functional Description

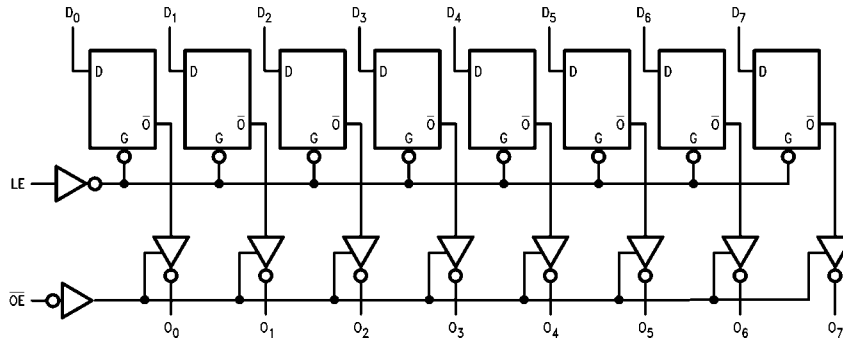
The ACQ/ACTQ373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	\overline{OE}	D _n	O _n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial
 O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latchup Source	
or Sink Current	± 300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACTQ Devices	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)	
		4.5		3.86	3.76			
5.5		4.86	4.76					
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)	
		4.5		0.36	0.44			
5.5		0.36	0.44					
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, GND$	
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
I_{OHD}	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.25	± 2.5	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 5)(Note 6)	
V_{OLV}	Quiet Output Maximum Dynamic V_{OL}	5.0	-0.6	-1.2		V	Figure 2, Figure 2 (Note 5)(Note 6)	

DC Electrical Characteristics for ACQ (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Note 5)(Note 7)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: DIP package.

Note 6: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 7: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for ACTQ

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions	
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
			4.5		3.86	3.76	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 8)
			5.5		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
			4.5		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 8)
			5.5		0.36	0.44		
I _{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 9)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} , or GND	
V _{OLP}	Quiet Output	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 10)(Note 11)	
	Maximum Dynamic V _{OL}							
V _{OLV}	Quiet Output	5.0	-0.6	-1.2		V	Figure 1, Figure 2 (Note 10)(Note 11)	
	Minimum Dynamic V _{OL}							
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 10)(Note 12)	
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 10)(Note 12)	

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

Note 10: Plastic DIP package.

Note 11: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 12: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics for ACQ								
Symbol	Parameter	V _{CC} (V) (Note 13)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay	3.3	2.5	8.0	10.5	2.5	11.0	ns
t _{PLH}	D _n to O _n	5.0	1.5	5.5	7.0	1.5	7.5	
t _{PHL}	Propagation Delay	3.3	2.5	8.0	12.0	2.5	12.5	ns
t _{PLH}	LE to O _n	5.0	2.0	6.0	8.0	2.0	8.5	
t _{PZL}	Output Enable Time	3.3	2.5	8.5	13.0	2.5	13.5	ns
t _{PZH}		5.0	1.5	6.5	8.5	1.5	9.0	
t _{PHZ}	Output Disable Time	3.3	1.0	9.0	14.5	1.0	15.0	ns
t _{PLZ}		5.0	1.0	6.5	9.5	1.0	10.0	
t _{OSHL}	Output to Output Skew	3.3		1.0	1.5		1.5	ns
t _{OSLH}	D _n to O _n (Note 14)	5.0		0.5	1.0		1.0	

Note 13: Voltage Range 5.0 is 5.0V ± 0.5V.
Voltage Range 3.3 is 3.3V ± 0.3V.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements for ACQ							
Symbol	Parameter	V _{CC} (V) (Note 15)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
t _S	Setup Time, HIGH or LOW	3.3	0	3.0	3.0		ns
	D _n to LE	5.0	0	3.0	3.0		
t _H	Hold Time, HIGH or LOW	3.3	0	1.5	1.5		ns
	D _n to LE	5.0	0	1.5	1.5		
t _W	LE Pulse Width, HIGH	3.3	2.0	4.0	4.0		ns
		5.0	2.0	4.0	4.0		

Note 15: Voltage Range 5.0 is 5.0V ± 0.5V.
Voltage Range 3.3 is 3.3V ± 0.3V.

AC Electrical Characteristics for ACTQ								
Symbol	Parameter	V _{CC} (V) (Note 16)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay	5.0	2.0	6.5	7.5	2.0	8.0	ns
t _{PLH}	D _n to O _n							
t _{PHL}	Propagation Delay	5.0	2.5	7.0	8.5	2.5	9.0	ns
t _{PLH}	LE to O _n							
t _{PZL}	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns
t _{PZH}								
t _{PHZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns
t _{PLZ}								
t _{OSHL}	Output to Output Skew	5.0		0.5	1.0		1.0	ns
t _{OSLH}	D _n to O _n (Note 17)							

Note 16: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 17: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements for ACTQ

Symbol	Parameter	V _{CC} (V) (Note 18)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum			
t _S	Setup Time, HIGH or LOW D _n to LE	5.0	0	3.0	3.0		ns
t _H	Hold Time, HIGH or LOW D _n to LE	5.0	0	1.5	1.5		ns
t _W	LE Pulse Width, HIGH	5.0	2.0	4.0	4.0		ns

Note 18: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	44.0	pF	V _{CC} = 5.0V

FACT Noise Characteristics

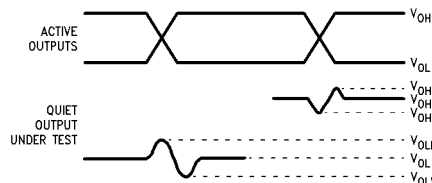
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics:

$f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next decrease the input HIGH voltage level, V_{IH} until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

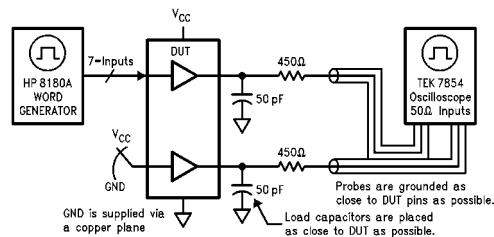
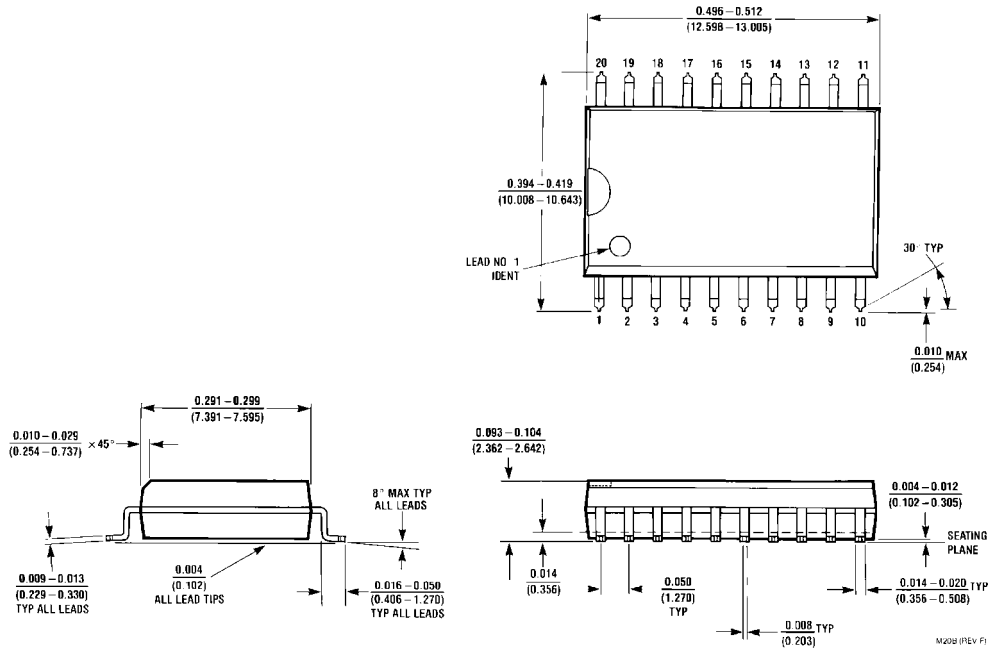


FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

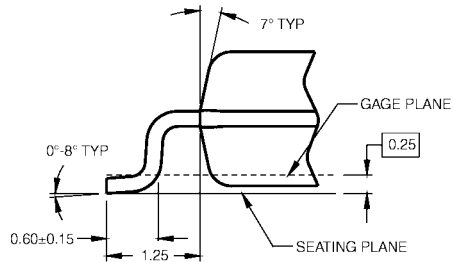
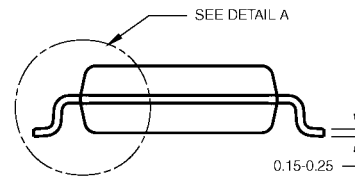
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



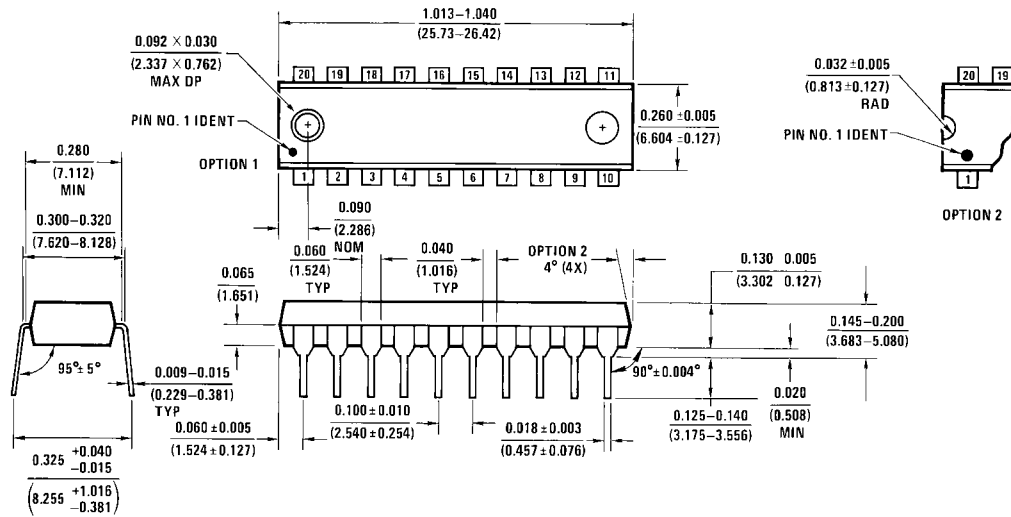
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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