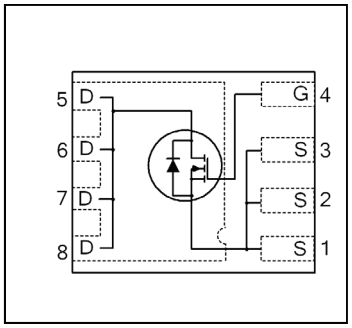
HEXFET® Power MOSFET

V_{DSS}	100	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	16.4	mΩ
Qg (typical)	13	nC
Rg (typical)	2.0	Ω
I_D ($@T_{C\ (Bottom)}$ = 25°C)	34	A



PQFN 3.3 x 3.3 mm

Applications

- Primary Switch for High Frequency 48V/60V Telecom DC-DC Power Supplies
- Secondary Side Synchronous Rectifier

Features		Benefits
Low R_{DSon} (<16.4mΩ)		Lower Conduction Losses
Low Charge (typical 13nC)		Low Switching Losses
Low Thermal Resistance to PCB (<3.4°C/W)		Enable better thermal dissipation
Low Profile (<0.9 mm)	results in	Increased Power Density
Industry-Standard Pinout	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Industrial Qualification		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM7194TRPbF	PQFN 3.3mm x 3.3mm	Tape and Reel	4000	IRFHM7194TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.3	A
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V	34	
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_{DM}	Pulsed Drain Current ①	95	
P_D @T_A = 25°C	Power Dissipation ⑤	2.8	W
P_D @$T_{C(Bottom)}$ = 25°C	Power Dissipation ⑤	37	
	Linear Derating Factor ⑤	0.022	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑤ are on page 8

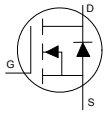
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	48	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	13.7	16.4	mΩ	V_{GS} = 10V, I_D = 20A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	3.6	V	V_{DS} = V_{GS}, I_D = 50µA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.5	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 80V, V_{GS} = 0V
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	45	—	—	S	V_{DS} = 25V, I_D = 20A
Q_g	Total Gate Charge	—	13	19	nC	V_{DS} = 50V V_{GS} = 10V I_D = 20A
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	1.8	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	0.9	—		
Q_{gd}	Gate-to-Drain Charge	—	4.3	—		
Q_{godr}	Gate Charge Overdrive	—	6.0	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	5.2	—		
Q_{oss}	Output Charge	—	40	—	nC	V_{DS} = 50V, V_{GS} = 0V
R_G	Gate Resistance	—	2.1	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	2.7	—	ns	V_{DD} = 50V, V_{GS} = 10V I_D = 20A R_G= 1.0Ω
t_r	Rise Time	—	3.3	—		
$t_{d(off)}$	Turn-Off Delay Time	—	8.0	—		
t_f	Fall Time	—	2.5	—		
C_{iss}	Input Capacitance	—	733	—	pF	V_{GS} = 0V V_{DS} = 50V f = 1.0MHz
C_{oss}	Output Capacitance	—	374	—		
C_{rss}	Reverse Transfer Capacitance	—	11	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	—	220	mJ
I_{AR}	Avalanche Current ①	—	12	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	34	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	95		
V_{SD}	Diode Forward Voltage	—	0.8	1.3	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	30	45	ns	T_J = 25°C, I_F = 20A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	—	26	39	nC	di/dt = 100A/µs ③

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	3.4	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	35	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	45	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	29	

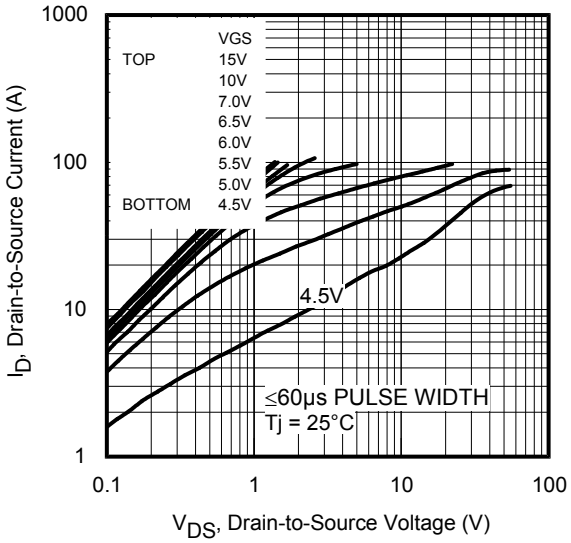


Fig 1. Typical Output Characteristics

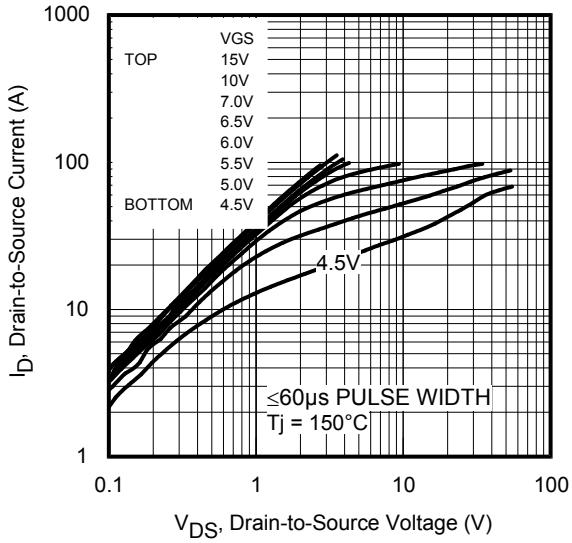


Fig 2. Typical Output Characteristics

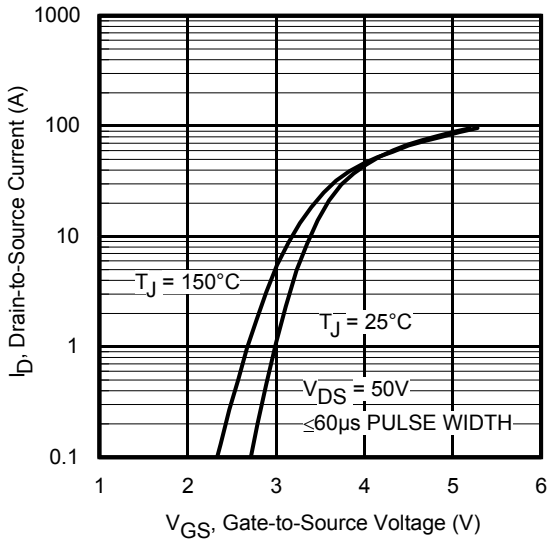


Fig 3. Typical Transfer Characteristics

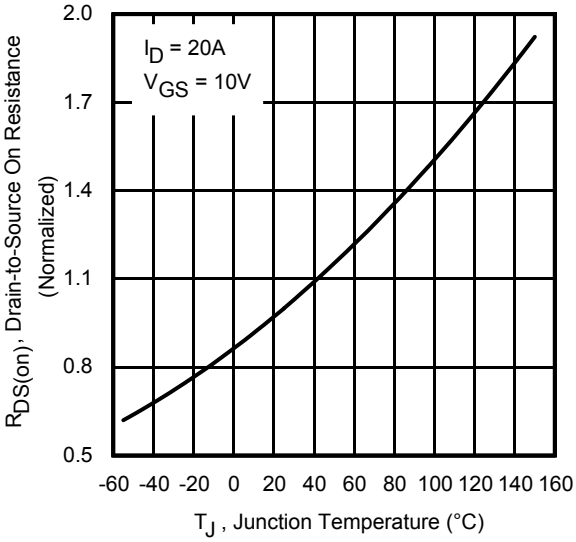


Fig 4. Normalized On-Resistance vs. Temperature

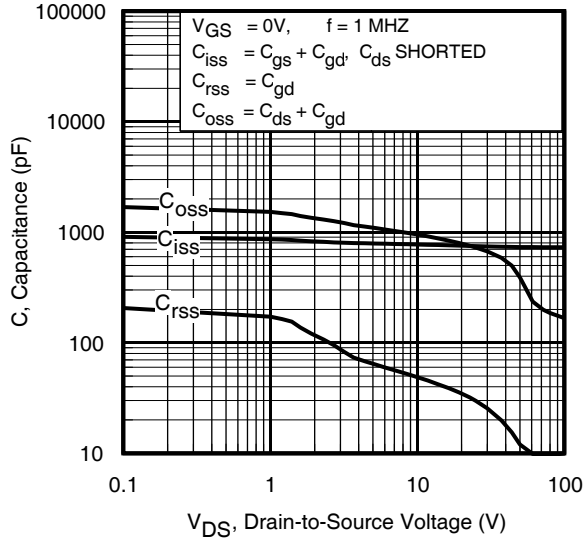


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

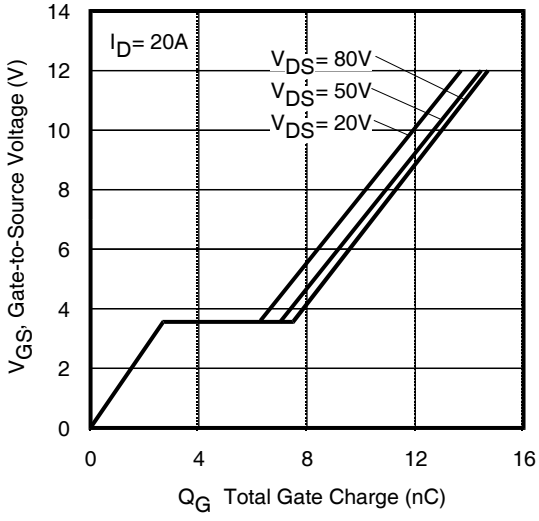


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

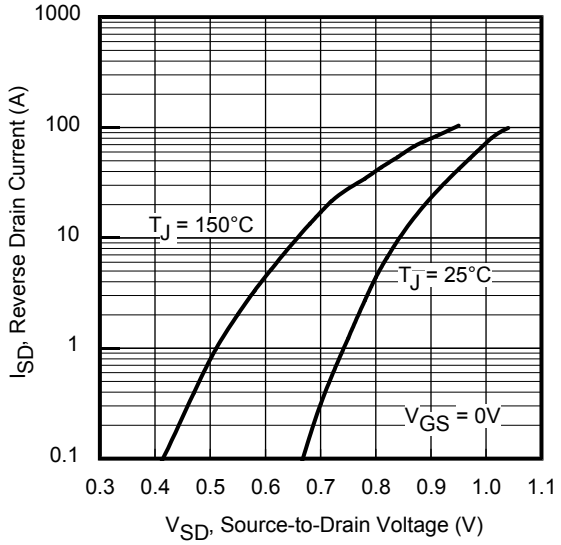


Fig 7. Typical Source-Drain Diode Forward Voltage

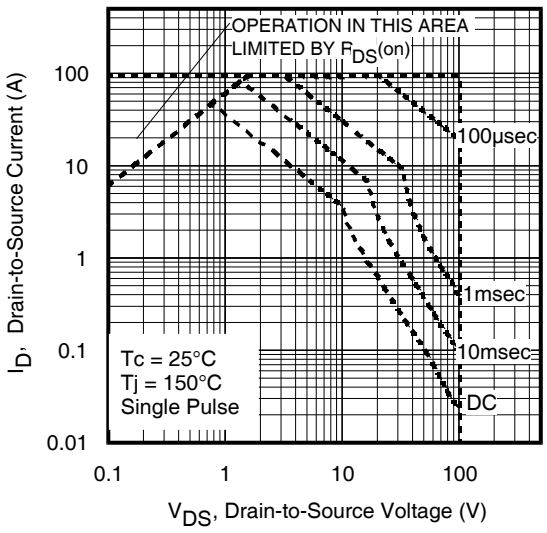


Fig 8. Maximum Safe Operating Area

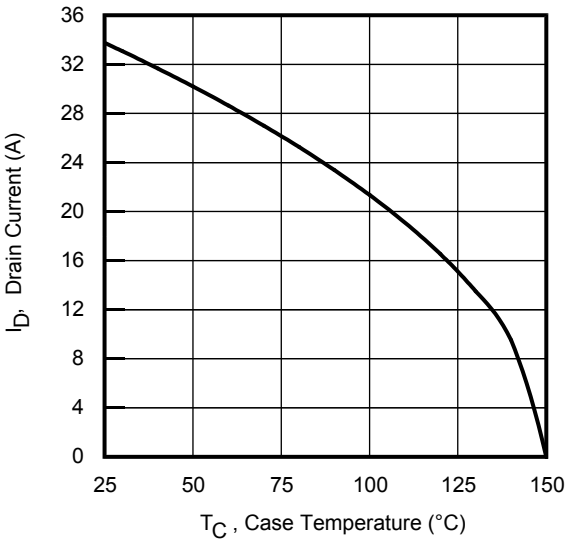


Fig 9. Maximum Drain Current vs. Case Temperature

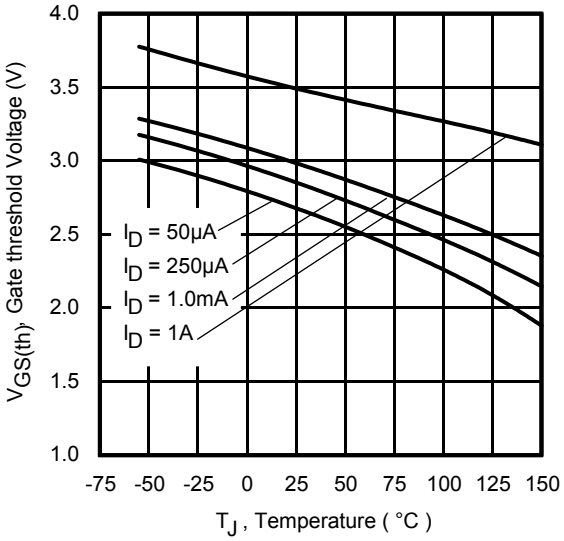


Fig 10. Threshold Voltage Vs. Temperature

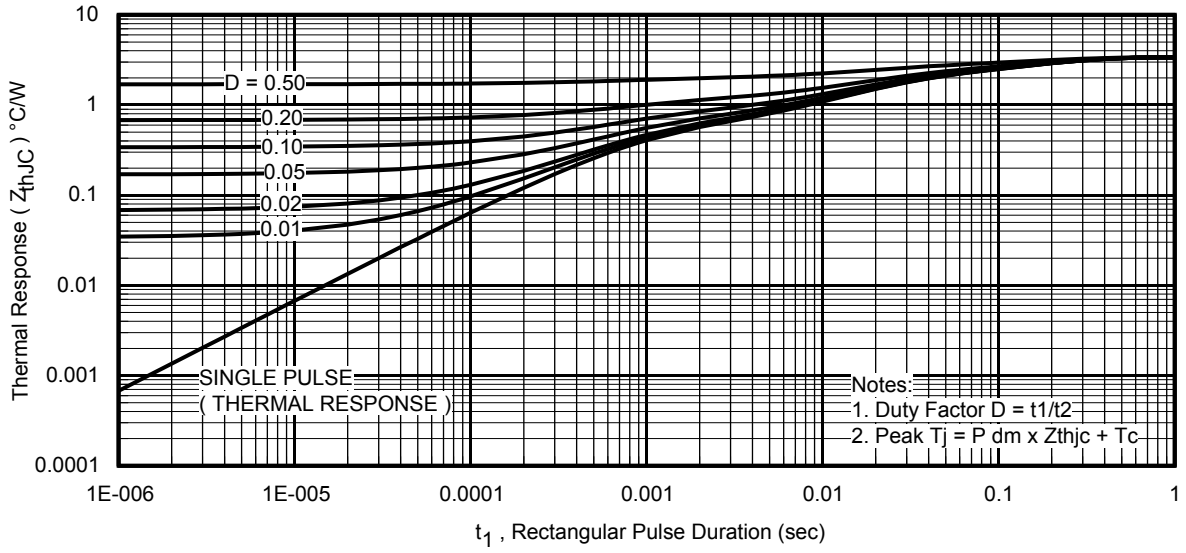


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

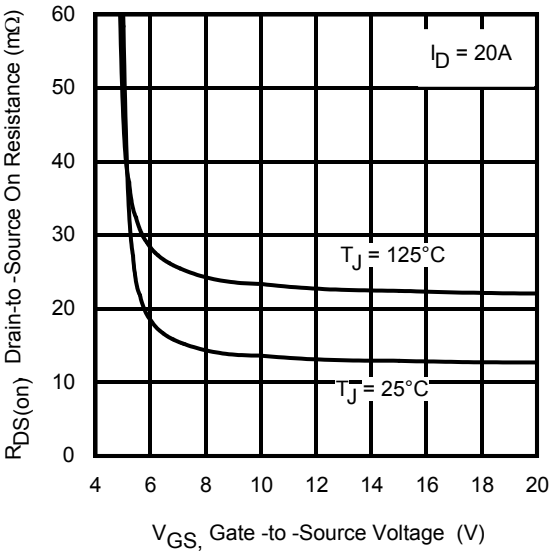


Fig 12. On– Resistance vs. Gate Voltage

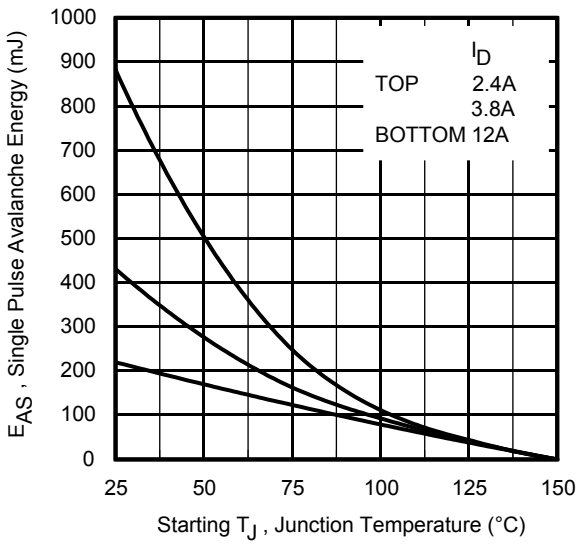


Fig 13. Maximum Avalanche Energy vs. Drain Current

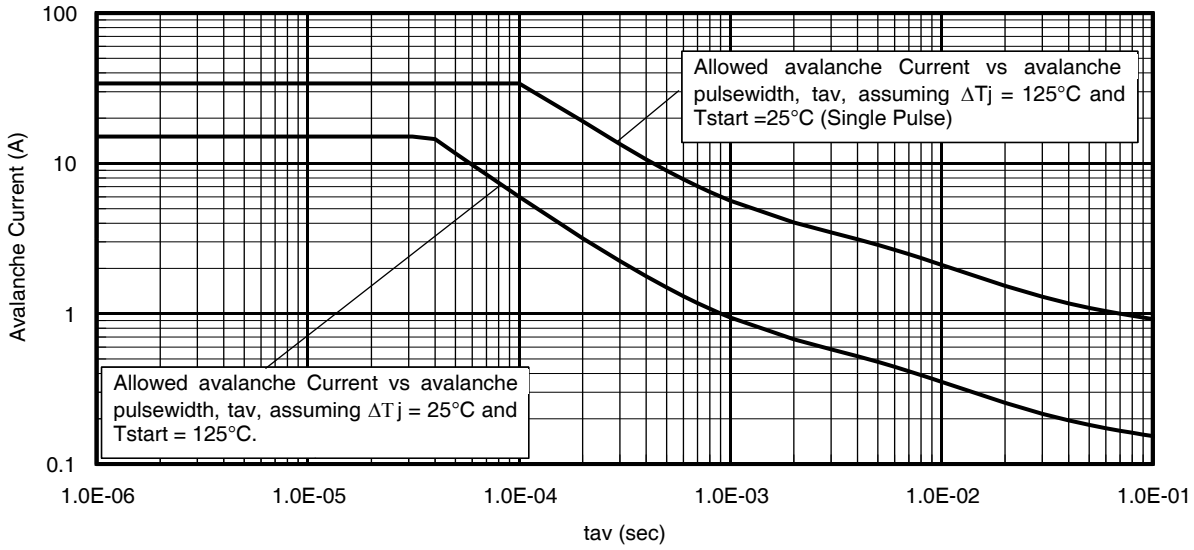


Fig 14. Single Avalanche Current vs. pulse Width

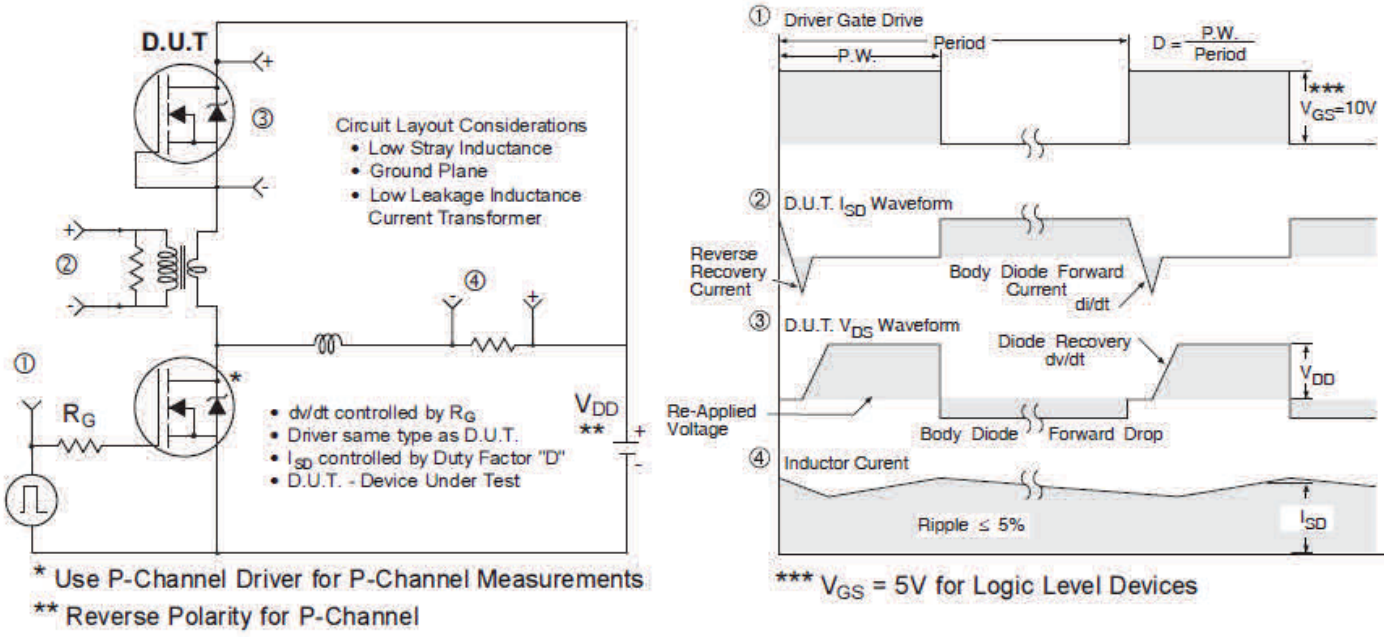


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

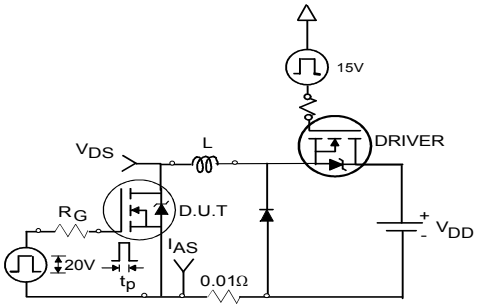


Fig 16a. Unclamped Inductive Test Circuit

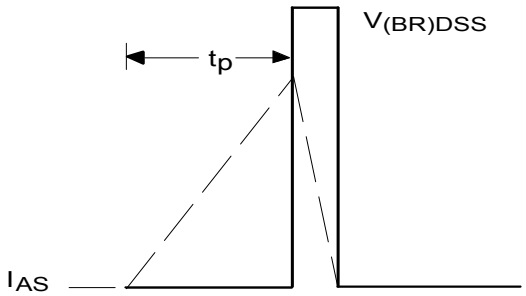


Fig 16b. Unclamped Inductive Waveforms

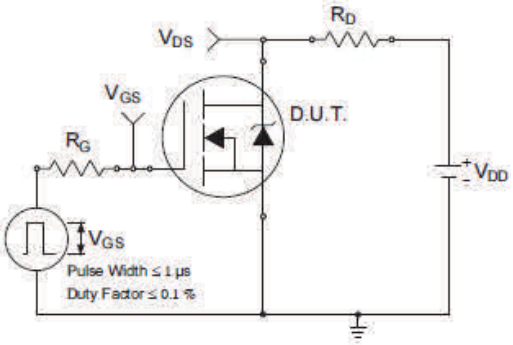


Fig 17a. Switching Time Test Circuit

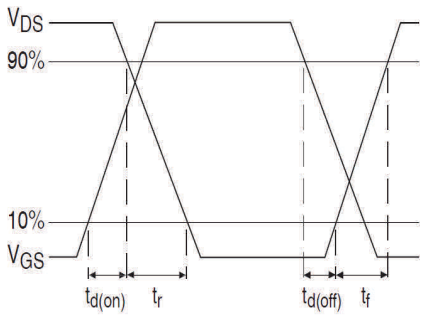


Fig 17b. Switching Time Waveforms

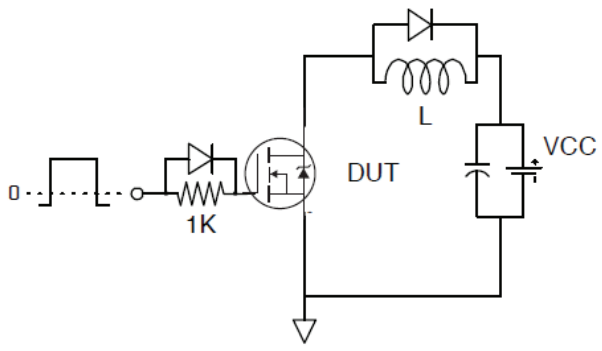


Fig 18. Gate Charge Test Circuit

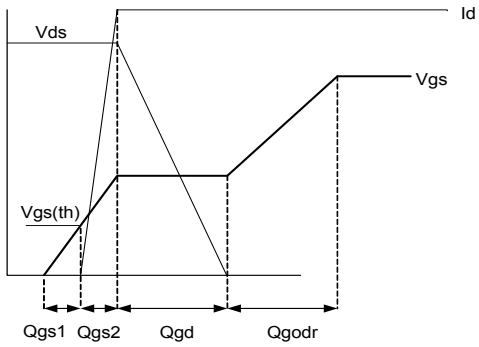
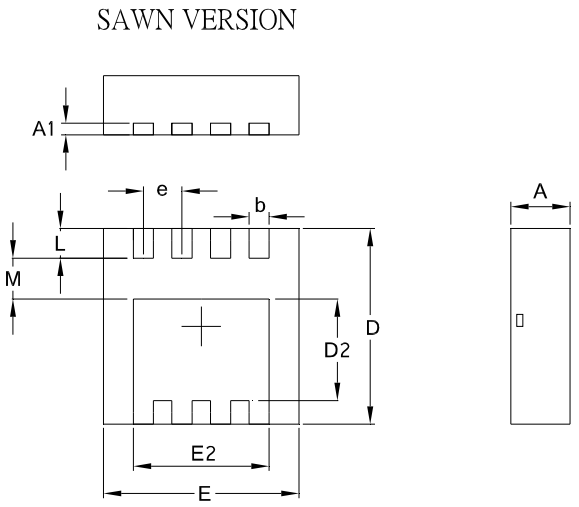


Fig 19. Gate Charge Waveform

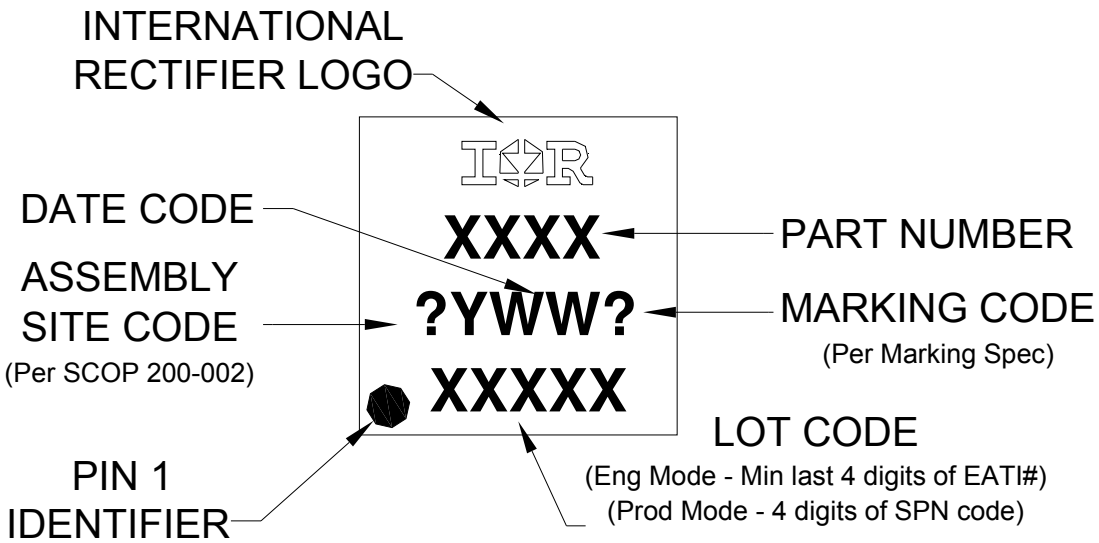
PQFN 3.3 x 3.3 Outline “B” Package Details



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.05	0.0276	0.0413
A1	0.12	0.39	0.0047	0.0154
b	0.25	0.39	0.0098	0.0154
D	3.20	3.45	0.1260	0.1358
D1	3.00	3.20	0.1181	0.1417
D2	1.69	2.20	0.0665	0.0866
E	3.20	3.40	0.1260	0.1339
E1	3.00	3.20	0.1181	0.1417
E2	2.15	2.59	0.0846	0.1020
e	0.65 BSC		0.0256 BSC	
L	0.15	0.55	0.0059	0.0217
M	0.59	—	0.0232	—
O	9Deg	12Deg	9Deg	12Deg

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

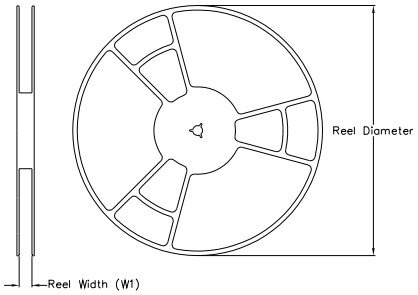
PQFN 3.3 x 3.3 Part Marking



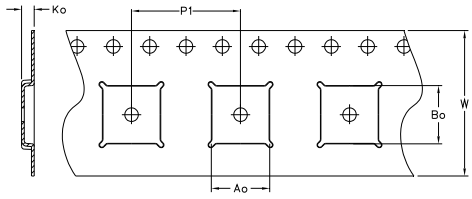
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

PQFN 3.3 x 3.3 Tape and Reel

REEL DIMENSIONS

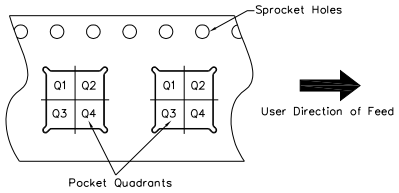


TAPE DIMENSIONS



CODE	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
Ao	3.50	3.70	.138	.146
Bo	3.50	3.70	.138	.146
Ko	1.10	1.30	.043	.051
P_1	7.90	8.10	.311	.319
W	11.80	12.20	.465	.480
W_1	12.30	12.50	.484	.492
Qty	4000			
Reel Diameter	13 Inches			

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 3mH, R_G = 50Ω, I_{AS} = 12A.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ R_θ is measured at TJ of approximately 90°C.

⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf

Revision History

Date	Comments
2/26/2016	• Updated datasheet with corporate template • Removed package outline "Punched Version" and updated with outline "Sawn Version" on page 7.

Published by
Infineon Technologies AG
81726 München, Germany

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