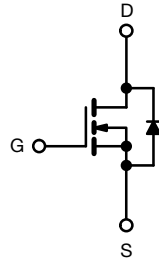


Power MOSFET



N-Channel MOSFET

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

Marking code: FA

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.20
Q_g max. (nC)	11
Q_{gs} (nC)	3.1
Q_{gd} (nC)	5.8
Configuration	Single

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHFL014TR-GE3 ^a
	IRFL014TRPbF-BE3 ^{a, b}
Lead (Pb)-free	IRFL014TRPbF ^a

Notes

- See device orientation
- “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	60	V	
Gate-source voltage		V_{GS}	± 20		
Continuous drain current	V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	2.7	A
			$T_C = 100\text{ }^\circ\text{C}$	1.7	
Pulsed drain current ^a		I_{DM}	22	W/ $^\circ\text{C}$	
Linear derating factor			0.025		
Linear derating factor (PCB mount) ^e			0.017		
Single pulse avalanche energy ^b		E_{AS}	100	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	3.1	W	
	$T_A = 25\text{ }^\circ\text{C}$		2.0		
Peak diode recovery dv/dt ^c		dV/dt	4.5	V/ns	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	For 10 s		300		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 16\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.7\text{ A}$ (see fig. 12)
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	60	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.068	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.6 A ^b	-	-	0.20	Ω
Forward transconductance	g _{fs}	V _{DS} = 25 V, I _D = 1.6 A		1.9	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	300	-	pF
Output capacitance	C _{oss}			-	160	-	
Reverse transfer capacitance	C _{rss}			-	29	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 10 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	11	nC
Gate-source charge	Q _{gs}			-	-	3.1	
Gate-drain charge	Q _{gd}			-	-	5.8	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, I _D = 10 A, R _g = 24 Ω, R _D = 2.7 Ω, see fig. 10 ^b		-	10	-	ns
Rise time	t _r			-	50	-	
Turn-off delay time	t _{d(off)}			-	13	-	
Fall time	t _f			-	19	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal source inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.7	A
Pulsed diode forward current ^a	I _{SM}			-	-	22	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 2.7 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 10 A, dI/dt = 100 A/μs ^b		-	70	140	ns
Body diode reverse recovery charge	Q _{rr}			-	0.20	0.40	
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

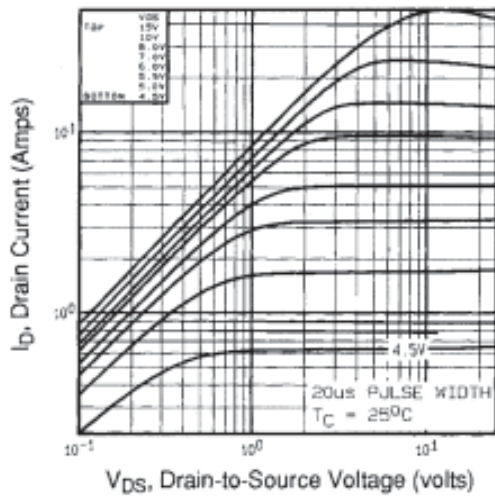


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

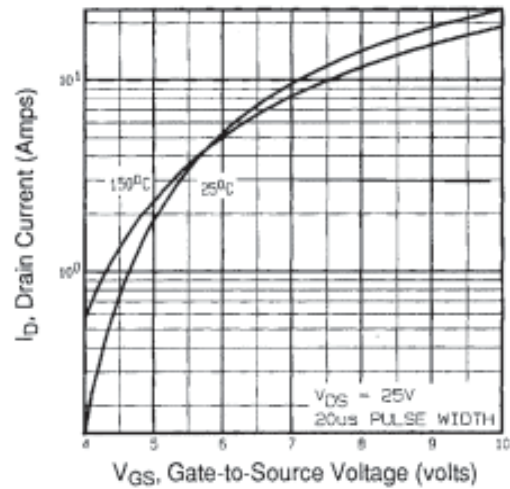


Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$



Fig. 4 - Normalized On-Resistance vs. Temperature

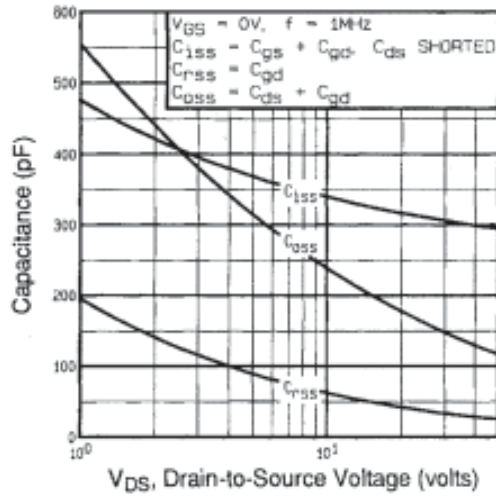


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

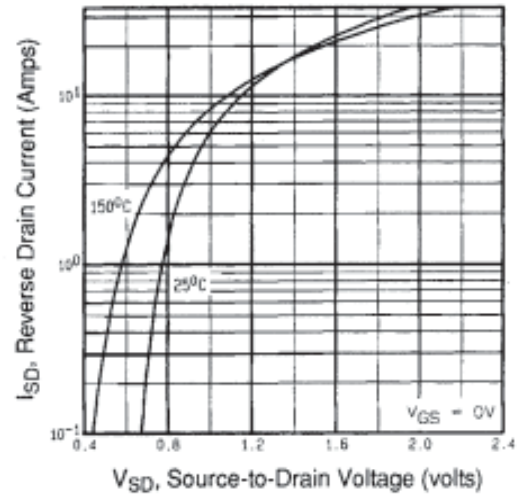


Fig. 7 - Typical Source-Drain Diode Forward Voltage

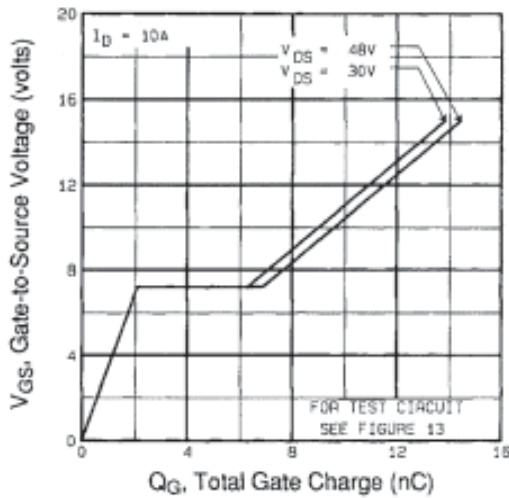


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

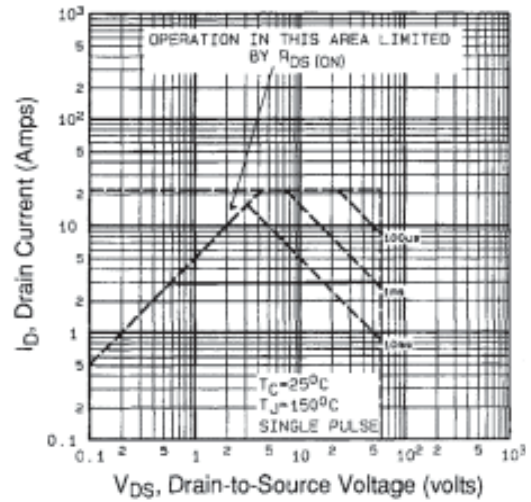


Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a -Switching Time Test Circuit



Fig. 10b -Switching Time Waveforms

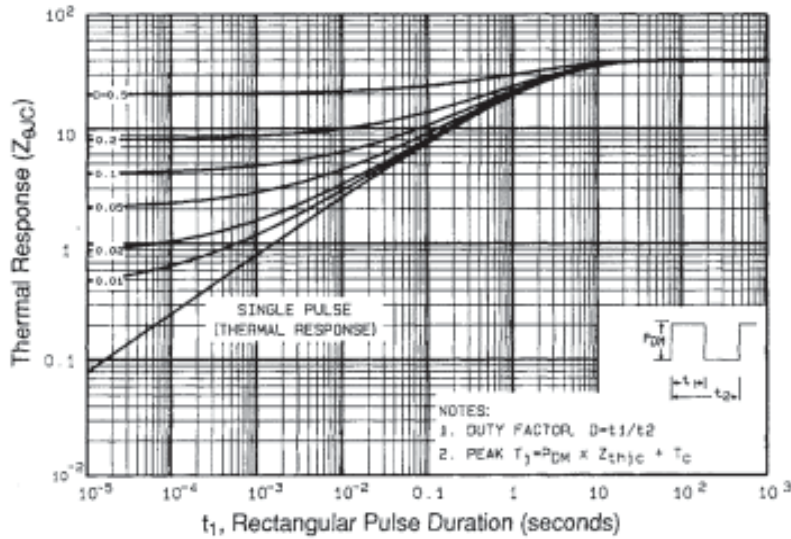


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

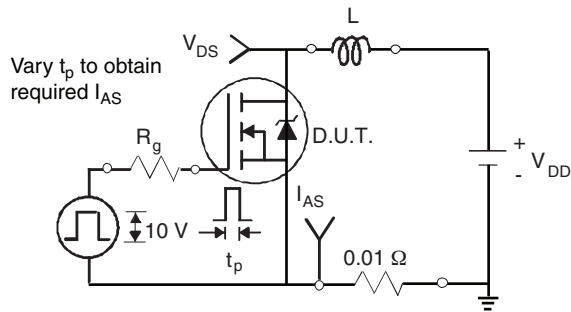


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

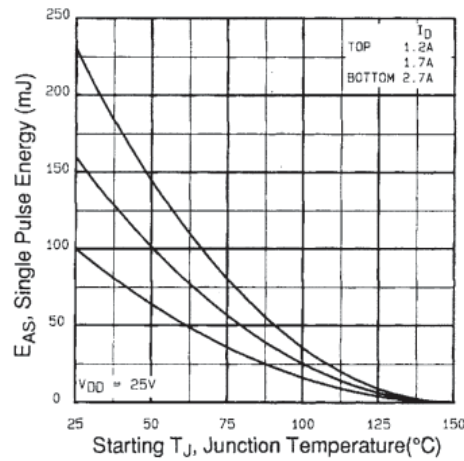


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

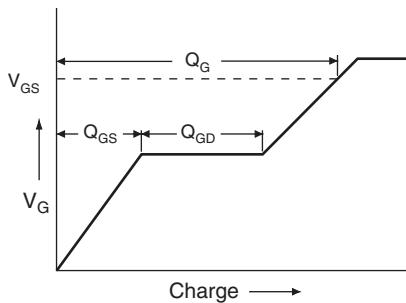


Fig. 13a - Basic Gate Charge Waveform

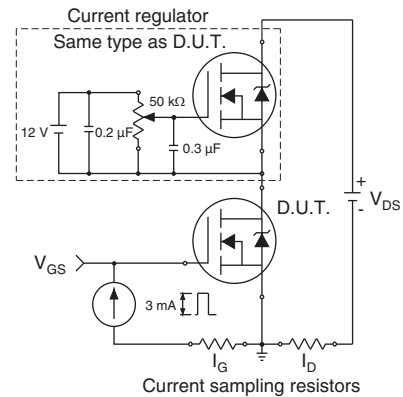
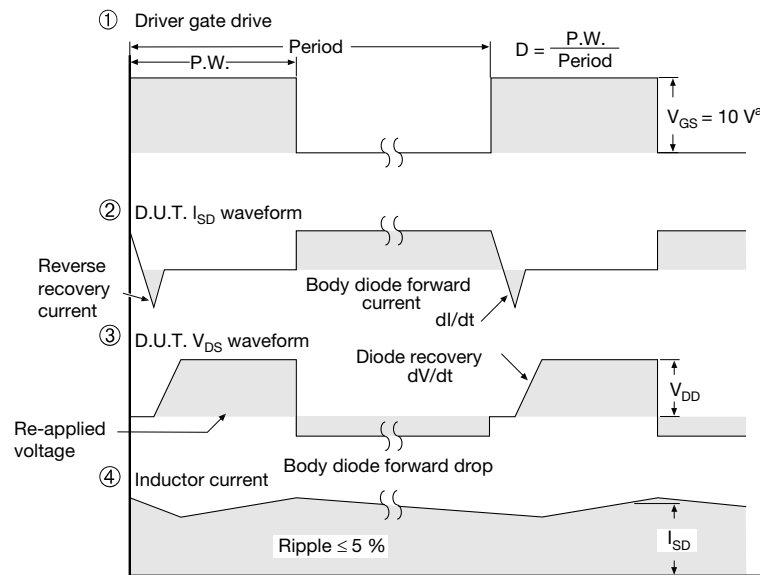
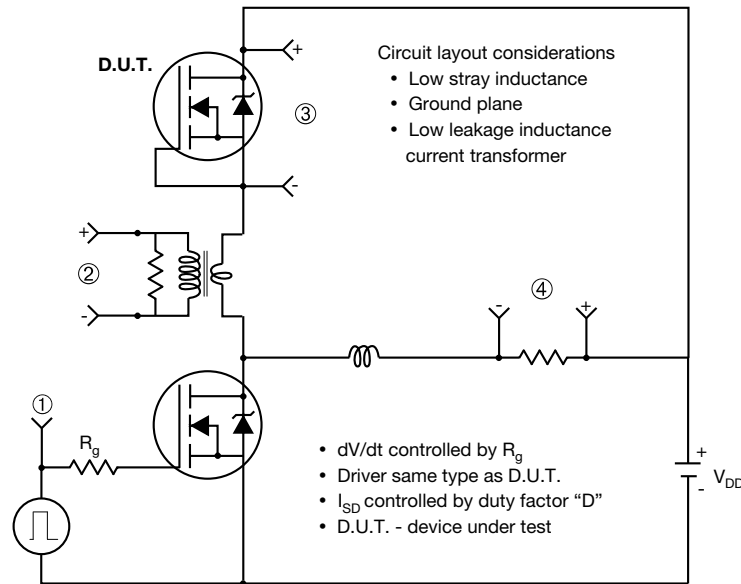


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 12 - For N-Channel

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SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08
DWG: 5969

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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