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# FSHDMI08 — Low-Voltage, Wide-Bandwidth, HDMI Switch with DDC and CEC Multiplexer

## Features

- -25db Non-Adjacent Channel Crosstalk at 1.65Gbps
- Low Signal Loss: -1.5dBg attenuation at 1.65Gbps
- Isolation Ground Between Channels
- Fast Turn-on/off Time (< 6ns)
- 1.65Gbps Throughput
- 8kV ESD Protection
- Low Skew: Intra-pair <90ps, Inter-pair < 150ps
- Low Power Consumption: 1µA Maximum

## Applications

- XGA and 720p DVI and HDMI Video Source Selection

## Description

The FSHDMI08 is a wide-bandwidth switch designed for routing HDMI link data, clock, and the relevant DDC and CEC control signals that support the data rate up to 1.65Gbps per channel for UXGA resolution. Applications include LCD TVs, DVD, set-top boxes, and notebook designs with multiple digital video interfaces.

This switch allows the passage of HDMI link signals with ultra-low non-adjacent channel crosstalk and ultra-low off isolation. This is critical to minimize ghost images between active video sources in video applications. The wide bandwidth of this switch allows the high-speed differential signal to pass through with minimal additive skew and phase jitter. The pinout supports an HDMI standard-A connector PCB layout.

### IMPORTANT NOTE:

For additional information, please contact [analogswitch@fairchildsemi.com](mailto:analogswitch@fairchildsemi.com).

## Ordering Information

Order Number	Eco Status	Package Description	Packing Method
FSHDMI08MTDX	RoHS	56-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide	Tape and Reel

For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

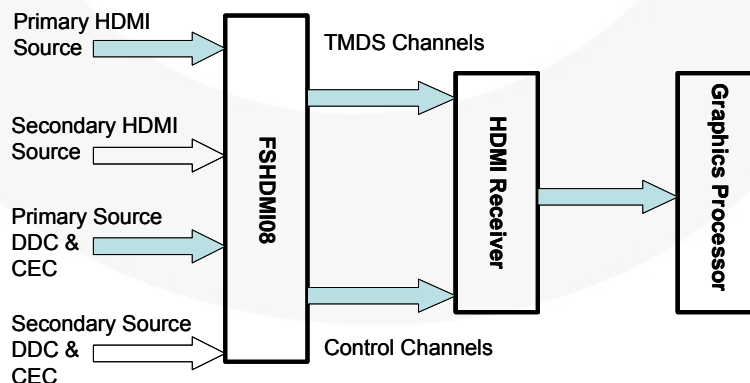


Figure 1. Single-Link HDMI Application

## Functional Diagram

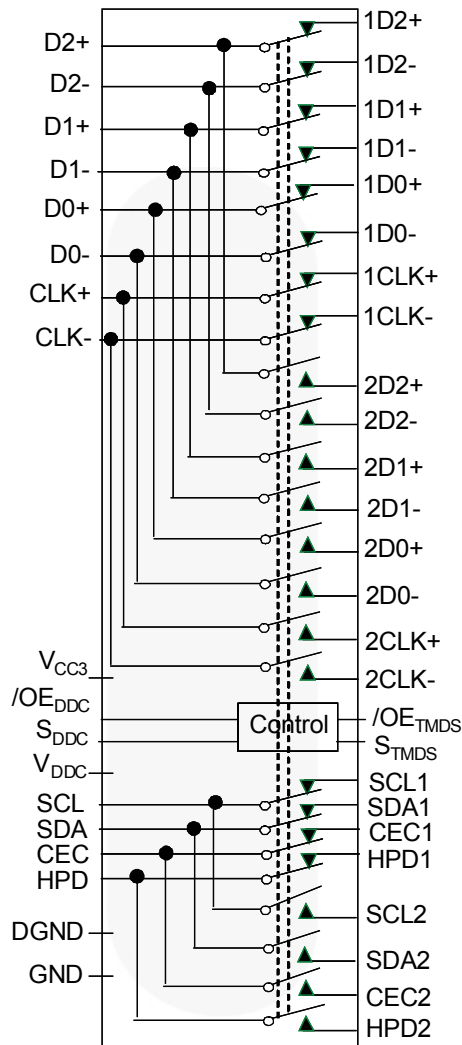


Figure 2. Functional Diagram

## Pin Descriptions

Pin	Name	Description
1-4,6,7,11-14,16,17,47,48,50,51,53,54	1Dn+, 1Dn-, 2Dn+, 2Dn-, Dn+, Dn-	TMDS Data Channels
8,9,18,19,44,45	1CLK+, 1CLK-, 2CLK+, 2CLK-, CLK+, CLK-	TMDS Clock Channels
24,28,33	HPD1, HPD2, HPD	Hot Plug Detects
22,26,35	SCL1, SCL2, SCL	Serial Clock (DDC)
23,27,34	SDA1, SDA2, SDA	Serial Data (DDC)
21,25,36	CEC1, CEC2, CEC	Consumer Electronics Control (CEC)
29	V <sub>DDC</sub>	DDC Power
20,39,40,55,56	V <sub>CC3</sub>	TMDS Power
30	DGND	DDC/CEC GND
5,10,15,38,43,46,49,52	GND	GND
32,42	S <sub>TMDMS</sub> , S <sub>DDC</sub>	Select Pins (TMDS, DDC)
31,41	/OE <sub>TMDMS</sub> , /OE <sub>DDC</sub>	Output Enable (TMDS, DDC)

## Pin Assignments

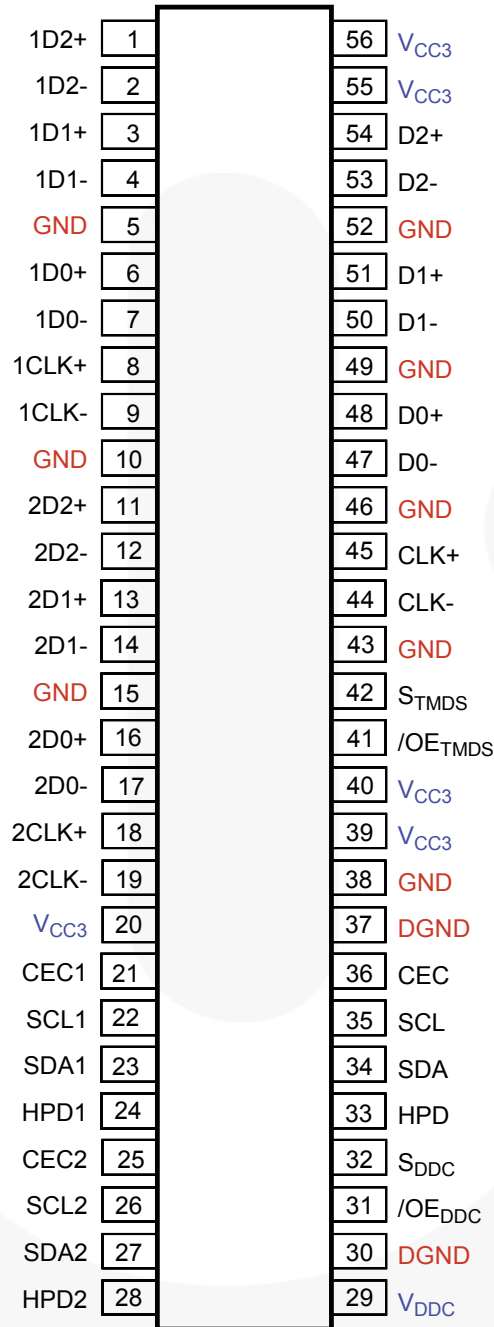


Figure 3. Pin Assignments

## Truth Table

$S_{TMDS}$ , $S_{DDC}$	$/OE_{TMDS}$ , $/OE_{DDC}$	Function
Don't Care	Logic Level HIGH	All Ports Disconnected (Hi-Z)
Logic Level LOW	Logic Level LOW	1Dn+/1Dn-=Dn+/Dn-; 1CLK+/ 1CLK-=CLK+/CLK-; HPD1=HPD; SCL1=SCL; SDA1=SDA; CEC1=CEC
Logic Level HIGH	Logic Level LOW	2Dn+/2Dn-=Dn+/Dn-; 2CLK+/ 2CLK-=CLK+/CLK-; HPD2=HPD; SCL2=SCL; SDA2=SDA; CEC2=CEC

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
$V_{CC3}$	Supply Voltage – TMD5 Channels		-0.5	4.6	V
$V_{DDC}$	Supply Voltage – 5V DDC		-0.5	6.0	V
$V_{SWTMD5}^{(1)}$	Switch I/O Voltage	1Dn+, 1Dn-, 2Dn+, 2Dn-, Dn+, Dn-, 1CLK+, 1CLK-, 2CLK+, 2CLK-, CLK+, CLK-	-0.5	$V_{CC3} + 0.3$	V
$V_{SWDDC}^{(1)}$	Switch I/O Voltage	HPD1, HPD2, HPD, SCL1, SCL2, SCL, SDA1, SDA2, SDA, CEC1, CEC2, CEC	-0.5	$V_{DDC} + 0.3$	V
$V_{CNTRLT}^{(1)}$	Control Input Voltage	$S_{TMD5}$ , $/OE_{TMD5}$	-0.5	4.6	V
$V_{CNTRLD}^{(1)}$	Control Input Voltage	$S_{DDC}$ , $/OE_{DDC}$	-0.5	6.0	V
$I_{IK}$	Input Clamp Diode Current			-50	mA
$I_{SW}$	Switch I/O Current (Continuous)			128	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$T_J$	Maximum Junction Temperature			+150	°C
$T_L$	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)		I/O to GND	8.0	kV
			All Other Pins	2.5	
	Charged Device Model (JEDEC: JESD22-C101)			2.0	

### Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC3}$	TMD5 Supply Voltage – 3V	3.0	4.3	V
$V_{DDC}$	DDC Supply Voltage	3.0	5.5	V
$V_{CNTRLT}$	Control Input Voltage – $S_{TMD5}$ , $/OE_{TMD5}$	0	$V_{CC3}$	V
$V_{CNTRLD}$	Control Input Voltage – $S_{DDC}$ , $/OE_{DDC}$	0	$V_{DDC}$	V
$V_{SWTMD5}$	Switch I/O Voltage for HDMI path	$V_{CC3} - 0.6$	$V_{CC3}$	V
$V_{SWDDC}$	Switch I/O Voltage for DDC path	0	$V_{DDC}$	V
$T_A$	Operating Temperature	-40	+85	°C
$\theta_{JA}$	Thermal Resistance (Free Air)		+80	°C/W

## DC Electrical Characteristics

All typical values are for  $V_{CC3}=3.3V$  and  $V_{DDC}=5.0V$  at  $25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	$V_{CC3} / V_{DDC} (V)$	Conditions	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$V_{CC3}=3.0$ $V_{DDC}=5.0$	$I_{IN}=-18mA$			-1.2	V
$V_{IH}$	Control Input Voltage High	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=3.0$ to $5.5$		2			V
$V_{IL}$	Control Input Voltage Low	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=3.0$ to $5.5$				0.8	V
$I_{OZTMDS}$	Off State Leakage TMD5 Channels	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$0 \leq V_{SWTMDS} \leq V_{CC3}$ Figure 5	-1		1	$\mu A$
$I_{OZDDC}$	Off State Leakage DDC/CEC Channels	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$0 \leq V_{SWDDC} \leq V_{DDC}$ Figure 5	-5		5	$\mu A$
$I_{INTMDS}$	Control Input Leakage ( $S_{TMDS}$ , $/OE_{TMDS}$ )	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$V_{SWDDC}=0$ to $V_{CC3}$	-1		1	$\mu A$
$I_{INDDC}$	Control Input Leakage ( $S_{DDC}$ , $/OE_{DDC}$ )	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$V_{SWDDC}=0$ to $V_{DDC}$	-1		1	$\mu A$
$I_{CC3}$	Quiescent Supply Current -TMD5	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$V_{SWTMDS}=V_{CC3}-0.6$ or $V_{CC3}$ , $I_{OUT}=0$			2	$\mu A$
$I_{DDC}$	Quiescent Supply Current -DDC	$V_{CC3}=3.6$ $V_{DDC}=5.5$	$V_{SWDDC}=0$ or $V_{DDC}$ , $I_{OUT}=0$			2	$\mu A$
$\Delta I_{CCT3}$	Increase in $I_{CC3}$	$V_{CC3}=3.6$ $V_{CC5}=5.5$	One input at $3.0V$ ; Other inputs at $V_{CC3}-0.6$ or $V_{CC3}$			100	$\mu A$
$\Delta I_{CCTD}$	Increase in $I_{DDC}$	$V_{CC3}=3.6$ $V_{CC5}=5.5$	One input at $3.0V$ ; Other inputs at $V_{DDC}$			15	$\mu A$

## AC Electrical Characteristics

All typical values are for  $V_{CC3}=3.3V$  and  $V_{DDC}=5.0V$  at  $25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	$V_{CC3}/V_{DDC}$ (V)	Conditions	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
<b>TMDS Channels</b>							
$t_{ONTMDS}$	Turn-On Time S, /OE to Output	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$V_{SWTMDS}=V_{CC3}-0.5$ , $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 6, Figure 7		4	6	ns
$t_{OFFTMDS}$	Turn-Off Time S to Output	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$V_{SWTMDS}=V_{CC3}-0.5$ , $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 6, Figure 7		2	4	
$t_{BBM-TMDS}$	Break-Before-Make Time <sup>(2)</sup>	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$V_{SWTMDS}=V_{CC3}-0.5$ , $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 15	1			ns
$t_{pd}$ ( $t_{pLH}$ , $t_{pHL}$ )	Switch Propagation Delay <sup>(2)</sup>	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$R_{PU}=50\Omega$ , $C_L=5pf$ Figure 14			400	ps
$t_{jitter}$	Total Jitter (DJ+RJ)	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$f=165MHz$ clock with 50% duty cycle, $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 14			90	ps
$t_{ratio}$	Duty Cycle Ratio	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$f=165MHz$ clock with 50% duty cycle, $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 14	40	50	60	%
$t_{SK1}$	Intra-Pair Skew (TMDS Cn+ to Cn-)	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$f=1.65Gbps$ , $2^{23}-1$ PRBS, $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 14		55	100	ps
$t_{SK2}$	Inter-Pair Skew (Between any two TMDS switch pair paths)	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$f=1.65Gbps$ , $2^{23}-1$ PRBS, $R_{PU}=50\Omega$ , $C_L=5pf$ Figure 14		90	160	ps
$OIRR_{TMDS}$	Off-Isolation (TMDS Channels)	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$R_T=50\Omega$ , $f=370MHz$ Figure 10	-30			dB
		$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$R_T=50\Omega$ , $f=825MHz$ Figure 10	-25			
$Xtalk_{TMDS}$	Non-Adjacent Channel Crosstalk (TMDS Channels)	$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$R_T=50\Omega$ , $f=370MHz$ Figure 11	-25			dB
		$V_{CC3}=3.0$ to $3.6$ $V_{DDC}=5.0$	$R_T=50\Omega$ , $f=825MHz$ Figure 11	-20			
$f_{max}$	Maximum Throughput <sup>(2)</sup>	$V_{CC3}=3.3$ $V_{DDC}=5.0$			1.65		Gbps
<b>Control Channels – DDC / CEC</b>							
$t_{ONDDC}$	Turn-On Time; $S_{DDC}$ , /OE <sub>DDC</sub> to Output	$V_{CC3}=3.3$ $V_{DDC}=3.0$ to $5.5$	$V_{SWDDC}=2V$ , $R_{DDC}=1k\Omega$ , $C_L=5pf$			28	ns
$t_{OFFDDC}$	Turn-Off Time; $S_{DDC}$ , /OE <sub>DDC</sub> to Output	$V_{CC3}=3.3$ $V_{DDC}=3.0$ to $5.5$	$V_{SWDDC}=2V$ , $R_L=1k\Omega$ , $C_L=5pf$			24	ns

**Note:**

- Guaranteed by characterization, not production tested.

Test Diagrams

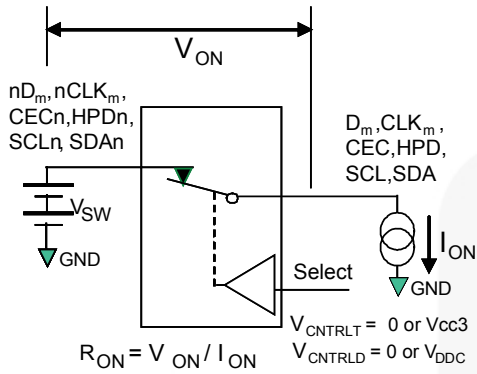
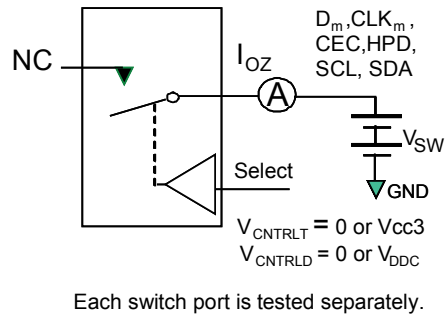
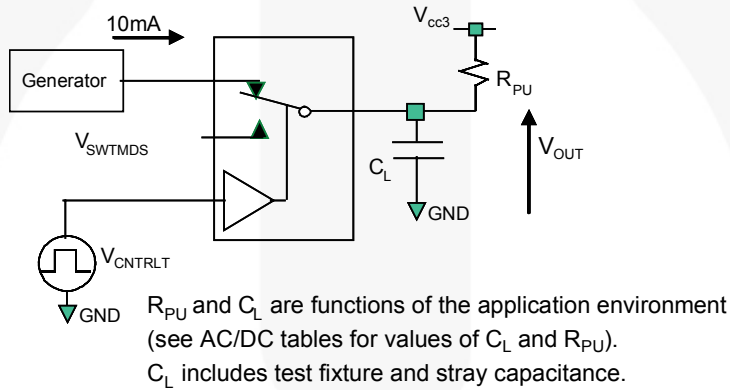


Figure 4. On Resistance



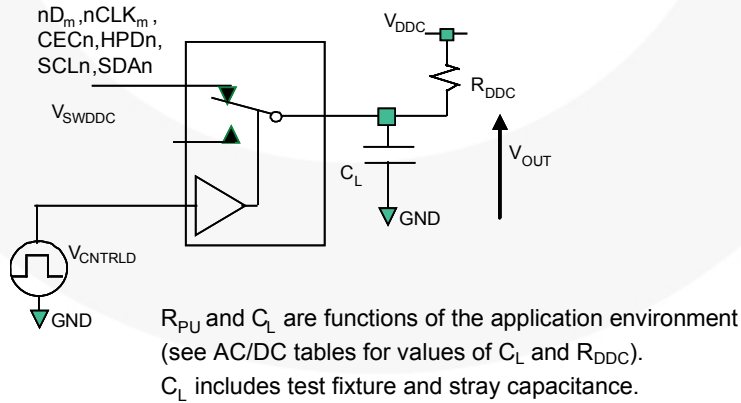
Each switch port is tested separately.

Figure 5. Off Leakage



$R_{PU}$  and  $C_L$  are functions of the application environment (see AC/DC tables for values of  $C_L$  and  $R_{PU}$ ).  $C_L$  includes test fixture and stray capacitance.

Figure 6. TMSD Test Circuit Load

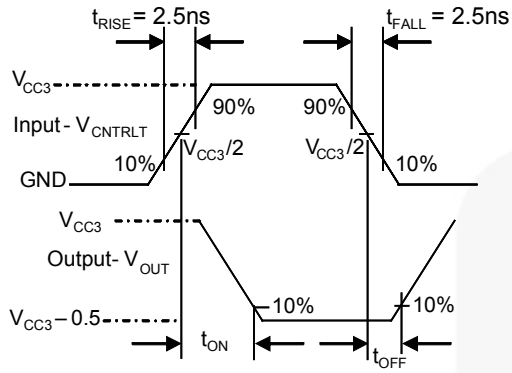


$R_{PU}$  and  $C_L$  are functions of the application environment (see AC/DC tables for values of  $C_L$  and  $R_{DDC}$ ).  $C_L$  includes test fixture and stray capacitance.

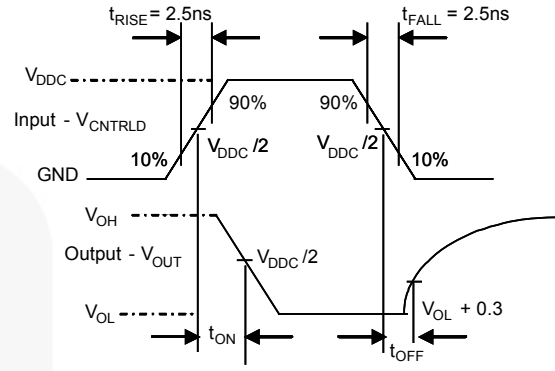
Figure 7. DDC Test Circuit Load



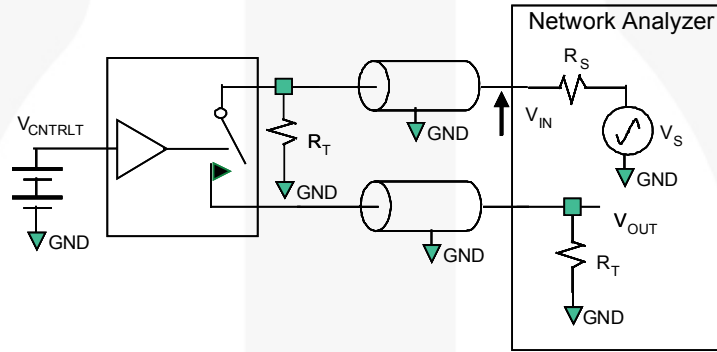
### Test Diagrams



**Figure 8. Turn-on / Turn-off Waveforms**

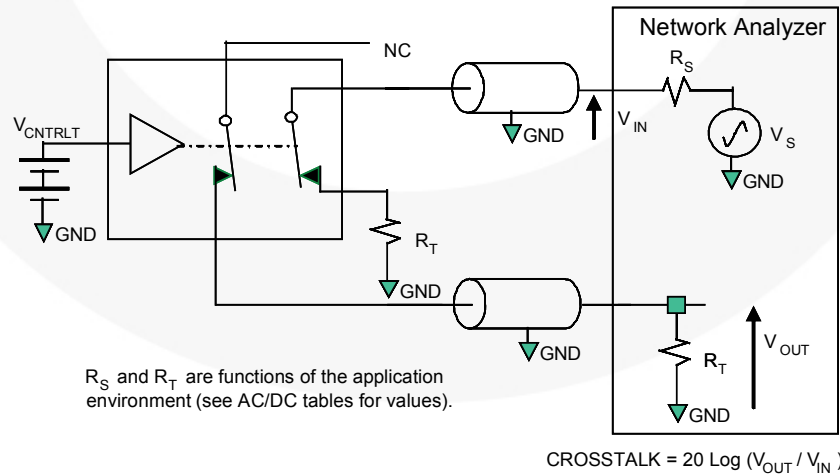


**Figure 9. DDC Turn-on / Turn-off Waveforms**



$$\text{Off Isolation} = 20 \text{ Log} (V_{\text{OUT}} / V_{\text{IN}})$$

**Figure 10. Channel Off Isolation**



$$\text{CROSSTALK} = 20 \text{ Log} (V_{\text{OUT}} / V_{\text{IN}})$$

**Figure 11. Non-Adjacent Channel-to-Channel Crosstalk**

## Test Diagrams

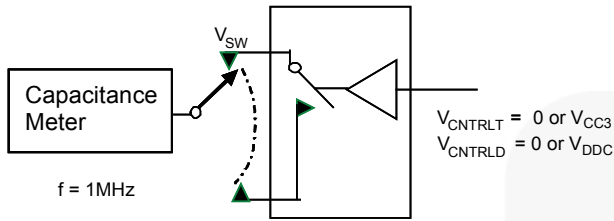


Figure 12. Channel Off Capacitance

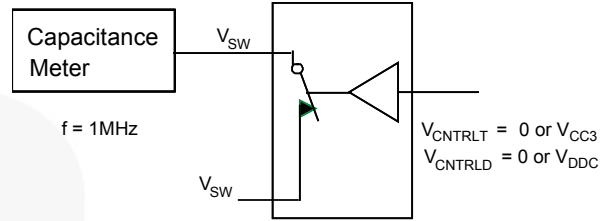


Figure 13. Channel On Capacitance

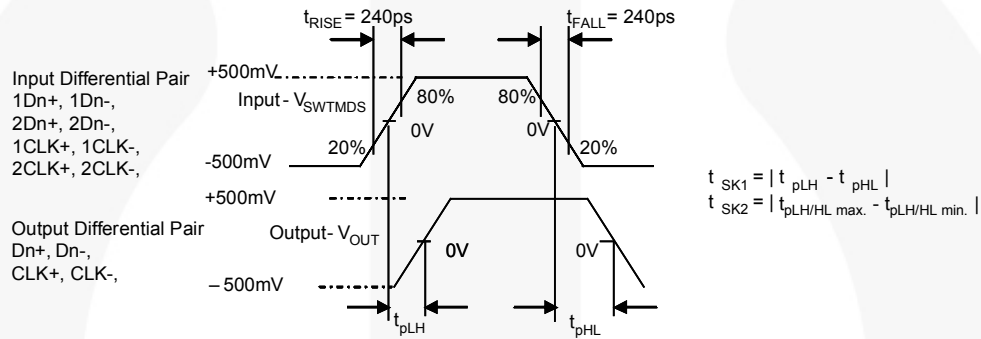


Figure 14. Intra- and Inter-Pair Skew  $t_{pd}$

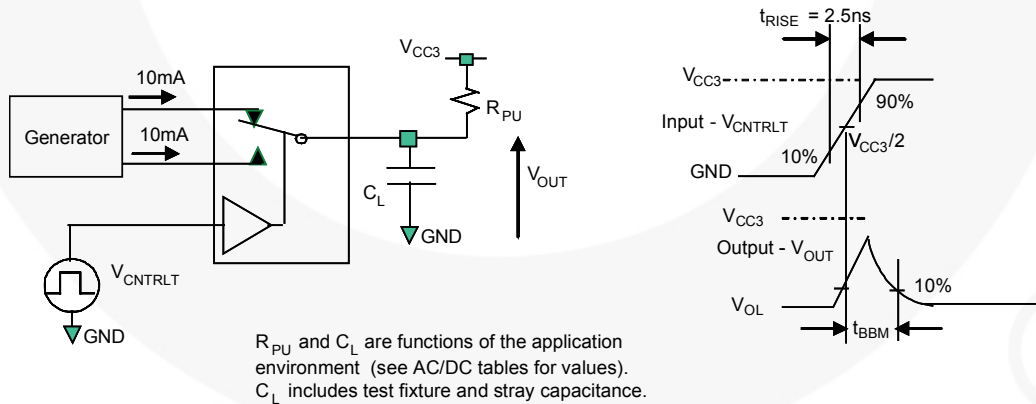
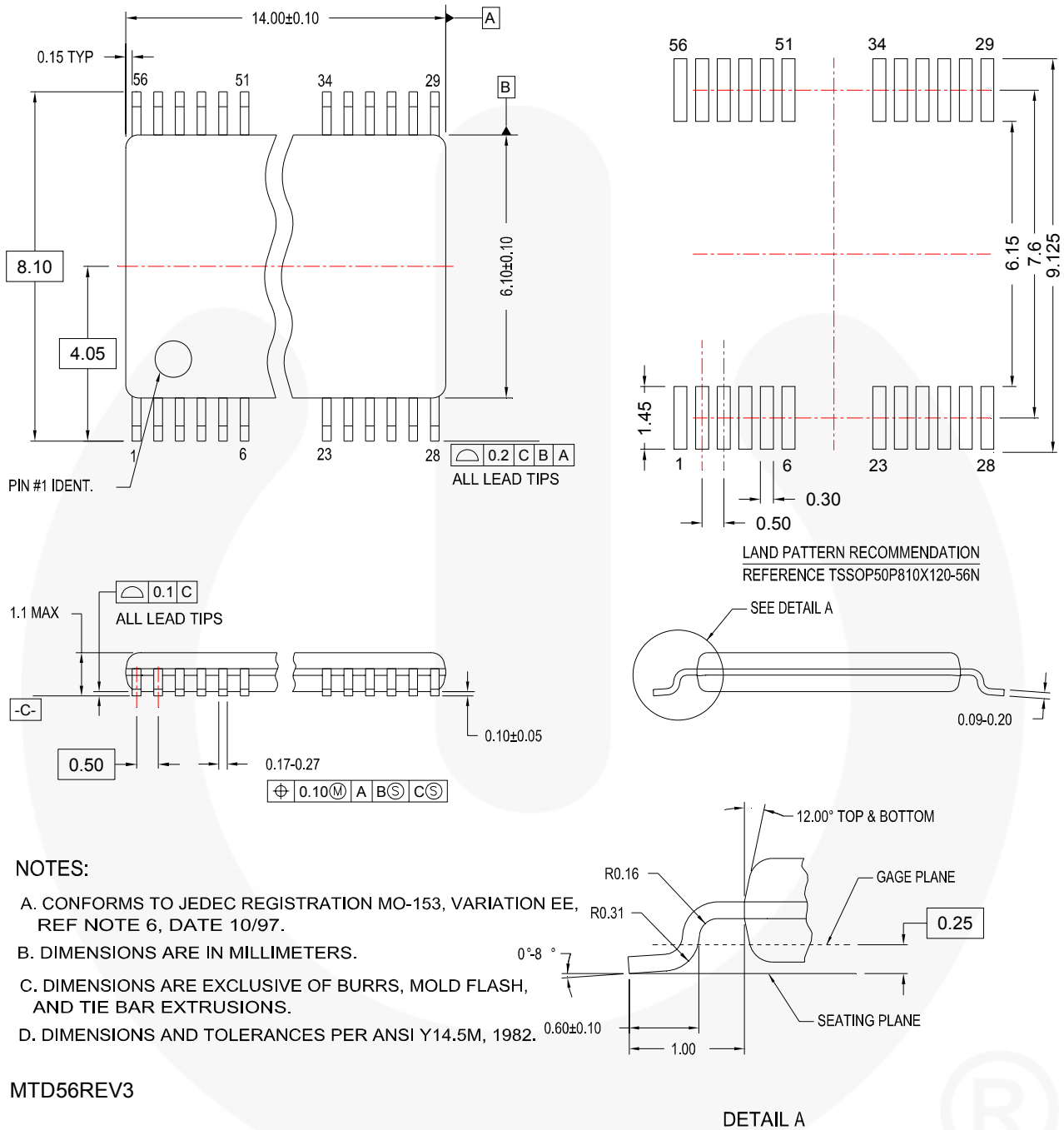


Figure 15. Break Before Make

## Physical Dimensions



**Figure 16. 56-Pin Thin-Shrink Small Outline Package (TSSOP)**

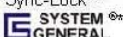
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**Definition of Terms**

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Rev. I42

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