Application Note ANI19

Selecting Charge Pump Capacitors for Serial RS-232 Transceivers

Scope

Modern serial communication systems often must operate at low voltages, using low power while adhering to legacy specification standards. The RS-232 standard in particular requires on-board charge pump regulators to generate the specified V_{OH} and V_{OL} levels. All industry RS-232 transceivers have capacitor values defined in their datasheets, but there are times when a system designer will need to alter the capacitor values based on some constraint, such as board space or cost for example. This article demonstrates a method for choosing charge pump capacitor values for V.28 and V.11 transceivers.

Background

RS-232 transceivers with on-chip charge pumps can be thought of as having two separate circuit functions. The charge pump circuit provides the proper V+ and V- bias rails for the transceiver circuits. The V+ (V_{DD}) voltage is higher than the supply voltage and the V- (V_{SS}) is a negative voltage, so the transceivers can swing symmetrically around Ground as required in the RS-232 specification. The load current (I_{OUT}) for the charge pump consists of the drivers, receivers and logic circuitry of the transceiver block. The load current ranges from the quiescent current level when no loads signals are present on the transceivers to a maximum current level when all transceivers are fully loaded with signals present.

All of Sipex's RS-232 and multi-protocol transceivers utilize four charge pump capacitors. Two of the capacitors are "flying caps" (C1 and C2), and are used to double, invert, and transfer the input voltage (V_{CC}) or charge while two more caps (C3 and C4) are used to store the charge at the outputs (V_{DD} and V_{SS}). This is required to generate the positive (V+) and negative (V-) voltages required by the RS-232 standard.

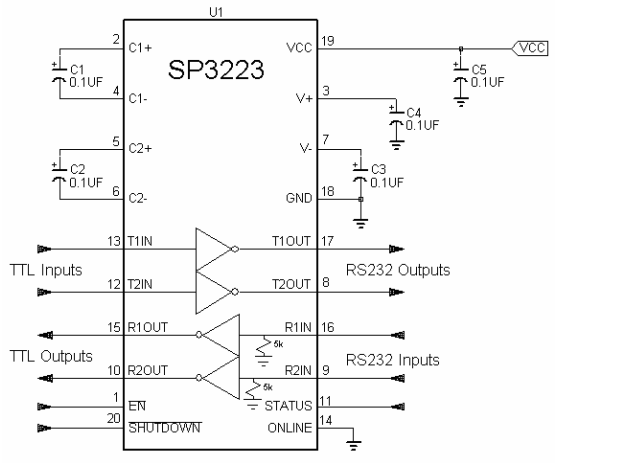


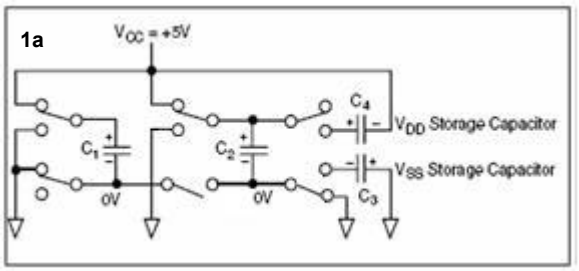
Figure 1 – Typical RS-232 Application

 © 2006 Sipex Corporation

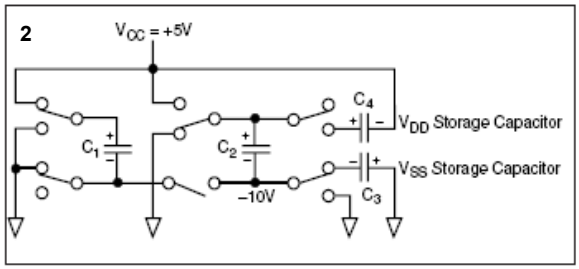
Charge Pump Theory

The charge pump on all Sipex interface products is a patented design (U.S. Patent 5,306,954) and uses a unique approach compared to older, less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical power supplies. The charge pump V_{DD} and V_{SS} outputs are regulated. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

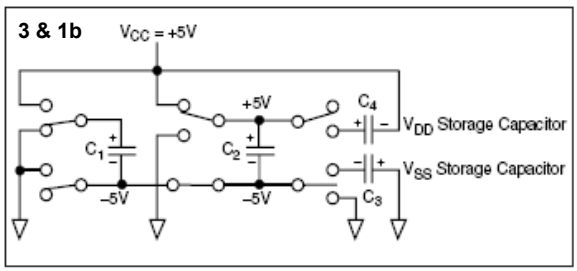
Phase 1 - V_{SS} Charge Storage
During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to V_{CC} (**1a**). C1+ is then switched to Ground and the charge in C1- is transferred to C2-. C2+ is connected to V_{CC}, the voltage potential across capacitor C2 is now 2xV_{CC} (**1b**).



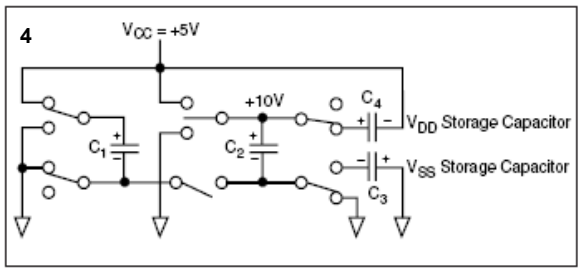
Phase 2 - V_{SS} Transfer
Phase two of the clock connects the negative terminal of C2 to the V_{SS} storage capacitor and the positive terminal of C2 to Ground, and transfers the negative generated voltage to C3. This generated voltage is regulated to V- or V_{SS}. Simultaneously, the positive side of the capacitor C1 is switched to V_{CC} and the negative side is connected to Ground.



Phase 3 – V_{DD} Charge Storage
The third phase of the clock is identical to the first phase: the charge transferred in C1 produces -V_{CC} in the negative terminal of C1 which is applied to the negative side of the capacitor C2. Since C2+ is at V_{CC}, the voltage potential across C2 is 2xV_{CC}.



Phase 4 - V_{DD} Transfer
The fourth phase of the clock connects the negative terminal of C2 to Ground, and transfers the generated V+ or V_{DD} across C2 to C4, the V_{DD} storage capacitor. This voltage is regulated. At the regulated voltage, the internal oscillator is disabled and simultaneously with this, the positive side of capacitor C1 is switched to V_{CC} and the negative side is connected to Ground, and the cycle begins again.



Early RS-232 devices had basic voltage doublers/inverters while later devices have regulated charge pump outputs. The unregulated charge pumps provide the bias rails for the transceiver block; V_{DD} = V_{CC}+V_{CC} = 2V_{CC} and V_{SS} = -V_{CC}-V_{CC} = -2V_{CC}. The regulated charge pumps offer a stable V_{DD} and V_{SS} voltage over a wide V_{CC} input range and load variations, which transceivers do present to the bias. Even though the V_{DD} and V_{SS} have lower initial voltages, the voltage is constant as V_{CC} changes. This translates to consistent and more reliable drive levels on a communication bus.

 © 2006 Sipex Corporation

Regulated Charge Pump Waveforms – SP3223, V_{CC}=3V, T_A=27°C, TX Loop Back to RX Switching

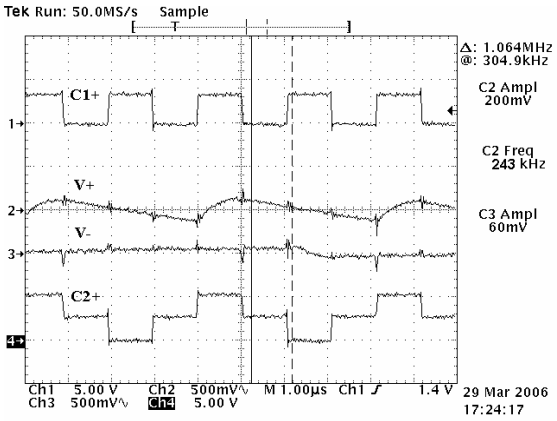


Figure 2 – V_{DD} and V_{SS} Terminal Ripple and Fly Capacitor Positive

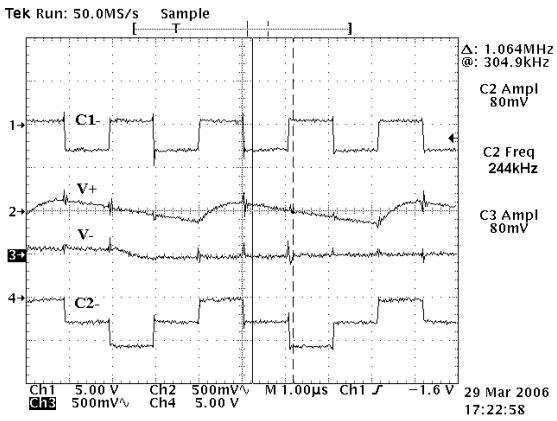


Figure 3 – V_{DD} and V_{SS} Ripple and Fly Capacitor Negative Terminal

Regulated Charge Pump Waveforms – SP3223, V_{CC}=5V, T_A=27°C, TX Loop Back to RX Switching

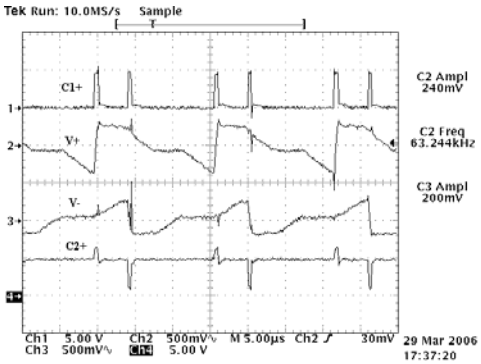


Figure 4 – V_{DD} and V_{SS} Ripple and Fly Capacitor Positive Terminal

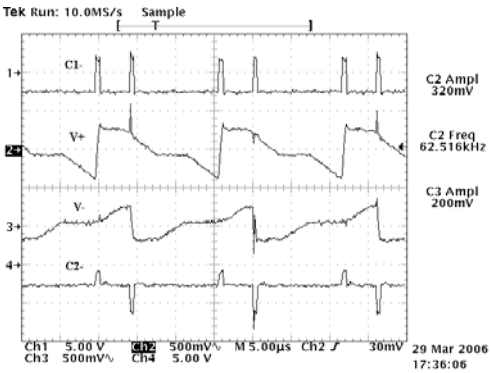


Figure 5 – V_{DD} and V_{SS} Ripple and Fly Capacitor Negative Terminal

 © 2006 Sipex Corporation

Capacitor Values Effect on Circuit Performance

Charge pump capacitor values are critical. Since they are a component of the charge pump circuitry, their value will affect its performance, which in turn affects the VOH and VOL levels of a communication system's transceivers. Initial power up times for a transceiver part will dictate the upper limit for the value of any of the four capacitors. Lower values will impact performance. C1 and C2 are responsible for the charge accumulation and can be reduced, but this will increase the output impedance of V_{DD} and V_{SS} causing voltage loss at the charge pump outputs. Reducing these capacitor values will limit the ability of the transceiver to maintain the DC voltages needed to generate the RS-232 output levels. The capacitor value range for all of the current Sipex products is listed on the Sipex website.[1]

Capacitors C3 and C4 are the output storage elements. They can also be reduced, but doing so will increase the ripple on V_{DD} and V_{SS}. Typically each driver will require 0.1µF of capacitance as a minimum to operate within all specified parameters. If five drivers are active in the circuit, then C3 and C4 must supply more current than if only one driver is active If five drivers are active in the circuit, then C3 and C4 must be larger than if only one driver is active. In order to operate at these minimum values, the supply voltage (V_{CC}) must be maintained at +5.0V ±5%. Also, the ambient operating temperature must follow that specified in the datasheet. The capacitor values can be chosen to suit the particular application. The designer must balance board space, cost, and performance to maximize the design. The capacitors can be polarized or non–polarized, axial-leaded or surface-mount. As the size and value decrease, so does the cost, however, the value should be chosen to accommodate worst-case load conditions.

Capacitor Types

The dielectric material separates the different capacitor types. There are many types with various properties; these properties affect temperature coefficient, working voltage, frequency of operation, aging, physical size, reliability, and price. Surface mount or chip capacitors are in most common use today due to their small size and ruggedness. The types commonly available in chip form are ceramic and electrolytic. Ceramic dielectric is more widely used because it is non-polarized, more stable over temperature, and has lower ESR than either tantalum or aluminum electrolytic dielectric. Ceramic chip capacitors are recommended for these reasons. ESR is a capacitor's equivalent series resistance and is a term in the dissipation factor which is the inverse of the quality (Q) of a capacitor. See Appendix B for the definitions of capacitor dielectric properties. A chart comparing capacitor dielectric properties is shown in appendix C.

Capacitor Working Voltage

The capacitor working voltage is a function of dielectric material breakdown. Capacitors should be operated below the specified working voltage. The information is included in each product datasheet. The charge pump storage caps on V_{DD} and V_{SS} see the charge pump output voltage and not the V_{CC} voltage. A product having V_{CC}=3V and a product with V_{CC}=5V will both output V_{DD}=6V, so the capacitors must have a 10V working voltage. A working voltage of 16V is recommended to provide margin for variations in the application [1].

[1] Refer the FAQs on the Sipex website.
RS-232 Products: http://www.sipex.com/files/FamilyFAQs/RS232FAQ.PDF
Muli-Protocol Products: http://www.sipex.com/files/FamilyFAQs/MultiprotocolFAQ.PDF

 © 2006 Sipex Corporation

Capacitor Temperature Coefficient

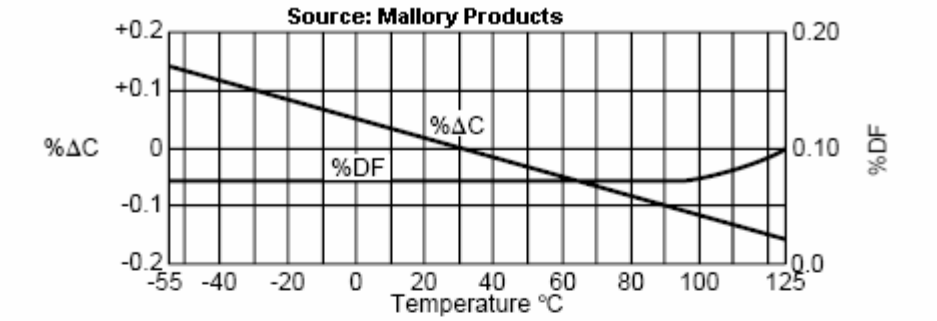
All capacitors have a temperature coefficient (TC). This factor will affect system performance and must be taken into account. Low TC capacitors are preferred but may add cost.

Ceramic capacitors are separated into three common grades of dielectric:

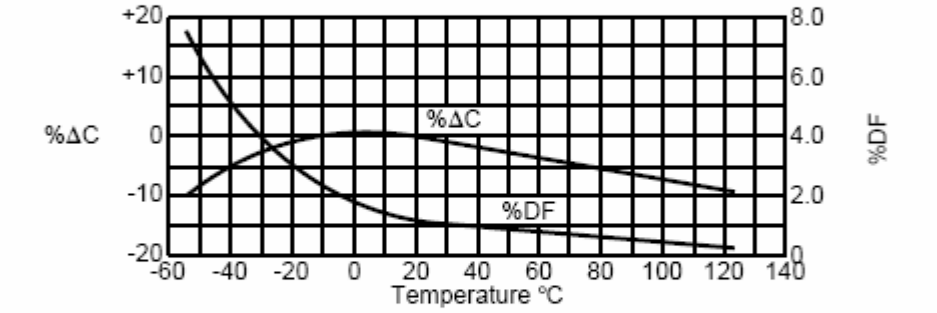
NP0 or C0G: best in all features except permittivity; due to the low K (dielectric constant) of the dielectric. Typical tolerance is 5%. Best temperature performance.

X7R: just a bit more expensive than the low grade Z5U, but improved in tolerance and temperature characteristics. Temperature coefficient is non-linear, however. Typical tolerance is 10%.

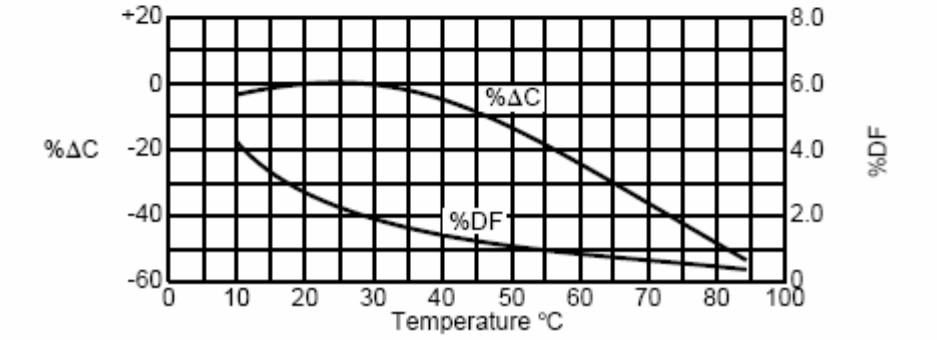
Z5U: Suffers from a relatively large temperature coefficient. Good points include price and size. These are the classic bypass capacitors. Typical tolerance is 20%. Temperature behavior of the 3 ceramic dielectric grades:



Capacitance and Dissipation Factor vs Temperature - COG



Capacitance and Dissipation Factor vs Temperature - X7R



Capacitance and Dissipation Factor vs Temperature - Z5U

 © 2006 Sipex Corporation

V_{CC} Capacitor (Decoupling, Bypass or Input Capacitor)

The decoupling capacitor supplies transient current to the chip. Without decoupling, the IC demands current faster than the power supply connection can supply it, as parts of the circuit rapidly switch on and off. As a result, electronics will frequently use multiple bypass capacitors — a small 0.1 µF rated for high frequencies and a large electrolytic rated for lower frequencies, and occasionally, an intermediate value capacitor. The V_{CC} capacitor will also decrease input voltage and current ripple filtering noise from going back into the power supply. A small 0.1µF capacitor mounted as close to the device as practical is recommended for most interface products. Some of the multi-protocol products recommend larger decoupling capacitors.

PCB Board and System Design

Capacitors should be placed as close to the device as possible. This will optimize the PCB trace parasitic elements of series resistance, series inductance and parallel capacitance. All of these elements will affect performance. The series resistance of the PCB trace will look the same as capacitor ESR to the circuit and reduce the charge pump output.

The charge pump outputs should not be used as an auxiliary output to bias other circuits in your system. The charge pumps are designed to provide enough energy tomaintain the proper bias for the transceiver circuit over all the variations of supply voltage, temperature and integrated circuit process. Therefore, operational margin for the design does not provide for extra loading that additional circuitry would impose on the charge pump.

Measure V_{DD} and V_{SS} Output Resistance for a Regulated Charge Pump

Measure the V_{DD} voltage to determine if the charge pump is regulated. The unregulated voltage for V_{DD} would be two times the V_{CC} voltage. If V_{DD} measures below this with no load the charge pump is regulated. Note that the unloaded regulated V_{DD} voltage is not needed in the calculation.

Load the V_{DD} output with a resistance (R_{LOAD}) low enough to bring the V_{DD} voltage to 2 volts below its regulated output voltage. Record both V_{DD} and R_{LOAD}.

Calculate R_{OUT} using the equation: $$\mathbf{R_{OUT} = (2*V_{CC})-V_{DD}) / (V_{DD}/R_{LOAD})}$$

Given: SP232, V_{CC}=5V, T_A=27°C, R_{LOAD}=200Ω, V_{DD}=4.58V=>R_{OUT} = 237Ω

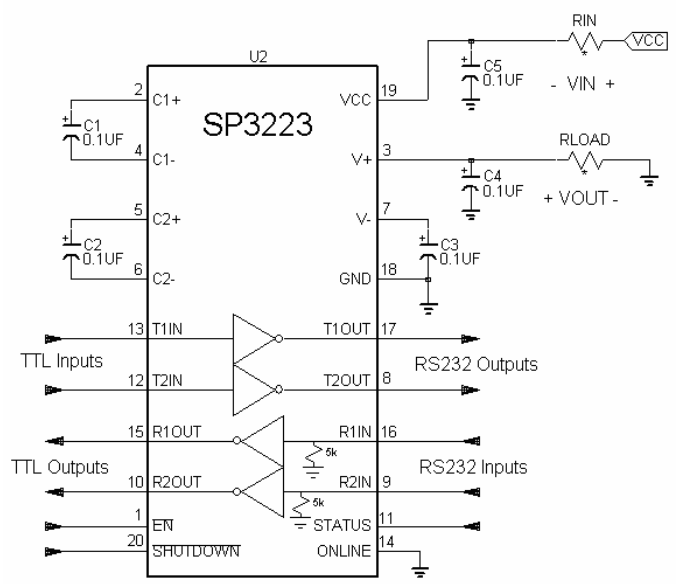
Measure Charge Pump Efficiency

There are many ways to measure efficiency (N);using small value accurate resistors to determine the input and output power is an accurate method. Since the currents in interface circuits are relatively small, the measurement resistor can be relatively large. Efficiency is the same when measuring one output or both outputs, so oneoutput is measured for simplicity.

 © 2006 Sipex Corporation

To measure efficiency for V_{DD} and V_{SS}, load both outputs equally and substitute the P_{OUT} term with: $(V_{DD}^2 + V_{SS}^2)/R_{LOAD}$

Use no signals or loads on the drivers or receivers for this test.
Connect a 1Ω, 0.1% resistor (R_{IN}) in series with the V_{CC} line.
Turn on V_{CC} and measure the voltage drop V_{INQ} across R_{IN} with a voltmeter (V_{DD} is unloaded).
Connect a 600Ω, 0.1% resistor (R_{LOAD}) from V_{DD} to Ground.
The R_{LOAD} value should be set to pull a typical current from the charge pump V_{DD} node.
Measure the voltage drop V_{OUT} across R_{LOAD}.
Measure the voltage drop V_{IN} across R_{IN} again.



$P_{IN} = V_{CC} * I_{IN}$, $I_{IN} = V_{IN}/R_{IN}$

$P_{INQ} = V_{CC} * I_Q$, $I_Q = V_{INQ}/R_{IN}$

$P_{OUT} = V_{OUT} * I_{OUT}$, $I_{OUT} = V_{OUT}/R_{LOAD}$

$N = 100 * P_{OUT} / (P_{IN} + P_{INQ})$

SP232, T_A=27°C, V_{CC}=5V, I_Q= 0.5mA
I_{IN}=13.6mA, V_{OUT}=5.69V, R_{LOAD}=1000Ω, I_{OUT}=5.69mA
N = 100 * 32.5mW / (68mW + 2.5mW) = 45.9 %

Ripple Voltage Measurements

Table 1 – SP3223, V_{DD} and V_{CC} Ripple Voltage versus C_{VDD} and C_{VCC} – V_{CC}=5V, R_L=1kΩ, T_A=27°C

V_{DD} (V)	C_{VDD} (uF)	I_{DD} (mA)	$V_{DDRIPPLE}$ (V)	C_{VCC} (uF)	$V_{CCRIPPLE}$ (V)	I_{IN} (mA)	F (kHz)
5.59	0.10	5.6	1.00	0.10	0.60	13.5	90
5.56	0.22	5.6	0.40	0.10	0.50	13.8	130
5.56	0.47	5.6	0.16	0.10	0.40	14.3	200
5.55	1.00	5.6	0.10	0.10	0.38	14.0	193
5.61	0.10	5.6	0.40	0.22	0.23	13.4	64
5.61	0.10	5.6	0.40	0.47	0.13	13.5	64
5.61	0.10	5.6	0.40	1.00	0.09	13.4	64

Output ripple voltage decreases as the output capacitor (C_{VDD}) is increased. Input ripple voltage decreases as the input capacitor (C_{VCC}) is increased. It is also affected by the storage capacitor value. The charge pump frequency depends on the load current and storage capacitor due to the regulation. The ripple voltage must be measured with an oscilloscope. It is best to use a digital oscilloscope and stop the sampling because the ripple voltage has a large measure of jitter causing the scope to have difficult triggering.

 © 2006 Sipex Corporation

Efficiency and Output Resistance Measurements

Table 2 – SP3223, Efficiency and Output Resistance versus Load Current and V_{CC}, T_A=27°C

V_{CC} (V)	R_{LOAD} (V)	V_{DD} (Ω)	I_{IN} (mA)	V_{RIPPLE} (V)	F (kHz)	I_{OUT} (mA)	N (%)	R_{OUT} (Ω)
5	1000000	5.79	0.5	0.600	0.3	0.006	0.7	727116
5	3000	5.60	5.0	0.800	38	1.9	38.0	2357
5	2000	5.67	7.2	0.800	50	2.8	41.8	1527
5	1000	5.69	13.6	0.920	90	5.7	45.9	757
5	500	5.36	24.9	1.290	102	10.7	45.2	433
5	400	5.44	31.9	0.920	194	13.6	45.7	335
5	300	5.11	38.4	1.420	130	17.0	44.8	287
5	200	4.58	62.5	1.300	125	22.9	33.3	237
5	150	4.30	96.2	0.900	152	28.7	25.5	199
5	100	4.18	125.3	0.600	177	41.8	27.8	139
5	50	4.10	175.8	0.200	195	82.0	38.1	72
3	30000	5.54	1.2	0.154	11	0.2	12.0	2473
3	3000	5.52	6.2	0.150	277	1.8	30.1	263
3	2000	5.51	8.1	0.146	223	2.8	35.3	177
3	1000	5.26	12.8	0.260	227	5.3	41.9	141

The efficiency is typically around 46% when the part is in regulation. The efficiency number is low for this product running at V_{CC}=5V, because the charge pump topology uses doublers but is regulated to 5.7V. If the output voltage was 10V the efficiency would approach 100%. The efficiency decreases when V_{CC}=3V because the part is regulating and therefore switching more often to maintain the same output voltage. The efficiency includes the quiescent current attributed to the input voltage. The output resistance of the charge pump averages 250Ω when in regulation and increases linearly when driven out of regulation

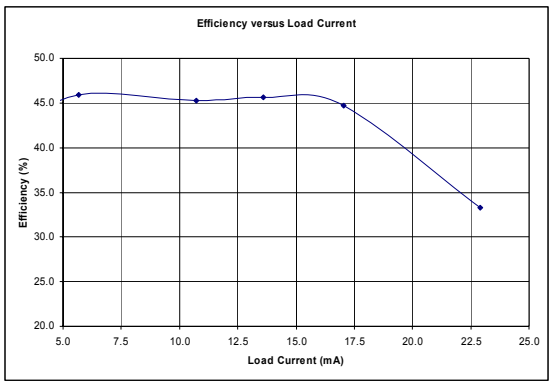


Figure 6 - Efficiency vs. Load Current – SP3223

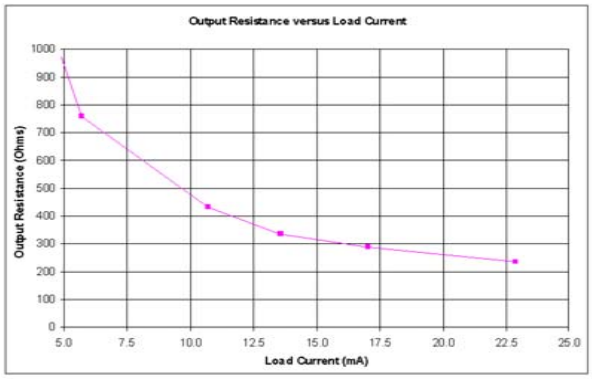


Figure 7 - Output Resistance versus Load Current - SP3223

 © 2006 Sipex Corporation

Power-On or Start-Up Time

Sipex conducted an empirical study on the SP232 to determine the effect of charge pump capacitor values on initial power-up times. The data provides a guideline for power-up time requirements for system designers. The transmitter output will be ready to transmit data after the times given in the table. The data is given for different supply ramp rates and charge pump capacitor values. This is a typical time value based on a small sample size and is not a guarantee, only a guideline. A robust design should provide at least 100% margin.

Table 3 –Time to T1 Final Output Voltage versus Power Supply Ramp and Charge Pump Capacitor Value

Capacitance (µF) =>	0.1	1.0	4.7
Supply Ramp Time (ms)	The Time for $T1_{OUT}$ to reach it's final value (ms)		
4.8	0	1.2	9.6
6.4	0	0.8	8
12	0	0.4	6.4
24	0	0	4
50	0	0	2.4

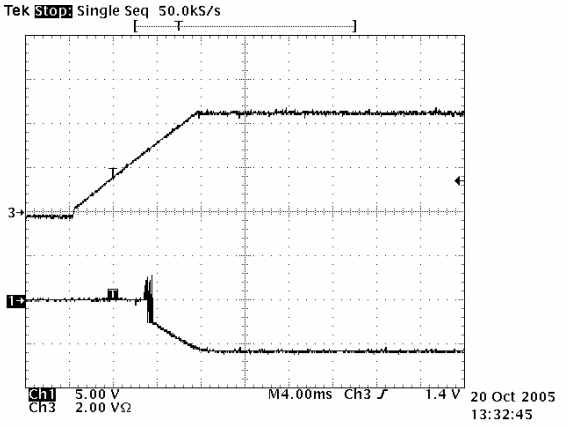


Figure 8 – Cpump=1.0µF, Ramp=12ms

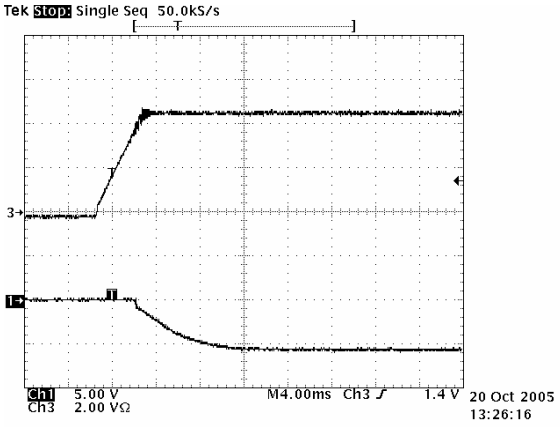


Figure 9 – Cpump=4.7µF, Ramp=4.8ms

The time for T1out to reach it's final value is measured from the end of the supply ramp. There is only a small delay (<1ms) for 0.1µF charge pump capacitors.

 © 2006 Sipex Corporation

Summary

- Charge pump strength is determined by the flying caps.
- Charge pump ripple is determined by the storage caps.
- Capacitor values can be tuned to a specific application.
- Simple tests for R_{OUT}, ripple voltage and efficiency can be conducted to ensure proper operation when selecting cap values.
- R_{OUT} indicates the relative strength of a charge pump.
- Efficiency indicates a well tuned pump for a given operating load.
- Ripple voltage and start-up time trade off when selecting the storage caps.
- Stay within the recommended capacitor value range for reliable performance.
- Refer to the RS-232 FAQ on the Sipex website for the recommended Capacitor value ranges for interface products.
- Ceramic capacitors are recommended due to their low ESR, low TC, long life and small size.

 © 2006 Sipex Corporation

Appendix A

Charge Pump Equations

C1 and C2 are the flying capacitors, while C3 and C4 are the output storage or load capacitors (CL).

Peak-to-peak output ripple voltage is: $V_{RIPPLE} = [I_{OUT} / (2*f_{PUMP}*C_L)] + I_{OUT}*ESR_{CL}$

Output ripple voltage is calculated by noting that capacitor CL supplies the output current during one half of the charge pump cycle. I_{OUT} is the quiescent and load current of all the transceivers for a product.

Losses in applications can be anticipated from the following:

Charge Pump Output Resistance: $V_{LOSS} = I_{LOAD} \times R_{OUT}$

Where V_{LOSS} is the voltage drop due to the output resistance, I_{OUT} is the load current, and R_{OUT} is the output resistance.

Fly Capacitor ESR: $V_{LOSSC1,C2} = 4 \times (ESR_{C1}+ESR_{C2}) \times I_{OUT}$

Where V_{LOSS} C1, C2 is the voltage drop due to the charge pump capacitor, C1+C2, ESR is the equivalent series resistance of C1+C2, and I_{OUT} is the load current. The losses in C1 and C2 are larger than the losses in the reservoir capacitors, C3 and C4, because they handle a current almost four times larger than the load current during charge pump operation. As a result of this, a change in the capacitor ESR has a much greater impact on the performance for C1 than for C2.

Storage Capacitor ESR: $V_{LOSSC3,C4} = ESR_{C3,C4} \times I_{OUT}$

Where V_{LOSS} C3, C4 is the voltage drop due to the storage capacitors C3 and C4, $ESR_{C3, C4}$ is the ESR of C3 and C4, and I_{LOAD} is the load current. Increasing the capacitance of C3 and C4 and/or reducing its ESR can reduce the output ripple that may be caused by the charge pump. A designer can filter high-frequency noise at the output by implementing a low ESR capacitor at C3 and C4. Generally, capacitors with larger capacitance values and higher voltage ratings tend to reduce ESR.

Effective Open Loop Output Resistance (R_{OL})

The effective open loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency (F_{OSC}), value of the flying capacitor (C_{FLY}), the non-overlap time, the total internal switch resistances (ΣR_S), and the ESR of the external capacitors. A first order approximation for R_{OL} is given below: The effective open loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator

 © 2006 Sipex Corporation

frequency (F_{OSC}), value of the flying capacitor (C_{FLY}), the non-overlap time, the internal switch resistances (R_S), and the ESR of the external capacitors. A first order approximation for R_{OL} is given below:

$R_{OL} = 2\Sigma R_S + 1 / (F_{OSC} * C_{FLY})$

For very light load applications, the flying capacitor may be reduced to save space or cost.

From the first order approximation of above, the theoretical minimum output resistance of a voltage doubling charge pump can be expressed by the following equation:

$R_{OL\ (MIN)} = (2V_{IN}-V_{OUT})/I_{OUT}\ \ 1 / (F_{OSC} * C_{FLY})$

Where, F_{OSC} is the switching frequency and C_{FLY} is the value of the flying capacitor. The charge pump will typically be weaker than the theoretical limit due to additional switch resistance. However, the above expression can be used as a guideline in determining a starting capacitor value.

Efficiency

A charge pump theoretically produces a doubled voltage at 100% efficiency. However in the real world, there is a small voltage drop on the output which reduces the output efficiency. Charge Pumps can usually run 99.9% efficient without driving a load. While driving a load, the efficiency remains over 90%.

Output Voltage Efficiency = $V_{OUT} / (-2 * V_{CC})$;
$V_{OUT} = -2 * V_{CC} + V_{DROP}$
$V_{DROP} = (I_{OUT}) * (R_{OUT})$
Power Loss = $I_{OUT} * (V_{DROP})$

The efficiency changes as the external charge pump capacitors are varied. Larger capacitor values will strengthen the output and reduce output ripple. Although smaller capacitors will cost less and save board space, lower values will reduce the output drive capability and also increase the output ripple.

The ESR of the charge pump capacitors also determines the output resistance. Assuming that switch resistances are approximately equal, the output resistance can be derived as shown below:

$R_{OUT} = 16 * (R_{SW1-3}) + 4 * (ESR_{C1} + ESR_{C2}) + ESR_{C3,C4} + 1 / (F_{OSC} * C_1) + 1 / (F_{OSC} * C_2)$

The outputs of devices that are not regulated are dependent on the output resistance and the amount of load current. As the load current increases, losses may slightly increase at the output and the voltage may drop slightly. The loss at the positive output, V_{LOSS}, equals the current draw, I_{OUT}, from V_{OUT} times the charge pump's source or output resistance, R_{OUT}:

$V_{LOSS} = I_{OUT} \times R_{OUT}$

The actual output voltage at V_{OUT} will be two times the voltage difference of V_{IN} and V_{LOSS}:

 © 2006 Sipex Corporation

$$V_{OUT} = 2(V_{IN} - V_{LOSS})$$

Theoretically, the total power loss of a switched capacitor voltage converter can be summed up as follows:

$$P_{LOSS} = P_{INT} + P_{CAP} + P_{CONV}$$

Where P_{LOSS} is the total power loss, P_{INT} is the total internal loss in the IC including any losses in the MOSFET switches, P_{CAP} is the resistive loss of the charge pump capacitors, and P_{CONV} is the total conversion loss during charge transfer between the flying and output capacitors. These are the three theoretical factors that may affect the power efficiency of devices. Internal losses come from the power dissipated in the IC's internal circuitry. Losses in the charge pump capacitors will be induced by the capacitors' ESR. The effects of the ESR losses and the output resistance can be found in the following equation: $I_{OUT}^2 \times R_{OUT} = P_{CAP} + P_{CONV}$
And

$$R_{OUT} \approx 4 \times (2 \times R_{SWITCHES} + ESR_{C1} + ESR_{C2}) + 1 / F_{OSC} \times C_1$$

Where I_{OUT} is the output current, R_{OUT} is the circuit's output resistance, $R_{SWITCHES}$ is the internal resistance of the MOSFET switches, ESR_{C1} and ESR_{C2} are the ESR of their respective capacitors, and F_{OSC} is the oscillator frequency. Conversion losses will happen during the charge transfer between the flying capacitor, C_1, C_2 and the output capacitor, C_3 or C_4 when there is a voltage difference between them. P_{CONV} can be determined by the following equation:

$$P_{CONV} = F_{OSC} \times [1/2 \times (C_1+C_2) \times (V_{IN}^2 - V_{OUT}^2) + 1/2 \times C_3 \times (V_{RIPPLE}^2 - 2 \times V_{OUT} \times V_{RIPPLE})]$$

Actual Efficiency
To determine the actual efficiency of operation, a designer can use the following equation:

$$Efficiency\ (ACTUAL) = \times 100\%\ P_{OUT} / P_{IN}$$

Where $P_{OUT} = V_{OUT} \times I_{OUT}$ and $P_{IN} = V_{IN} \times I_{IN}$ where P_{OUT} is the power output, V_{OUT} is the output voltage, I_{OUT} is the output current, P_{IN} is the power from the supply driving the device, V_{IN} is the supply input voltage, and I_{IN} is the supply input current.

 © 2006 Sipex Corporation

Appendix B

Glossary - http://xtronics.com/reference/esr.htm

The ESR rating of a capacitor is a rating of quality. A theoretically perfect capacitor would be lossless and have an ESR of zero. It would have no in-phase AC resistance. Realistically, however, all capacitors have some amount of ESR. To understand why, let us review what a capacitor is and what they are made of and how we rate them.

What is a Capacitor?
A capacitor consists of two conductive metal plates separated by an insulating dielectric. The dielectric can be made of glass, ceramic, tantalum oxide, or plastics such as polyethylene or polycarbonate. Even air can be used as the dielectric. When the capacitor holds some energy in the form of extra electrons on one plate and electron holes on the other we say that the capacitor is charged.

Farads
Capacitance (C) is the amount of charge per Volt of potential that a capacitor holds. (C =Q/V where Q = coulombs (the unit of charge) and V = Volts)

Capacitance is measured in Farads, but most often a small fraction of a Farad thus:

- micro-Farads,μF, (10^{-6}) Farads
- pico-Farads,pF, (10^{-12}) Farads (sometimes called 'puffs' in engineering slang)

The energy stored in a capacitor is $E = CV^2/2$ E is in joules.

Thus, the average power in watts is $P_{av} = CV^2/2t$ where t = time in seconds.

The maximum voltage rating and its capacitance determine the amount of energy a capacitor holds. The voltage rating increases with increasing dielectric strength and the thickness of the dielectric. The capacitance increases with the area of the plates and decreases with the thickness of the dielectric.

Thus, the capacitance of a capacitor (C) is related to the plate area (A), plate separation distance (d) and permittivity (ε) of the dielectric by the following equation:

$C = \varepsilon A/d$ Here A and d are based on meters as the unit and ε is in coulombs squared per Newton-meters squared.

 © 2006 Sipex Corporation

Dielectric Constants
Dielectric constant (*k*) gets its value by comparison of the charge holding ability of a vacuum where *k* = 1. Thus, *k* is the ratio of the capacitance with a volume of dielectric compared to that of a vacuum dielectric.

$K = \varepsilon_d/\varepsilon_0$ Where ε_d is the permittivity of the dielectric and ε_0 is the permittivity of free space.

Air has nearly the same dielectric value as a vacuum with *k* = 1.0001. Teflon, a very good insulator, has a value of *k* =2 while the plastics range in the low 2s to low 3s. Mica has a value of *k* =6. Aluminum oxide is 7, tantalum's *k* is 11 and the ceramics range from 35 to over 6,000.

Dielectric constants vary with temperature, voltage, and frequency making capacitors messy devices to characterize. Whole books have been written about choosing the correct dielectric for an application, balancing the desires of temperature range, temperature stability, size, cost, reliability, dielectric absorption, voltage coefficients, current handling capacity, and ESR.

Dielectric strength
Dielectric strength is a property of the dielectric that is usually expressed in volts per mil (V/.001") or volts per centimeter (V/cm). If we exceed the dielectric strength, an electric arc will 'flash over' and often weld the plates of a capacitor together.

Q or Quality Factor
The *Q* of a capacitor is important in tuned circuits because they are more damped and have a broader tuning point as the *Q* goes down.

$Q = 1/RX_C$ where X_C is the capacitive reactance *where* $X_C = 1/(2\pi FC)$ and *R* is the 'soon to be defined term of ESR'.

Q is proportional to the inverse of the amount of energy dissipated in the capacitor. Thus, ESR rating of a capacitor is inversely related to its quality.

Dissipation Factor
The inverse of Q is the dissipation factor (δ). Thus, $\delta = ESR/X_C$ and the higher the ESR the more losses in the capacitor and the more power we dissipate. If too much energy is dissipated in the capacitor, it heats up to the point that values change (causing drift in operation) or failure of the capacitor.

Ripple Current Rating
The ripple current is sometimes rated for a capacitor in RMS current. Remembering that $P = I^2R$ where R in this case is ESR, it is plain to see that this is a power dissipation rating.

 © 2006 Sipex Corporation

Dielectric Absorption
This is the phenomenon where after a capacitor has been charged for some time, and then discharged, some stored charge will migrate out of the dielectric over time, thus changing the voltage value of the capacitor. This is extremely important in sample and hold circuit applications. The typical method of observing dielectric absorption is to charge up a capacitor to a known DC voltage for a given time, then discharge the capacitor through a 2Ω resistor for one second, then watch the voltage on a high-input-impedance voltmeter. The ratio of recovered voltage (expressed in percent) is the usual term for dielectric absorption.

The charge absorption effect is caused by a trapped space charge in the dielectric and is dependent on the geometry and leakage of the dielectric material.

ESL
ESL (Equivalent Series Inductance) is pretty much caused by the inductance of the electrodes and leads. The ESL of a capacitor sets the limiting factor of how well (or fast) a capacitor can de-couple noise off a power bus.

The ESL of a capacitor also sets the resonate-point of a capacitor. Because the inductance appears in series with the capacitor, they form a tank circuit.

ESR Defined
ESR is the sum of in-phase AC resistance. It includes resistance of the dielectric, plate material, electrolytic solution, and terminal leads at a particular frequency. ESR acts like a resistor in series with a capacitor (thus the name Equivalent Series Resistance). This resister can cause circuits to fail that look just fine on paper and is often the failure mode of capacitors.

To charge the dielectric material, current needs to flow down the leads, through the lead plate junction, through the plates themselves, and even through the dielectric material. The dielectric losses can be thought of as friction of aligning dipoles and thus appear as an increase (or a reduction of the rate of decrease, this increase is what makes the resistance vs. frequency line to go flat) of measured ESR as frequency increases.

As the dielectric thickness increases, so does the ESR. As the plate area increases, the ESR will go down if the plate thickness remains the same.

 © 2006 Sipex Corporation

Formulas at a glance

$$\delta = \frac{ESR}{X_c}$$

$$X_c = \frac{1}{2\ \pi CF}$$

$$X_L = 2\ \pi LF$$

$$\omega = 2\ \pi F$$

$$I = \frac{E}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

$$F_r = \frac{1}{2\pi\sqrt{LC}}$$

Where *k* = dielectric constant, *A* = area, *t* = thickness of the dielectric, *Q* = coulombs the unit of charge, and *V* = Volts

$$C = \frac{(8.85 \times 10^{-12})kA}{t}$$

$$C = \frac{Q}{V}$$

Where *A* (area) and *d* (thickness) use meters as the unit and ε is in coulombs (squared per Newton-meters squared), ε_d is the permittivity of the dielectric, and ε_0 is the permittivity of free space

$$C = \frac{\in A}{d}$$

$$k = \frac{\in_d}{\in_0}$$

Where energy *E* (in joules) stored in a capacitor is given by

 © 2006 Sipex Corporation

$$E = \frac{CV^2}{2}$$

Thus, the average power in watts where *t* = time in seconds.

$$P_{av} = \frac{CV^2}{2t}$$

$$Z_0 = \sqrt{ERS^2 + X_c^{\ 2}}$$

- Time Domain Refletometry (TDR) formulas
- Characteristic Impedance of cable formulas
- Discontinuance of transmission characteristic impedance

Z_a = characteristic impedance through which the incident wave travels first and Z_b is the characteristic impedance through which the incident wave travels next. V_r is the reflected wave amplitude, V_i is the incident wave amplitude, and V_t is the transmitted wave amplitude.

$$\frac{\mathrm{Vr}}{\mathrm{Vi}} = \frac{\mathrm{Zb} - \mathrm{Za}}{\mathrm{Zb} + \mathrm{Za}}$$

$$\frac{\mathrm{Vr}}{\mathrm{Vt}} = \frac{2\,\mathrm{Zb}}{\mathrm{Zb} + \mathrm{Za}}$$

$$\mathrm{Zb} = \mathrm{Za}\,\frac{\mathrm{Vi} + \mathrm{Vr}}{\mathrm{Vi} - \mathrm{Vr}}$$

Where Z_0 is the characteristic impedance:

$$\tau = RC = \frac{Z_0}{2}C$$

 © 2006 Sipex Corporation

Capacitor Dielectric Comparison Chart

		Multi-Layer Ceramics							Multi-Layer Glass-K									
Characteristics		NP0	Stable	HiK	Ceramic Discs	Internal Barrier Layer	Reduced Titanates	Multi-Layer Glass	"T" Characteristic	"U" Characteristic	"V" Characteristic	Mica	Polyester	Poly-carbonate	Poly-propylene	Poly-styrene	Solid Tantalums	Aluminum Electrolytics
Capacitance	Range, mfd	1pF – .01µF	1pF – 2.2µF	.001 – 10µF	1pF 0.1µF	.01 – .22µF	.01 – 1.0µF	0.5pF – .01µF	270pF – .02µF	.012 – .039µF	.022 – .1µF	1pF – .09µF	.001 – 10µF	.001 – 10µF	47 – .047µF	100pF – .027µF	.01 – 1000µF	0.5 – 10^6µF
	Min. Tol. Avail. %	±0.5%	±5%	±20%	Same as Multi-layers	±20%	±20%	±0.5%	±5%	±10%	±10%	±0.5%	±5%	±1%	±0.5%	±0.5%	±5%	±20%
	Std. Tol. %	±5%, ±10%	±10%	+80%, -20%	Same as Multi-layers	+80%, -20%	+80%, -20%	±1%, ±5%	±5%, ±10%	±5%, ±10%	±5%, ±10%	±1%, ±5%	±10%	±10%	±5%	±5%	±20%	+100%, -10%
Voltage Range	Typical, VDC	50 – 200	50 – 200	25 – 100	50 – 10,000	50	3 – 50	50 – 2000	25 – 50	25 – 50	25 – 50	50 – 500	100 – 600	100 – 600	100 – 600	30 – 600	6 – 125	3 – 500
Temperature	Range, °C	-55°C, +125°C	-55°C, +125°C	+10°C, +85°C and -55°C, +85°C	-55°C, +85°C	-55°C, +85°C	-55°C, +85°C	-75°C, +200°C	-75°C, +200°C	-75°C, +200°C	-75°C, +200°C	-55°C, +125°C	-55°C, +125°C	-55°C, +125°C	-55°C, +85°C	-55°C, +70°C	-55°C, +125°C	-40°C, +85°C
	T.C. %Δ C	±0.3%	±15%	+22%, –56% and –22%, –80%	Same as Multi-layers	±30%	±10%, ±30%	±1.65%	+2%, –10%	–2%, –15%	+20%, –45%	-.4%, +1.8%	±12%	±2%	±2.5%	±1%	±8%	±10%
I.R.	<1.0 mfd	10^5 MΩ	10^5 MΩ	10^4 MΩ	Same as Multi-layers	10^4 MΩ	10 MΩ	10^5 MΩ	10^4 MΩ	10^4 MΩ	10^4 MΩ	10^2 MΩ	10^4 MΩ	10^5 MΩ	10^5 MΩ	10^6 MΩ	10^2 MΩ	N.A.
	>1.0 mfd MΩ –mfd	N.A.	2,500	1,000	N.A.	N.A.	0.1	N.A.	N.A.	N.A.	N.A.	N.A.	10^3	10^4	N.A.	N.A.	10	100
Dissipation Factor	Percent At 1KHz, %	0.1%	2.5%	3.0%	0.1% to 4.0%	5.0%	5% to 10%	0.2%	1.0%	1.5%	3.0%	0.1%	2%	1.0%	0.35%	.1%	8% to 24%	8% (at 120 Hz)
Dielectric Absorption	Percent Typical, %	0.6%	2.5%	N.A.	Same as Multi-layers	N.A.	N.A.	.05%	0.1%	0.1%	1.3%	0.3% – 0.7%	0.5%	0.35%	.05%	.05%	N.A.	N.A.
Frequency Response	Freq. Response 10 = Best, 1 = Poorest	9	8	8	8	3	2	9	8	8	8	7	6	6	6	6	5	2
	Max. Freq. (MHz) For Δ C = ±10%	100	10	10	Same as Multi-layers	10	1	100	100	75	10	100	N.A.	N.A.	N.A.	N.A.	.002	N.A.
Stability (1000 Hrs.)	Typical Life Test, %Δ C	0.1%	10%	20%	Same as Multi-layers	20%	20%	0.5%	5%	10%	20%	0.1%	10%	5%	3%	2%	10%	10%
Polarity	Single Cap	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	N.P.	P	P

NOTICE: Specifications are subject to change without notice. Contact your nearest AVX Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable, but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should not assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all applications.

© AVX Corporation