Product Change Notification / SYST-17JQZJ208

Date:

19-Mar-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - ATmega3208/3209 Data Sheet Document Revision

Affected CPNs:

SYST-17JQZJ208_Affected_CPN_03192021.pdf
SYST-17JQZJ208_Affected_CPN_03192021.csv

Notification Text:

SYST-17JQZJ208

Microchip has released a new Product Documents for the ATmega3208/3209 Data Sheet of devices. If you are using one of these devices please read the document located at ATmega3208/3209 Data Sheet.

Notification Status: Final

Description of Change:

1)Entire Document

a)Terminology update:

– The SPI and TWI standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

b)Editorial updates throughout the document

2)Table of Contents

a)Removed the peripheral name in the title under the peripheral Register Summary and Register Description sections

b)The Crystal Error Correction section is added

3)megaAVR® 0-series Overview

a)Updated the megaAVR® Device Designations figure

4)Features

a)Speed grade range upper limit is changed from -40°C to +105°C. Speed grade range added for Automotive part

5)Pinout - RESET text added for pin PF6

6)AVR® CPU

a)The Arithmetic Logic Unit (ALU) section is updated to differentiate between register and working register

b)Program Flow section is updated to clarify changes in the program flow

c)The Stack and Stack Pointer section is updated:

– Clarify the pushing and popping of data onto the stack

– The reference to EICAL instruction removed

d)The Register File section is updated to clarify instruction access to the register file

e)The X-, Y-, and Z-Register section is updated to differentiate between register and working register and certify the different addressing modes

f)The Status Register description is updated to be in line with the AVR Instruction Set description

g)The Accessing 16-Bit Registers section is added

7)Peripherals and Architecture

a)The Interrupt vector Mapping table is updated :

– Added Description and Peripherals Source names columns

– The Vector Address changed to Program address (word)

8)NVMCTRL - Nonvolatile Memory Controller

a)Updated the NVMCTRL Block Diagram for better understanding of the NVMCTRL peripheral

b)Improved the Set Up Flash Sections table description of the boot section lock and application code sections

c)Added a section detailing the write access after Power-on Reset

d)Added the NVMCTRL.CTRLB to registers under Configuration Change Protection

9)CLKCTRL - Clock Controller

a)Corrected the Block Diagram by removing the TCD timer which is not present on this device

b)Updated the MCLKCTRLB, PDIV bit field description (table changed)

10)SLPCTRL - Sleep Controller

a)In the Sleep Mode Activity Overview for Peripherals table:

– Removed column Clock and Group

– Updated notes below the table

b)Added separate tables Sleep Mode Activity for Clock Source and Sleep Mode Activity Wake-up Sources

11)RSTCTRL - Reset Controller

a)Updated Features to improve the readability of Reset sources grouping Power Supply Reset Sources and User Reset Sources

b)Improved the working principle of the different reset sources and inclusion of timing diagrams in Functional Description under Initialization section

c)In the Logic Domains Affected by Various Resets table removed columns:

– TCD Pin Override Functionality Available

– Reset of TCD Pin Override Settings

– Reset of BOD configuration

d)Clarified the behavior of the flags in the Reset Flag (RSTFR) register after a POR has occurred

e)Updated the description in the Power-on Reset (POR) section

12)CPUINT - CPU Interrupt Controller

a)Added a table to improve the description, and moved relevant text below figures, in the Interrupt Response Time section

b)In the High-Priority Interrupt section: Clarified that priority level 1 will interrupt priority level 0 interrupts

c)Added the Debug Operation section

d)Corrected the terminology from number to address in the Interrupt Vector with Priority Level 1 register description

13)EVSYS - Event System

a)Improved the Block Diagram figure by adding EVOUTx

b)In the Event Generators section, improved readability by adding the Properties of Generated Events and the Event Generators tables.

c)Added information on event user synchronization

14)PORT - I/O Pin Configuration

a)Improved the Overview text and the Block Diagram

b)Updated Functional Description:

– Added optional initialization steps

– Moved Pin n Control offset from Basic Functions to Pin Configuration

– Clarified that the pull-up is disabled when the output driver is enabled

– Moved interrupt settings considerations from the Pin Configuration to the Interrupt section

– Updated the Asynchronous Sensing Pin Properties section

– Updated the Events section per AVR best practice

– Added the Debug Operation section per AVR best practice

c)Updated the Registers Description per AVR best practice

15)WDT - Watchdog Timer

a)Improved the Block Diagram

b)Corrected the oscillator frequency from 1 kHz to 1.024 kHz, and 32 kHz to 32.768 kHz

c)In the Control A register description in the Window bit field table, the precision of the values have been corrected

16)TCA - 16-bit Timer/Counter Type A

a)Clarifications added

– For single-slope PWM generation, counting from TOP to BOTTOM is not supported

– Dual-slope PWM results in approx. half the maximum operation frequency compared to single-slope PWM operation, due to twice the number of timer increments per period

– Added timing diagram for split mode

– Event actions with level input detection work reliably only if the event frequency is lower than the timer's frequency

– (H/L)CMPnOV bits in CTRLC in normal and split mode: When the output is connected to the pad, overriding these bits requires the CMPnEN bits in the TCAn.CTRLB register to be enabled. The CMPnEN bit is bypassed when the output is connected to the CCL.

– LUPD bit in CTRLESET/CLR: LUPD does not prevent an update issued by CTRLE.CMD

– For operation modes with update condition on BOTTOM and compare interrupt enabled: (1) If CMPn=0, an interrupt will be given together with the update at BOTTOM (2) If CMPnBUF=0, an interrupt will be given the next time the counter reaches BOTTOM

17)TCB - 16-bit Timer/Counter Type B

a)The Initialization section is updated to include an optional step to enable waveform output on a pin

b)Time-Out Check Mode_ Input Capture on Event Mode, Input Capture Frequency Measurement Mode, Input Capture Pulse-Width Measurement Mode, Input Capture Frequency and Pulse-Width Measurement Mode, Single-Shot Mode sections explanation about TCB as event user added

c)In the Single-Shot Mode section, the EDGE bit explanation is corrected

d)In the 8-Bit PWM Mode section, the explanation of duty cycle and period is corrected

e)In the Output section, the explanation of the CCMPEN bit is added

f)In the Events section, the reference to the OVF event and the COUNT event user are removed

g)The Control B register description is updated:

– The CCMPINIT bit has no effect in Single-Shot and 8-bit PWM mode

– Improved description of the CCMPEN bit

h)The Event Control register description: The EDGE bit explanation is corrected

i)The Temporary Value register description is improved

j)The Capture/Compare register description explanation of the duty cycle and period is corrected

18)RTC - Real-Time Counter

a)Restructured the Events Generators in RTC table:

– Added a table for the Interrupt Control and the Periodic Interrupt Timer Control A registers

– Added the Feature Crystal Error Correction and related text

– Added the Frequency Error Correction bit in the CTRLA register

– Added the Crystal Frequency Calibration register

19)USART - Universal Synchronous and Asynchronous Receiver and Transmitter

a)In the Overview section:

– single - write is changed to two level - write

b)In the Feature list and the IRCOM TXPLCTRL register, system clock is change to peripheral clock

c)Changed the Block diagram text

d)Added information about the TX Buffer register

e)Restructured the Data Transmission and the Data Reception sections

f)Auto Baud section text regarding tolerance configuration is added

g)Register text restructure and bit fields tables added:

– Receiver Data Register Low Byte, Receiver Data Register High Byte register, and USART Status

– USART Status register table added for the configuration of the bit field WFB

– Control A, Control B register table added for bit field configuration

– Control D register text was restructured and table values regarding tolerance are updated

– IrDA Control register added table

h)Register name changed from Control C - Asynchronous Mode to Control C - Normal Mode

20)SPI - Serial Peripheral Interface

a)First Receive Buffer and Second Receive Buffer registers now referred to as Receive Data Register and Receive Data Register

21)TWI - Two-Wire Interface

a)Updated the Features section terminology

b)Added the Debug Operation section

c)Clarifications and corrections

– Description of Bus Error (BUSERR) in MSTATUS and SSTATUS registers

– Description of Address Packet Flag Activation of Read/Write Interrupt Flags (WIF/RIF) in MSTATUS register

– Description of Data and Address or Stop Interrupt Flags (DIF/ APIF) in SSTATUS register

– Behavior of the Acknowledge Action (ACKACT) bit in MCTRLB, MDATA, SCTRLB registers

– The Clock Generation section is expanded to ensure correct low times for SCL in Fm+ mode

22)CRCSCAN - Cyclic Redundancy Check Memory Scan

a)Improved description of CRC scan in ENABLE bit in the Control A (CRCSCAN.CTRLA) register, and the OK bit in the Status (CRCSCAN.STATUS) register

b)Added missing CRC Flash Access Mode (MODE) bit field in the Control B (CRCSCAN.CTRLB) register

23)CCL - Configurable Custom Logic

a)LUTn-IN[] has been renamed to LUTn-TRUTHSEL[] to better reflect its functionality

b)The Truth Table Logic section is rewritten for clarity and an example is added

c)The Event Input Selection (EVENTx) section reference to a wrong register is corrected

d)The CTRLA register description is rewritten for clarity

e)The TRUTHn register description is updated to include a truth table

24)AC - Analog Comparator

a)The Input Sources section: Fixed typo from MUXTRLA to MUXCTRLA

b)The Power Modes section: Fixed bug from MODE to LPMODE

c)The Internal Inputs section: Fixed typo from DAC to AC

d)Restructured the text for the Events section

e)Added a title to the bit field table INTMODE in Control A register

f)Restructured the text for the INVERT bit field in the MUX Control register

g)Restructured the text for the DAC Voltage Reference register

25)ADC - Analog-to-Digital Converter

a)Added the Definitions section to define terms such as Offset or Gain Error, Integral Non-Linearity, and Differential Non-Linearity among others

b)Correction of the bit field name from WCOMP to WCMP, in both INTCTRL and INTFLAG registers

26)UPDI - Unified Program and Debug Interface

a)Reorganized the BREAK Character section into BREAK and SYNCH with some more details

b)In the ASI Control A register added the missing value, 0x00 (32 MHz UPDI Clock), to the UPDI Clock Select bit field

c)In the Status A register, the UPDI Revision bit field Access Reset is corrected from 0x01 to 0x03

27)Electrical Characteristics

a)General Operating Ratings

– Clarified ranges in the Maximum Frequency vs. VDD figures

– Added Maximum Frequency vs. VDD figure for automotive range parts

b)Power Consumption

– Clarified clock source for the Active/Idle Supply vs. Frequency plots

– Added a Max. 25°C column in the Power Consumption in PowerDown, Standby and Reset Mode table

c)External Reset Characteristics

– Number for tMIN_RST max limit updated

d)TWI

– Updated the TWI - Specifications table with typical numbers for tHD;STA, tSU;STA, tSU;STD and tBUF

– Added SDA Hold Time table

e)TEMPSENSE Characteristics

– Added the TEMPSENSE Characteristics section

f)UPDI

– Updated the UPDI Max. Bit Rates vs. VDD table

28)Package Drawings - Section Package Marking Information added

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 19 Mar 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATmega3208/3209 Data Sheet

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Affected Catalog Part Numbers (CPN)

ATMEGA3208-AF
ATMEGA3208-AFR
ATMEGA3208-AU
ATMEGA3208-AUR
ATMEGA3208-MF
ATMEGA3208-MFR
ATMEGA3208-MU
ATMEGA3208-MUR
ATMEGA3208-XF
ATMEGA3208-XFR
ATMEGA3208-XU
ATMEGA3208-XUR
ATMEGA3209-AF
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ATMEGA3209-AUR
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