

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# NCV6354

## 3MHz, 2A Fixed-Frequency Synchronous Buck Converter

### High Efficiency, Low Ripple, Adjustable Output Voltage

The NCV6354, a synchronous buck converter, which is optimized to supply the different sub systems of portable applications powered by one cell Li-ion or three cell Alkaline/NiCd/NiMH batteries. The device is able to deliver up to 2 A on an external adjustable voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feedforward control is employed to deal with wide input voltage range. Synchronous rectification offers improved system efficiency. The NCV6354 is in a space saving, low profile 2.0x2.0x0.75 mm WDFN-8 package.

#### Features

- 2.3 V to 5.5 V Input Voltage Range
- External Adjustable Voltage
- Up to 2 A Output Current
- 3 MHz Switching Frequency
- Synchronous Rectification
- Enable Input
- Power Good Output
- Soft Start
- Over Current Protection
- Active Discharge when Disabled
- Thermal Shutdown Protection
- WDFN-8, 2x2 mm, 0.5 mm Pitch Package
- Maximum 0.8 mm Height for Super Thin Applications
- These are Pb-Free Devices

#### Typical Applications

- Cellular Phones, Smart Phones, and PDAs
- Portable Media Players
- Digital Still Cameras
- Wireless and DSL Modems
- USB Powered Devices
- Point of Load
- Game and Entertainment System



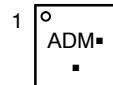
ON Semiconductor®

<http://onsemi.com>



WDFN8  
CASE 511BT

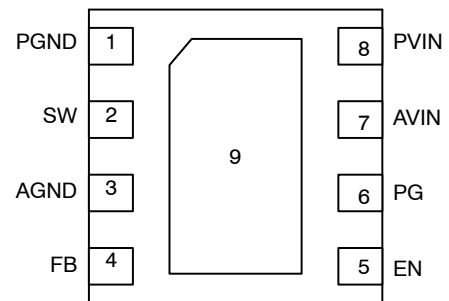
#### MARKING DIAGRAM



AD = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)

#### BLOCK DIAGRAM



(Top View)

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 14 of this data sheet.

# NCV6354

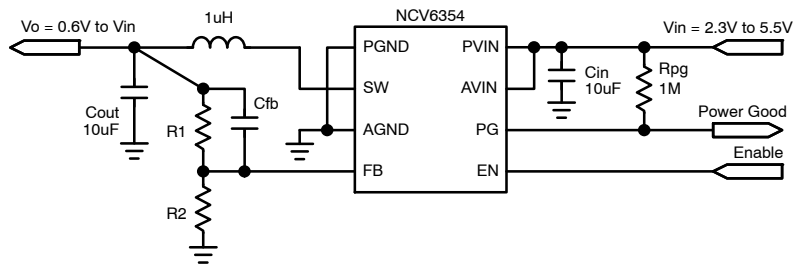
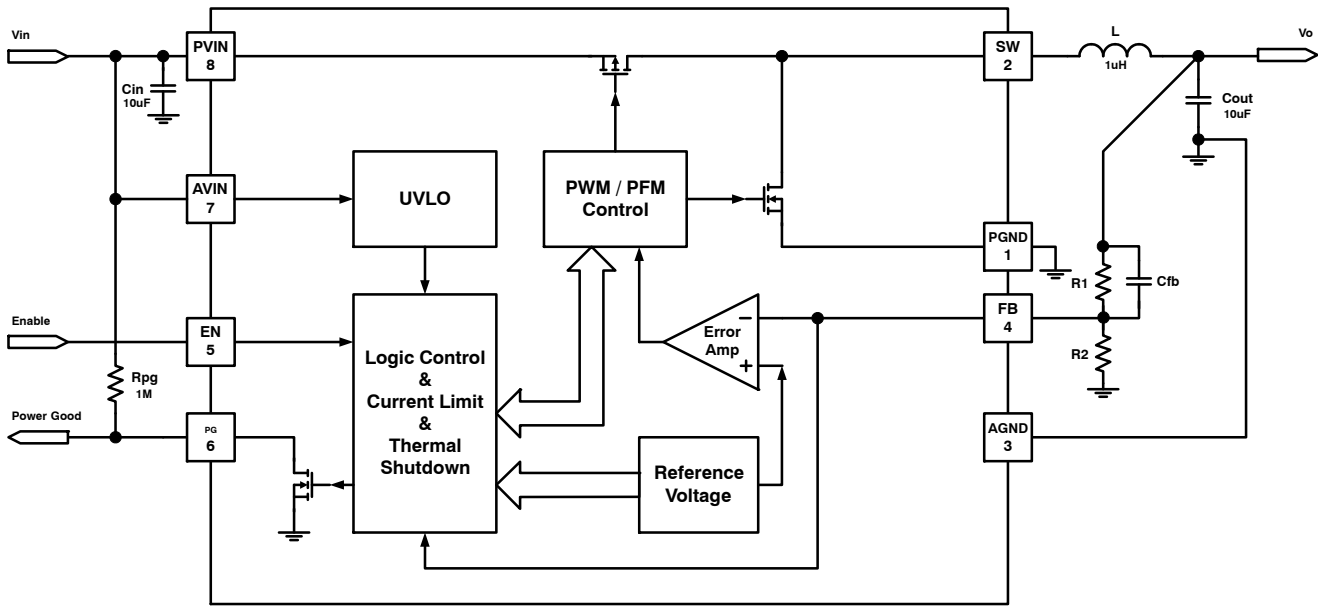


Figure 1. Typical Application Circuit

## PIN DESCRIPTION

Pin	Name	Type	Description
1	PGND	Power Ground	Power Ground for power, analog blocks. Must be connected to the system ground.
2	SW	Power Output	Switch Power pin connects power transistors to one end of the inductor.
3	AGND	Analog Ground	Analog Ground analog and digital blocks. Must be connected to the system ground.
4	FB	Analog Input	Feedback Voltage from the buck converter output. This is the input to the error amplifier. This pin is connected to the resistor divider network between the output and AGND.
5	EN	Digital Input	Enable of the IC. High level at this pin enables the device. Low level at this pin disables the device.
6	PG	Digital Output	PG pin is for NCV6354 with Power Good option. It is open drain output. Low level at this pin indicates the device is not in power good, while high impedance at this pin indicates the device is in power good.
7	AVIN	Analog Input	Analog Supply. This pin is the analog and the digital supply of the device. An optional 1 $\mu$ F or larger ceramic capacitor bypasses this input to the ground. This capacitor should be placed as close as possible to this input.
8	PVIN	Power Input	Power Supply Input. This pin is the power supply of the device. A 10 $\mu$ F or larger ceramic capacitor must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
9	PAD	Exposed Pad	Exposed Pad. Must be soldered to system ground to achieve power dissipation performances. This pin is internally unconnected

# NCV6354



**Figure 2. Functional Block Diagram.**

## MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Input Supply Voltage to GND	$V_{PVIN}, V_{AVIN}$	-0.3	7.0	V
Switch Node to GND	$V_{SW}$	-0.3	7.0	V
EN, PG to GND	$V_{EN}, V_{PG}$	-0.3	7.0	V
FB to GND	$V_{FB}$	-0.3	2.5	V
Human Body Model (HBM) ESD Rating (Note 1)	ESD HBM		2000	V
Machine Model (MM) ESD Rating (Note 1)	ESD MM		200	V
Latchup Current (Note 2)	$I_{LU}$	-100	100	mA
Operating Junction Temperature Range (Note 3)	$T_J$	-40	125	°C
Operating Ambient Temperature Range	$T_A$	-40	85	°C
Storage Temperature Range	$T_{STG}$	-55	150	°C
Thermal Resistance Junction-to-Top Case (Note 4)	$R_{\theta JC}$	12		°C/W
Thermal Resistance Junction-to-Board (Note 4)	$R_{\theta JB}$	30		°C/W
Thermal Resistance Junction-to-Ambient (Note 4)	$R_{\theta JA}$	62		°C/W
Power Dissipation (Note 5)	$P_D$	1.6		W
Moisture Sensitivity Level (Note 6)	MSL	1		-

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM)  $\pm 2.0$  kV per JEDEC standard: JESD22-A114.  
Machine Model (MM)  $\pm 200$  V per JEDEC standard: JESD22-A115.
- Latchup Current per JEDEC standard: JESD78 Class II.
- The thermal shutdown set to 160°C (typical) avoids potential irreversible damage on the device due to power dissipation.
- The thermal resistance values are dependent of the PCB heat dissipation. Board used to drive these data was an 80 x 50mm NCP6334EVB board. It is a multilayer board with 1-once internal power and ground planes and 2-once copper traces on top and bottom of the board. If the copper traces of top and bottom are 1-once too,  $R_{\theta JC} = 11^\circ\text{C/W}$ ,  $R_{\theta JB} = 30^\circ\text{C/W}$ , and  $R_{\theta JA} = 72^\circ\text{C/W}$ .
- The maximum power dissipation ( $P_D$ ) is dependent on input voltage, maximum output current and external components selected.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

# NCV6354

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $L = 1\ \mu\text{H}$ ,  $C = 10\ \mu\text{F}$ , typical values are referenced to  $T_J = 25^\circ\text{C}$ , Min and Max values are referenced to  $T_J$  up to  $125^\circ\text{C}$ , unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
-----------------	-----------------	--------	-----	-----	-----	------

### SUPPLY VOLTAGE

Input Voltage $V_{IN}$ Range	(Note 9)	$V_{IN}$	2.3	–	5.5	V
------------------------------	----------	----------	-----	---	-----	---

### SUPPLY CURRENT

$V_{IN}$ Quiescent Supply Current	EN high, no load	$I_Q$	–	5	–	mA
$V_{IN}$ Shutdown Current	EN low	$I_{SD}$	–	–	1	$\mu\text{A}$

### OUTPUT VOLTAGE

Output Voltage Range	(Note 7)	$V_{OUT}$	0.6	–	$V_{IN}$	V
FB Voltage		$V_{FB}$	594	600	606	mV
FB Voltage in Load Regulation	$V_{IN} = 3.6\text{ V}$ , $I_{OUT}$ from 200 mA to $I_{OUTMAX}$ . (Note 7)		–	–0.5	–	%/A
FB Voltage in Line Regulation	$I_{OUT} = 200\text{ mA}$ , $V_{IN}$ from $\text{MAX}(V_{NOM} + 0.5\text{ V}, 2.3\text{ V})$ to 5.5 V (Note 7)		–	0	–	%/V
Maximum Duty Cycle	(Note 7)	$D_{MAX}$	–	100	–	%

### OUTPUT CURRENT

Output Current Capability	(Note 7)	$I_{OUTMAX}$	2.0	–	–	A
Output Peak Current Limit		$I_{LIM}$	2.3	2.8	3.3	A

### VOLTAGE MONITOR

$V_{IN}$ UVLO Falling Threshold		$V_{INUV-}$	–	–	2.3	V
$V_{IN}$ UVLO Hysteresis		$V_{INHYS}$	60	–	200	mV
Power Good Low Threshold	$V_{OUT}$ falls down to cross the threshold (percentage of FB voltage)	$V_{PGL}$	87	90	92	%
Power Good Hysteresis	$V_{OUT}$ rises up to cross the threshold (percentage of Power Good Low Threshold ( $V_{PGL}$ ) voltage)	$V_{PGHYS}$	0	3	5	%
Power Good High Delay in Start Up	From EN rising edge to PG going high.	$T_{dPGH1}$	–	1.15	–	ms
Power Good Low Delay in Shut Down	From EN falling edge to PG going low. (Note 7)	$T_{dPGL1}$	–	8	–	$\mu\text{s}$
Power Good High Delay in Regulation	From $V_{FB}$ going higher than 95% nominal level to PG going high. Not for the first time in start up. (Note 7)	$T_{dPGH}$	–	5	–	$\mu\text{s}$
Power Good Low Delay in Regulation	From $V_{FB}$ going lower than 90% nominal level to PG going low. (Note 7)	$T_{dPGL}$	–	8	–	$\mu\text{s}$
Power Good Pin Low Voltage	Voltage at PG pin with 5mA sink current	$V_{PG\_L}$	–	–	0.3	V
Power Good Pin Leakage Current	3.6 V at PG pin when power good valid	$PG\_LK$	–	–	100	nA

### INTEGRATED MOSFETS

High-Side MOSFET ON Resistance	$V_{IN} = 3.6\text{ V}$ (Note 8) $V_{IN} = 5\text{ V}$ (Note 8)	$R_{ON\_H}$	–	140 130	200 –	$\text{m}\Omega$
Low-Side MOSFET ON Resistance	$V_{IN} = 3.6\text{ V}$ (Note 8) $V_{IN} = 5\text{ V}$ (Note 8)	$R_{ON\_L}$	–	110 100	140 –	$\text{m}\Omega$

### SWITCHING FREQUENCY

Operation Frequency		FSW	2.7	3.0	3.3	MHz
---------------------	--	-----	-----	-----	-----	-----

7. Guaranteed by design, not tested in production.

8. Maximum value applies for  $T_J = 85^\circ\text{C}$ .

9. Operation above 5.5 V input voltage for extended periods may affect device reliability.

# NCV6354

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $L = 1\text{ }\mu\text{H}$ ,  $C = 10\text{ }\mu\text{F}$ , typical values are referenced to  $T_J = 25^\circ\text{C}$ , Min and Max values are referenced to  $T_J$  up to  $125^\circ\text{C}$ . unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
-----------------	-----------------	--------	-----	-----	-----	------

### SOFT START

Soft-Start Time	Time from EN to 90% of output voltage target	TSS	–	0.4	1	ms
-----------------	--	-----	---	-----	---	----

### CONTROL LOGIC

EN Input High Voltage		VEN_H	1.1	–	–	V
EN Input Low Voltage		VEN_L	–	–	0.4	V
EN Input Hysteresis		VEN_HYS	–	270	–	mV
Enable Input Bias Current		IEN_BIAS		0.1	1	$\mu\text{A}$

### OUTPUT ACTIVE DISCHARGE

Internal Output Discharge Resistance	from SW to PGND	R_DIS	75	500	700	$\Omega$
--------------------------------------	-----------------	-------	----	-----	-----	----------

### THERMAL SHUTDOWN

Thermal Shutdown Threshold		TSD	–	160	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis		TSD_HYS	–	25	–	$^\circ\text{C}$

7. Guaranteed by design, not tested in production.
8. Maximum value applies for  $T_J = 85^\circ\text{C}$ .
9. Operation above 5.5 V input voltage for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

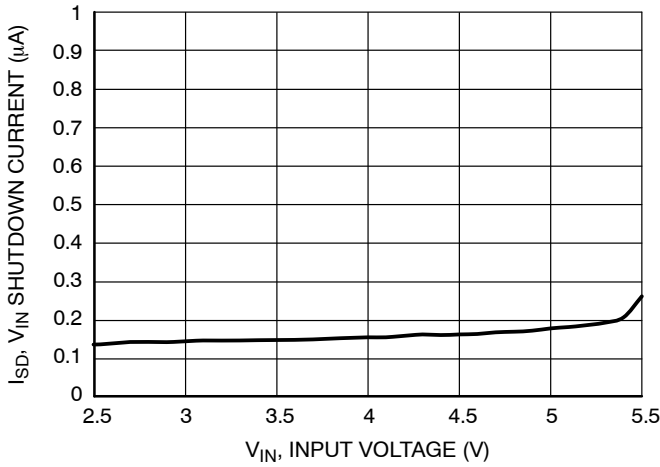


Figure 3. Standby Current vs. Input Voltage  
(EN = Low, T<sub>A</sub> = 25°C)

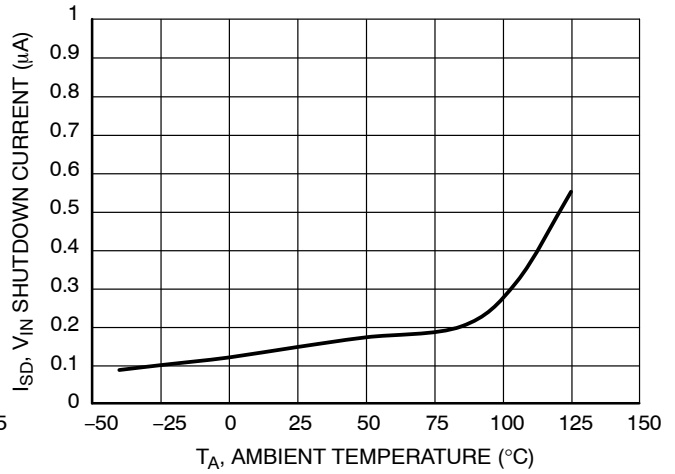


Figure 4. Standby Current vs. Temperature  
(EN = Low, V<sub>IN</sub> = 3.6 V)

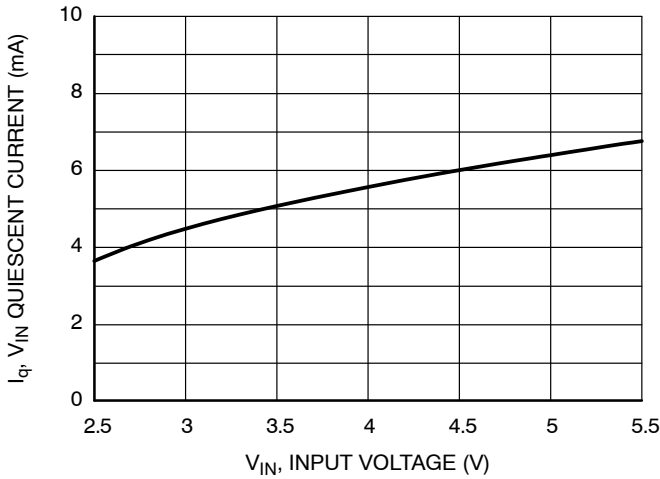


Figure 5. Quiescent Current vs. Input Voltage  
(EN = High, Open Loop, V<sub>OUT</sub> = 1.8V, T<sub>A</sub> = 25°C)

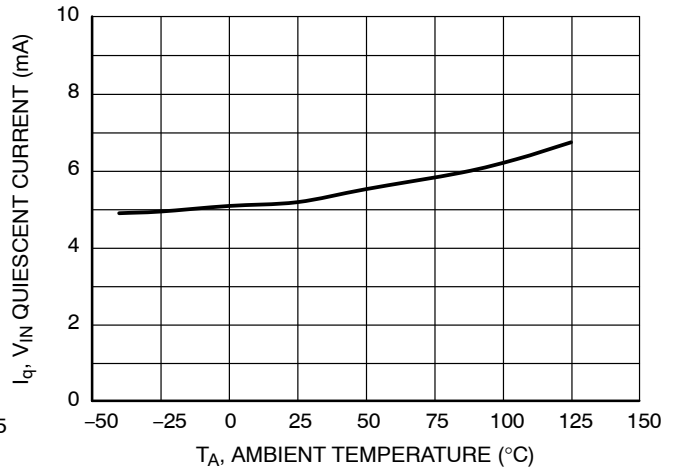


Figure 6. Quiescent Current vs. Temperature  
(EN = High, Open Loop, V<sub>OUT</sub> = 1.8 V, V<sub>IN</sub> = 3.6 V)

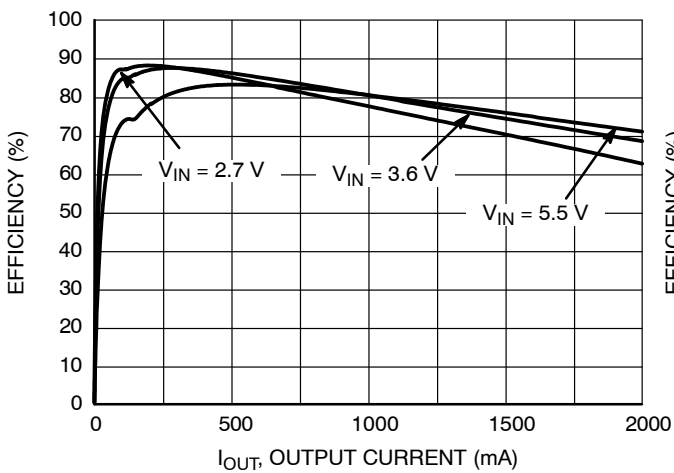


Figure 7. Efficiency vs. Output Current and Input Voltage (V<sub>OUT</sub> = 1.05 V, T<sub>A</sub> = 25°C)

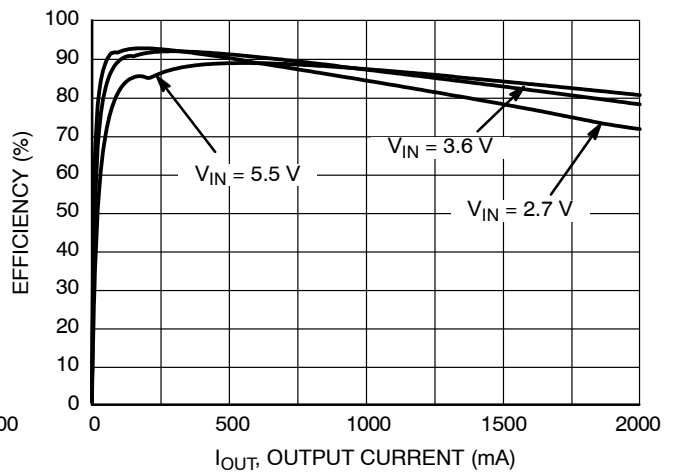


Figure 8. Efficiency vs. Output Current and Input Voltage (V<sub>OUT</sub> = 1.8 V, T<sub>A</sub> = 25°C)

TYPICAL OPERATING CHARACTERISTICS

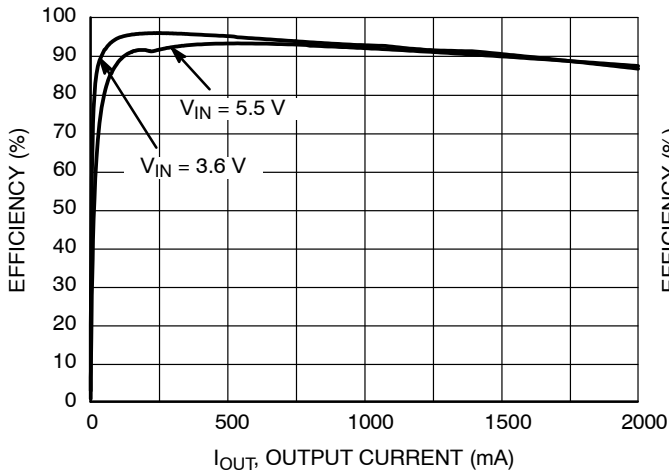


Figure 9. Efficiency vs. Output Current and Input Voltage ( $V_{OUT} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

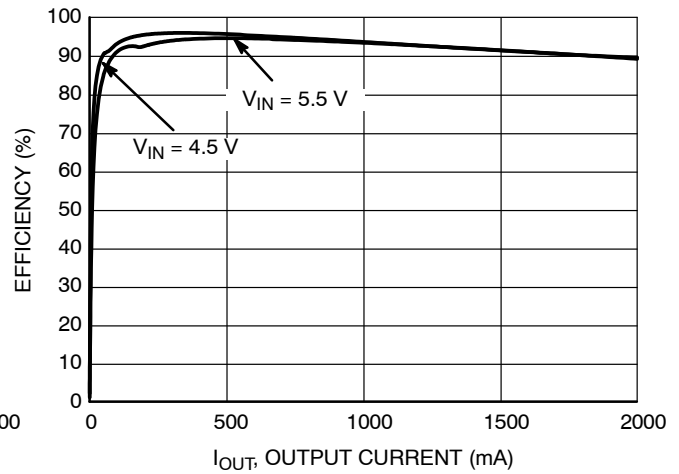


Figure 10. Efficiency vs. Output Current and Input Voltage ( $V_{OUT} = 4\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

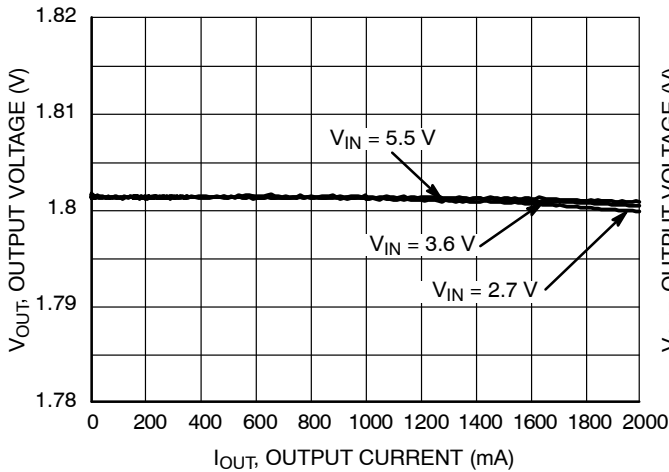


Figure 11. Load Regulation vs. Output Current and Input Voltage ( $V_{OUT} = 1.8\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

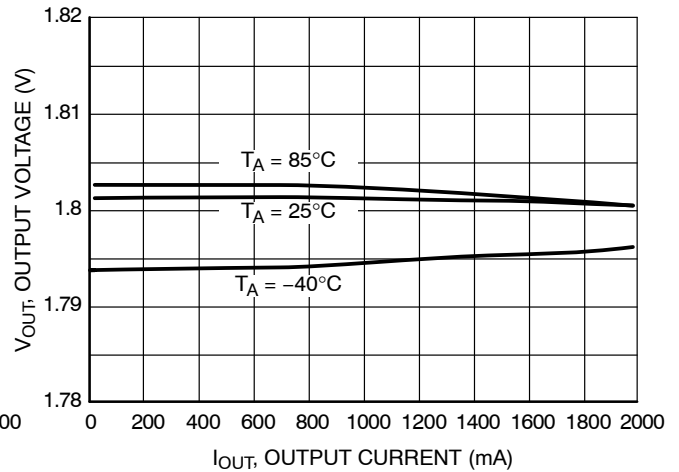


Figure 12. Load Regulation vs. Output Current and Temperature ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ )

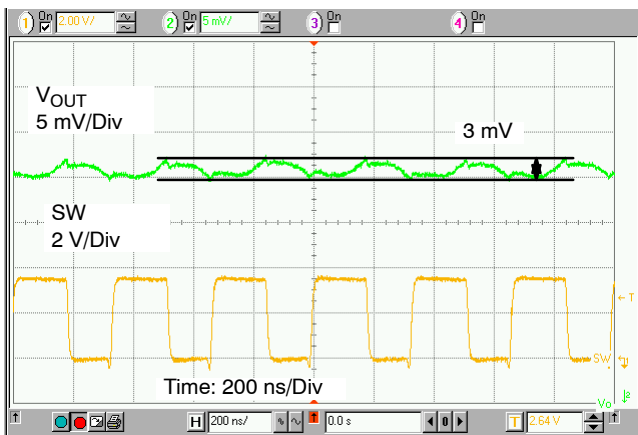


Figure 13. Output Ripple Voltage ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ )

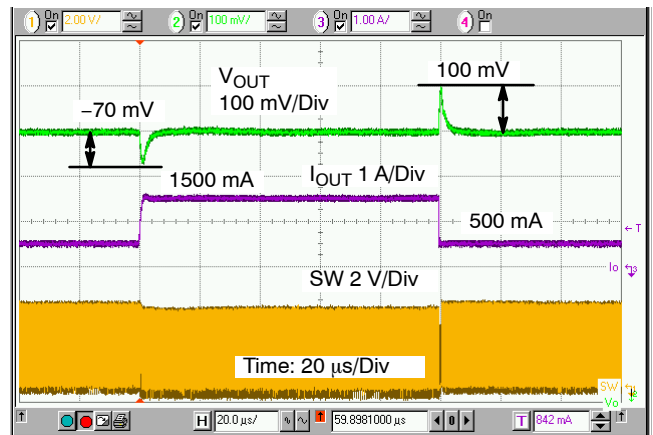


Figure 14. Load Transient Response ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$  to  $1500\text{ mA}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ )



TYPICAL OPERATING CHARACTERISTICS

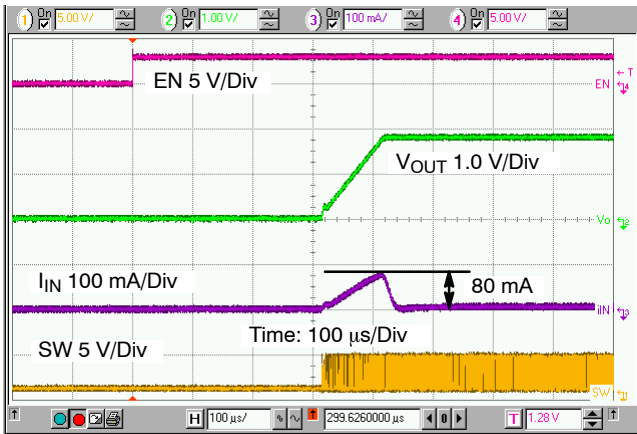


Figure 15. Power Up Sequence and Inrush Current in Input ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 0\text{ A}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ )

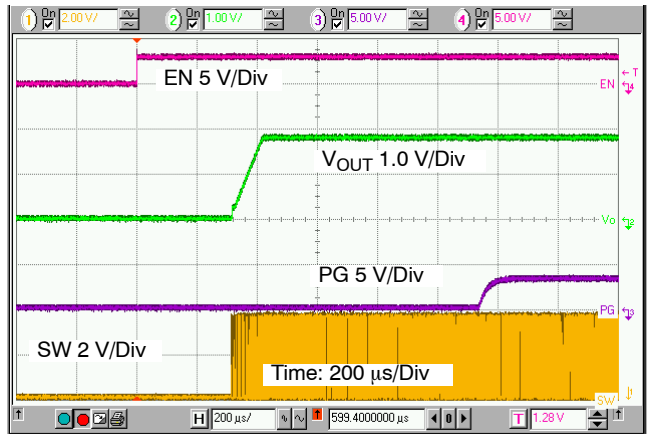


Figure 16. Power Up Sequence and Power Good ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 0\text{ A}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ )

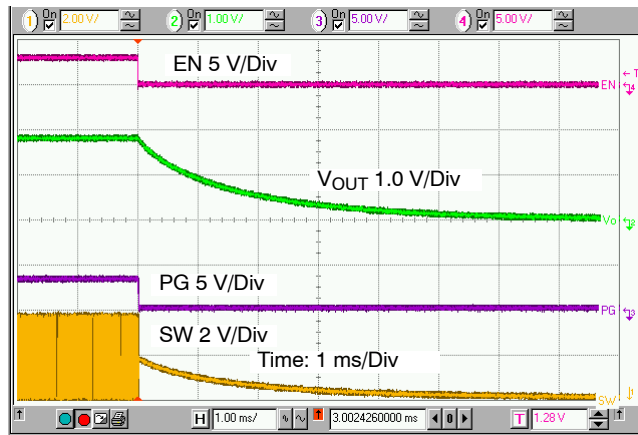


Figure 17. Power Down Sequence and Active Output Discharge ( $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 0\text{ A}$ ,  $L = 1.0\text{ }\mu\text{H}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ )

DETAILED DESCRIPTION

**General**

The NCV6354, a synchronous buck converter, which is optimized to supply the different sub systems of portable applications powered by one cell Li-ion or three cell Alkaline/NiCd/NiMH batteries. The device is able to deliver up to 2 A on an external adjustable voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feedforward control is employed to deal with wide input voltage range. Synchronous rectification offers improved system efficiency.

**PWM Operation**

The inductor current is continuous and the device operates in fixed switching frequency, which has a typical value of 3 MHz. The output voltage is regulated by on-time pulse width modulation of the internal P-MOSFET. The internal N-MOSFET operates as synchronous rectifier and its turn-on signal is complimentary to that of the P-MOSFET.

**Undervoltage Lockout**

The input voltage  $V_{IN}$  must reach or exceed 2.4 V (typical) before the NCV6354 enables the converter output to begin the start up sequence. The UVLO threshold hysteresis is typically 100 mV.

**Enable**

The NCV6354 has an enable logic input pin EN. A high level (above 1.1 V) on this pin enables the device to active mode. A low level (below 0.4 V) on this pin disables the

device and makes the device in shutdown mode. There is an internal filter with 5  $\mu$ s time constant. The EN pin is pulled down by an internal 10 nA sink current source. In most of applications, the EN signal can be programmed independently to VIN power sequence.

**Power Good Output**

For NCV6354 with power good output, the device monitors the output voltage and provides a power good output signal at the PG pin. This pin is an open-drain output pin. To indicate the output of the converter is established, a power good signal is available. The power good signal is low when EN is high but the output voltage has not been established. Once the output voltage of the converter drops out below 90% of its regulation during operation, the power good signal is pulled low and indicates a power failure. A 5% hysteresis is required on power good comparator before signal going high again.

**Soft Start**

A soft start limits inrush current when the converter is enabled. After a minimum 300  $\mu$ s delay time following the enable signal, the output voltage starts to ramp up in 100  $\mu$ s (for external adjustable voltage devices) or with a typical 10 V/ms slew rate (for fixed voltage devices).

**Active Output Discharge**

An output discharge operation is active in when EN is low. A discharge resistor (500  $\Omega$  typical) is enabled in this condition to discharge the output capacitor through SW pin.

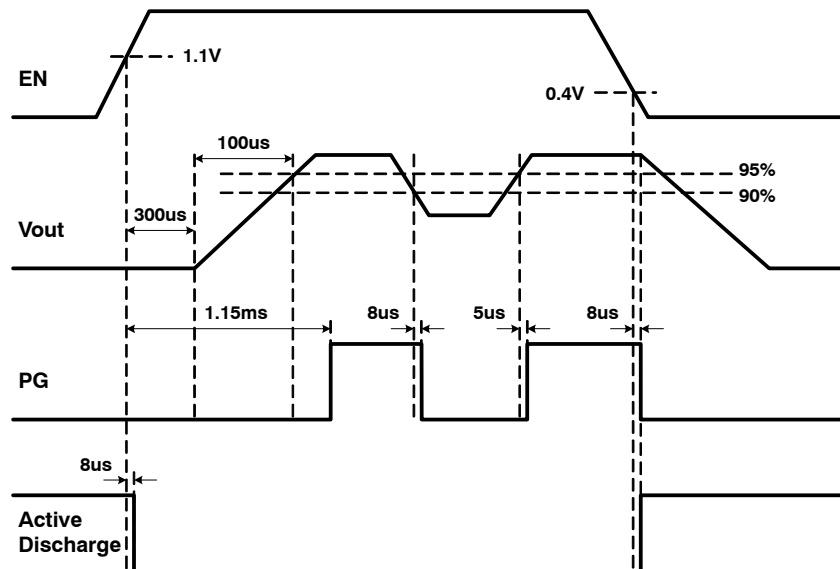


Figure 18. Power Good and Active Discharge Timing Diagram

**Cycle-by-Cycle Current Limitation**

The NCV6354 protects the device from over current with a fixed cycle-by-cycle current limitation. The typical peak current limit ILMT is 2.8 A. If inductor current exceeds the

current limit threshold, the P-MOSFET will be turned off cycle-by-cycle. The maximum output current can be calculated by

$$I_{MAX} = I_{LMT} - \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot V_{IN} \cdot f_{SW} \cdot L} \quad (\text{eq. 1})$$

where  $V_{IN}$  is input supply voltage,  $V_{OUT}$  is output voltage,  $L$  is inductance of the filter inductor, and  $f_{SW}$  is 3 MHz normal switching frequency.

**Thermal Shutdown**

The NCV6354 has a thermal shutdown protection to protect the device from overheating when the die temperature exceeds 160°C. Once the thermal protection is triggered, the fault state can be ended by re-applying  $V_{IN}$  and/or EN when the temperature drops down below 125°C.

**APPLICATION INFORMATION**

**Output Filter Design Considerations**

The output filter introduces a double pole in the system at a frequency of

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \quad (\text{eq. 2})$$

The internal compensation network design of the NCV6354 is optimized for the typical output filter comprised of a 1.0  $\mu\text{H}$  inductor and a 10  $\mu\text{F}$  ceramic output capacitor, which has a double pole frequency at about 50 kHz. Other possible output filter combinations may have a double pole around 50 kHz to have optimum operation with the typical feedback network. Normal selection range of the inductor is from 0.47  $\mu\text{H}$  to 4.7  $\mu\text{H}$ , and normal selection range of the output capacitor is from 4.7  $\mu\text{F}$  to 22  $\mu\text{F}$ .

**Inductor Selection**

The inductance of the inductor is determined by given peak-to-peak ripple current  $I_{L\_PP}$  of approximately 20% to

50% of the maximum output current  $I_{OUT\_MAX}$  for a trade-off between transient response and output ripple. The inductance corresponding to the given current ripple is

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}} \quad (\text{eq. 3})$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2} \quad (\text{eq. 4})$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table 1 shows some recommended inductors for high power applications and Table 2 shows some recommended inductors for low power applications.

**Table 1. LIST OF RECOMMENDED INDUCTORS FOR HIGH POWER APPLICATIONS**

Manufacturer	Part Number	Case Size (mm)	L ( $\mu\text{H}$ )	Rated Current (mA) (Inductance Drop)	Structure
MURATA	LQH44PN2R2MP0	4.0 x 4.0 x 1.8	2.2	2500 (-30%)	Wire Wound
MURATA	LQH44PN1R0NP0	4.0 x 4.0 x 1.8	1.0	2950 (-30%)	Wire Wound
MURATA	LQH32PNR47NNP0	3.0 x 2.5 x 1.7	0.47	3400 (-30%)	Wire Wound

**Table 2. LIST OF RECOMMENDED INDUCTORS FOR LOW POWER APPLICATIONS**

Manufacturer	Part Number	Case Size (mm)	L ( $\mu\text{H}$ )	Rated Current (mA) (Inductance Drop)	Structure
MURATA	LQH44PN2R2MJ0	4.0 x 4.0 x 1.1	2.2	1320 (-30%)	Wire Wound
MURATA	LQH44PN1R0NJ0	4.0 x 4.0 x 1.1	1.0	2000 (-30%)	Wire Wound
TDK	VLS201612ET-2R2	2.0 x 1.6 x 1.2	2.2	1150 (-30%)	Wire Wound
TDK	VLS201612ET-1R0	2.0 x 1.6 x 1.2	1.0	1650 (-30%)	Wire Wound

**Output Capacitor Selection**

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For a given peak-to-peak ripple current  $I_{L\_PP}$  in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as below.

$$V_{OUT\_PP} = V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)} \quad (\text{eq. 5})$$

where  $V_{OUT\_PP(C)}$  is a ripple component by an equivalent total capacitance of the output capacitors,  $V_{OUT\_PP(ESR)}$  is a ripple component by an equivalent ESR of the output capacitors, and  $V_{OUT\_PP(ESL)}$  is a ripple component by an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}} \quad (\text{eq. 6})$$

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \cdot ESR \quad (\text{eq. 7})$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad (\text{eq. 8})$$

and the peak-to-peak ripple current is

$$I_{L\_PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L} \quad (\text{eq. 9})$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is  $V_{OUT\_PP(C)}$ . So that the minimum output capacitance can be calculated regarding to a given output ripple requirement  $V_{OUT\_PP}$  in PWM operation mode.

$$C_{MIN} = \frac{I_{L\_PP}}{8 \cdot V_{OUT\_PP} \cdot f_{SW}} \quad (\text{eq. 10})$$

### Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage

ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding to the input ripple voltage  $V_{IN\_PP}$  is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \cdot (D - D^2)}{V_{IN\_PP} \cdot f_{SW}} \quad (\text{eq. 11})$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \quad (\text{eq. 12})$$

In addition, the input capacitor needs to be able to absorb the input current, which has a RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \cdot \sqrt{D - D^2} \quad (\text{eq. 13})$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least a 4.7  $\mu$ F capacitor is required. The input capacitor should be located as close as possible to the IC on PCB.

**Table 3. LIST OF RECOMMENDED INPUT CAPACITORS AND OUTPUT CAPACITORS**

Manufacturer	Part Number	Case Size	Height Max (mm)	C ( $\mu$ F)	Rated Voltage (V)	Structure
MURATA	GRM21BR60J226ME39, X5R	0805	1.4	22	6.3	MLCC
TDK	C2012X5R0J226M, X5R	0805	1.25	22	6.3	MLCC
MURATA	GRM21BR61A106KE19, X5R	0805	1.35	10	10	MLCC
TDK	C2012X5R1A106M, X5R	0805	1.25	10	10	MLCC
MURATA	GRM188R60J106ME47, X5R	0603	0.9	10	6.3	MLCC
TDK	C1608X5R0J106M, X5R	0603	0.8	10	6.3	MLCC
MURATA	GRM188R60J475KE19, X5R	0603	0.87	4.7	6.3	MLCC

### Design of Feedback Network

For NCV6354 devices with an external adjustable output voltage, the output voltage is programmed by an external resistor divider connected from  $V_{OUT}$  to FB and then to AGND, as shown in the typical application schematic Figure 1a. The programmed output voltage is

$$V_{OUT} = V_{FB} \cdot \left( 1 + \frac{R_1}{R_2} \right) \quad (\text{eq. 14})$$

where  $V_{FB}$  is equal to the internal reference voltage 0.6 V,  $R_1$  is the resistance from  $V_{OUT}$  to FB, which has a normal value range from 50 k $\Omega$  to 1 M $\Omega$  and a typical value of

220 k $\Omega$  for applications with the typical output filter.  $R_2$  is the resistance from FB to AGND, which is used to program the output voltage according to Equation 14 once the value of  $R_1$  has been selected. An capacitor  $C_{fb}$  needs to be employed between the  $V_{OUT}$  and FB in order to provide feedforward function to achieve optimum transient response. Normal value range of  $C_{fb}$  is from 0 to 100pF, and a typical value is 15 pF for applications with the typical output filter and  $R_1 = 220$  k $\Omega$ .

Table 4 provides reference values of  $R_1$  and  $C_{fb}$  in case of different output filter combinations. The final design may need to be fine tuned regarding to application specifications.

# NCV6354

**Table 4. REFERENCE VALUES OF FEEDBACK NETWORKS ( $R_1$  AND  $C_{fb}$ ) FOR OUTPUT FILTER COMBINATIONS (L AND C)**

$R_1$ (k $\Omega$ )		$L$ ( $\mu$ H)					
$C_{fb}$ (pF)		0.47	0.68	1	2.2	3.3	4.7
$C$ ( $\mu$ F)	4.7	220	220	220	220	330	330
		3	5	8	15	15	22
	10	220	220	220	220	330	330
		8	10	15	27	27	39
	22	220	220	220	220	330	330
		15	22	27	39	47	56

LAYOUT CONSIDERATIONS

**Electrical Layout Considerations**

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated ground planes for PGND and AGND and connect the two planes at one point. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense and feedback network, and make it surrounded by a ground plane.

**Thermal Layout Considerations**

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pad must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and/or underneath the exposed pad to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

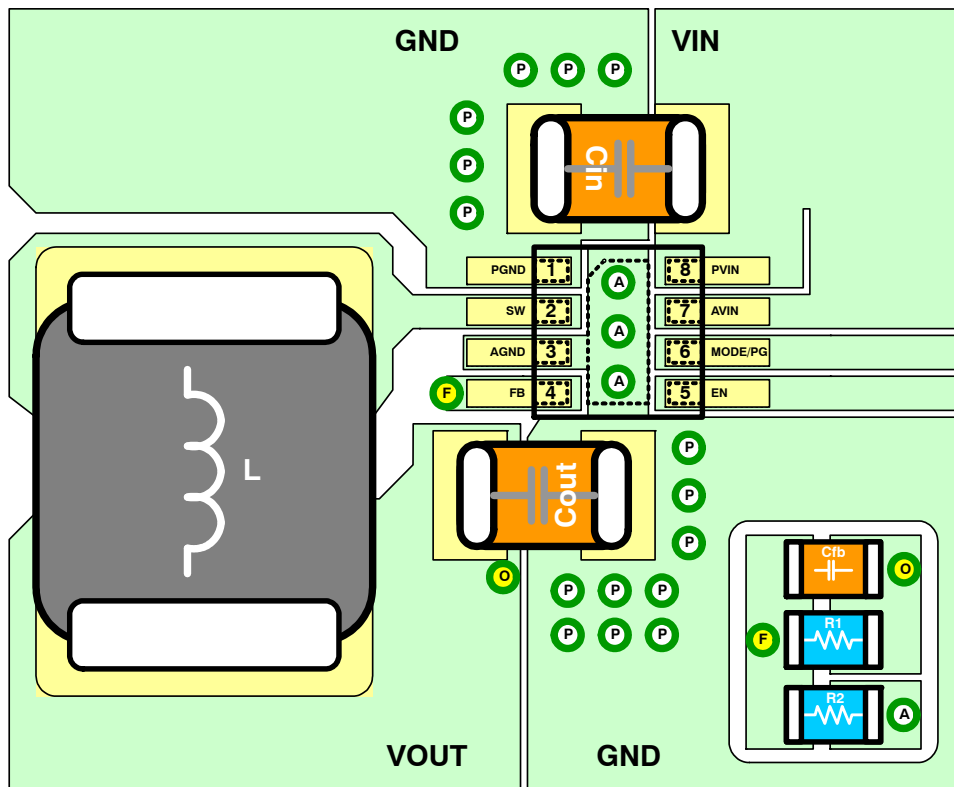


Figure 19. Recommended PCB Layout for Application Boards

# NCV6354

## ORDERING INFORMATION

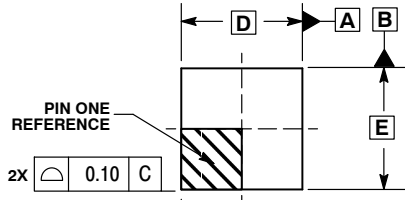
Device	Marking	Package	Shipping <sup>†</sup>
NCV6354BMTAATBG	AD	WDFN8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

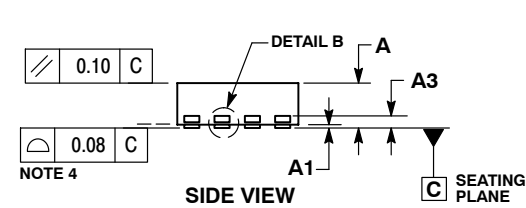
# NCV6354

## PACKAGE DIMENSIONS

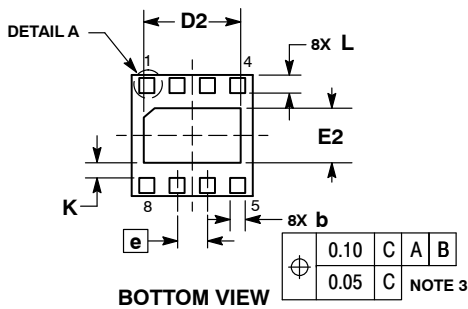
WDFN8 2x2, 0.5P  
CASE 511BT  
ISSUE O



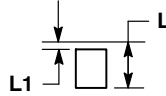
TOP VIEW



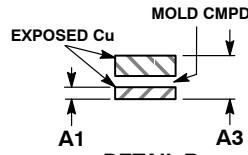
SIDE VIEW



BOTTOM VIEW



DETAIL A



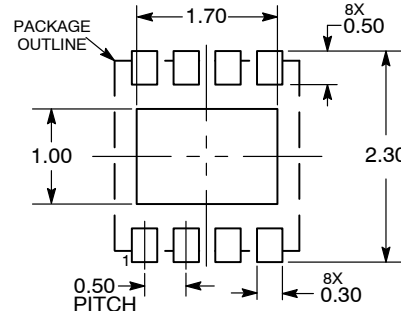
DETAIL B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.50	1.70
E	2.00	BSC
E2	0.80	1.00
e	0.50	BSC
K	0.25	REF
L	0.20	0.40
L1	---	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative