2:1, DIFFERENTIAL-TO-LVPECL MULTIPLEXER

ICS85301

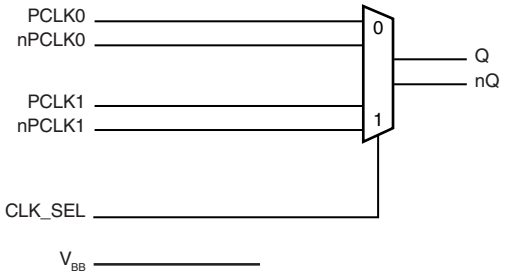
General Description

The ICS85301 is a high performance 2:1 Differential-to-LVPECL Multiplexer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS85301 can also perform differential translation because the differential inputs accept LVPECL, CML as well as LVDS levels. The ICS85301 is packaged in a small 3mm x 3mm 16 VFQFN package, making it ideal for use on space constrained boards.

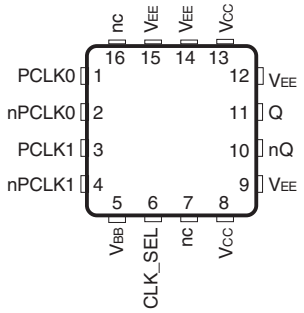
Features

- 2:1 LVPECL MUX
- One LVPECL output
- Two differential clock inputs can accept: LVPECL, LVDS, CML
- Maximum input/output frequency: 3GHz
- Translates LVCMOS/LVTTL input signals to LVPECL levels by using a resistor bias network on nPCLK0, nPCLK0
- Propagation delay: 490ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Additive phase jitter, RMS: 0.009ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

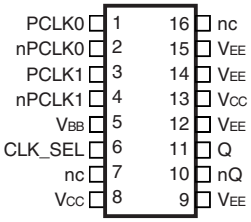
Block Diagram



Pin Assignment



ICS85301
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View



ICS85301
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
5	V_{BB}	Output		Bias voltage.
7, 16	nc	Unused		No connect.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS / LVTTL interface levels.
8, 13	V_{CC}	Power		Positive supply pins.
9, 12, 14, 15	V_{EE}	Power		Negative supply pins.
10, 11	nQ, Q	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			1		pF
R_{PULLUP}	Input Pullup Resistor			37		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			37		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Input	Input Selected
CLK_SEL	**PCLK**
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
16 VFQFN	51.5°C/W (0 lfpm)
16 TSSOP	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				26	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				24	mA

Table 4C. LVCMOS / LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

NOTE: Outputs terminated with 50Ω to V_{CC}/2. See Parameter Measurement Information, "Output Load Test Circuit".

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0, PCLK1, nPCLK1	V_{CC} = V_{IN} = 3.465			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		3.3	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} - 1.125		V_{CC} - 0.93	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} - 1.895		V_{CC} - 1.62	V
V_{swing}	Peak-to-Peak Output Voltage Swing			0.495		0.975	V
V_{BB}	Bias Voltage			1.695		2.145	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V. .

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0, PCLK1, nPCLK1	$V_{CC} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			150		1200	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		2.5	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} - 1.125		V_{CC} - 0.93	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} - 1.895		V_{CC} - 1.62	V
V_{swing}	Peak-to-Peak Output Voltage Swing			0.495		0.975	V
V_{BB}	Bias Voltage			0.935		1.305	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V. .

TABLE 5A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1		240		490	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				150	ps
*t*sk(i)	Input Skew				25	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	622MHz (Integration Range: 12kHz - 20MHz)		0.009		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		48		52	%
MUX_{ISOL}	MUX Isolation	f = 622MHz		-55		dBm

All parameters measured at f ≤ 1.7GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

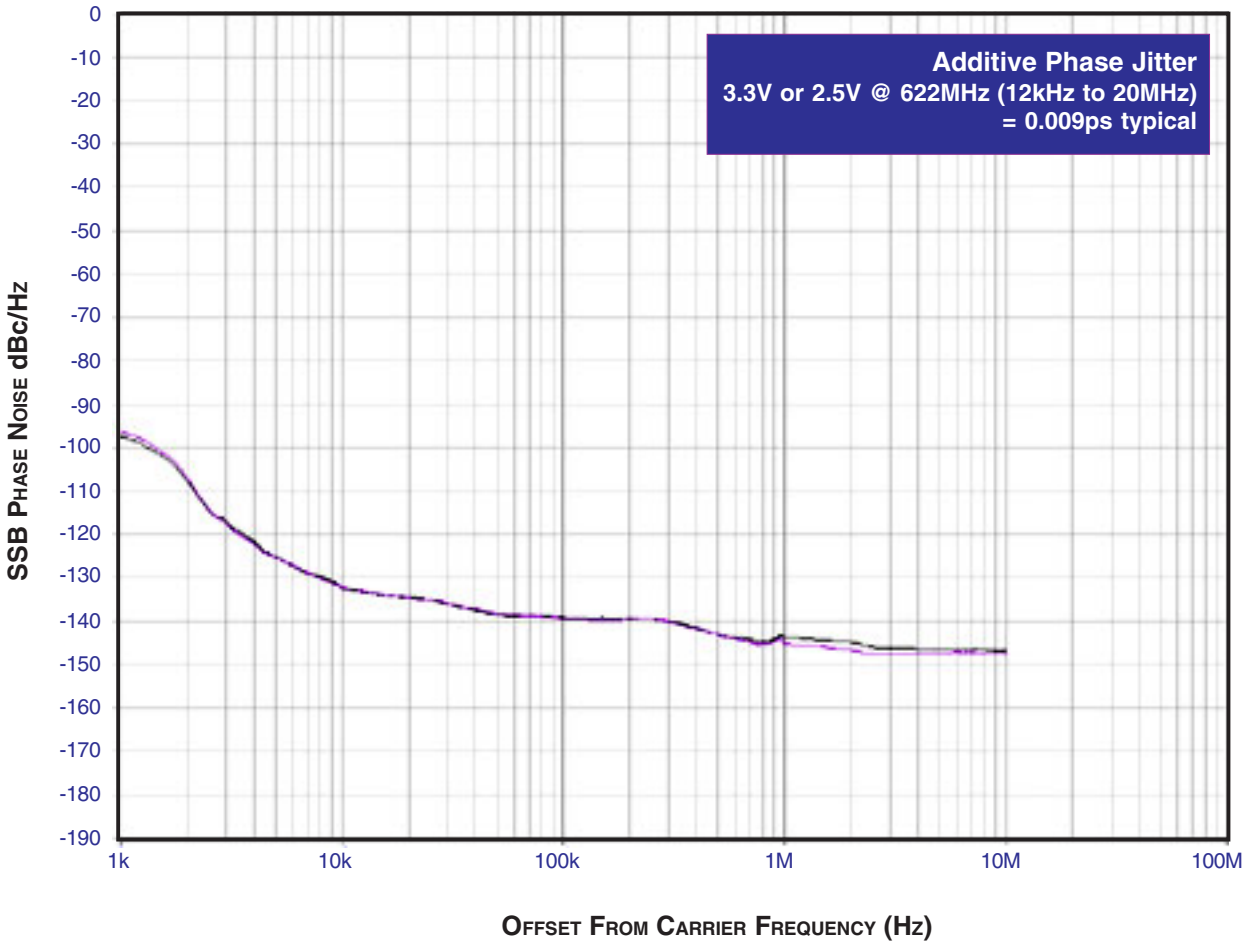
TABLE 5B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1		240		490	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				150	ps
*t*sk(i)	Input Skew				25	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	622MHz (Integration Range: 12kHz - 20MHz)		0.009		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		47		53	%
MUX_{ISOL}	MUX Isolation	f = 622MHz		-55		dBm

For notes, see Table 5A above.

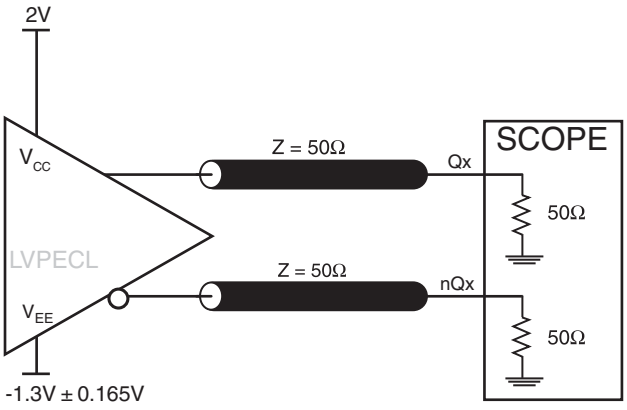
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

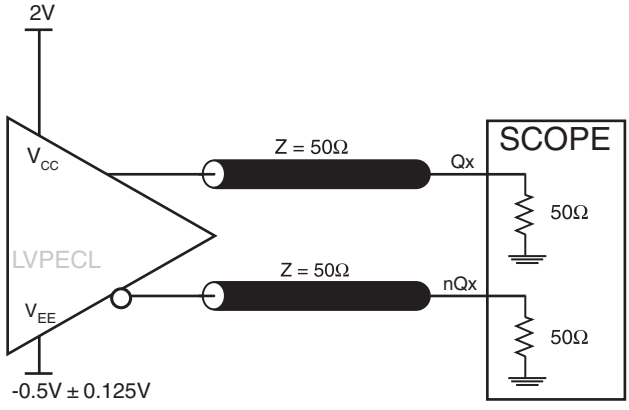


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

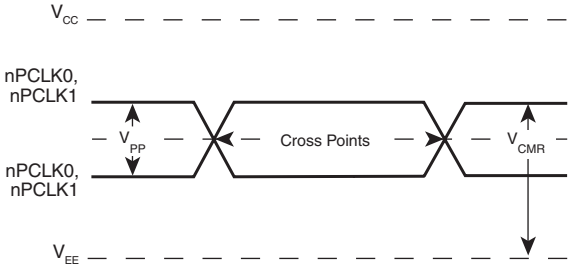
PARAMETER MEASUREMENT INFORMATION



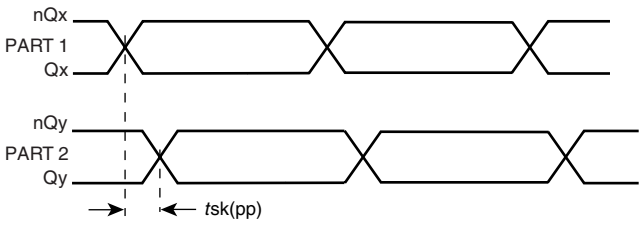
3.3V OUTPUT LOAD AC TEST CIRCUIT



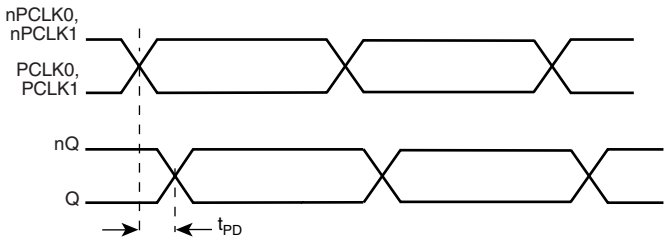
2.5V OUTPUT LOAD AC TEST CIRCUIT



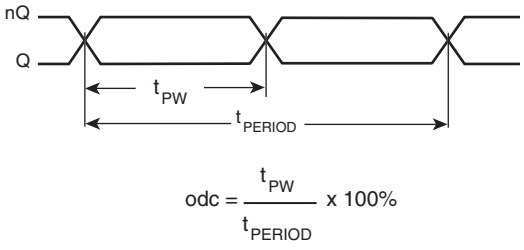
DIFFERENTIAL INPUT LEVEL



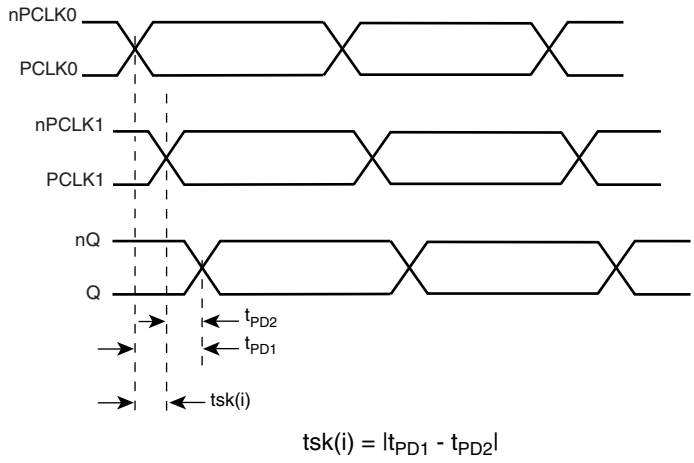
PART-TO-PART SKEW



PROPAGATION DELAY

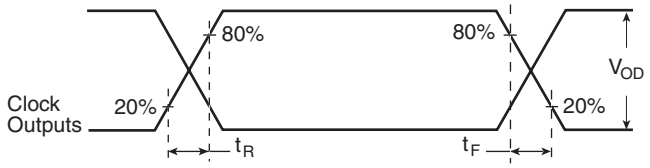


OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$tsk(i) = |t_{PD1} - t_{PD2}|$

INPUT SKEW



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1A shows an example of the differential input that can be wired to accept single ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

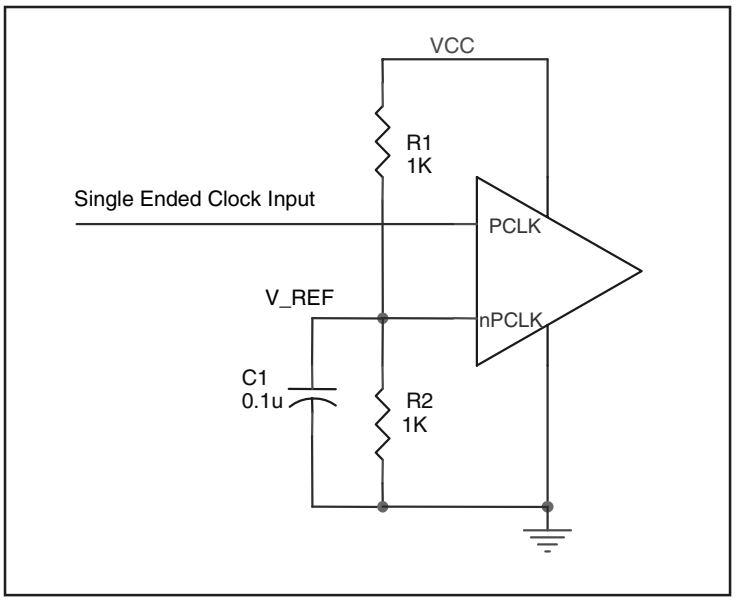


FIGURE 1A. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVPECL LEVELS

Figure 1B shows an example of the differential input that can be wired to accept single ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input.

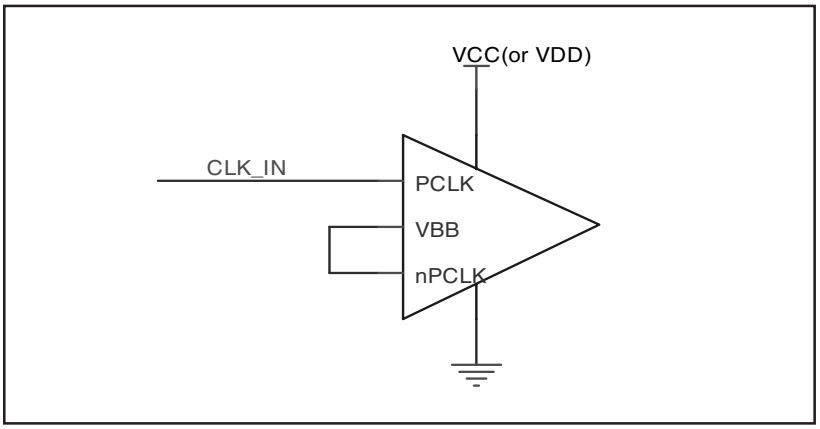


FIGURE 1B. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

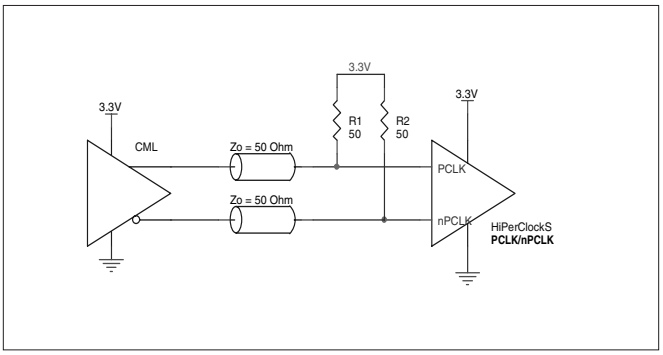


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

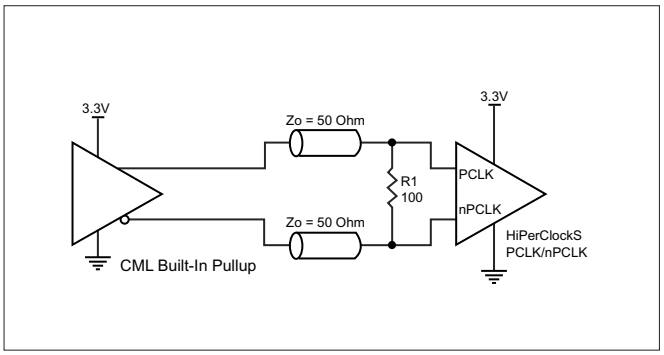


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

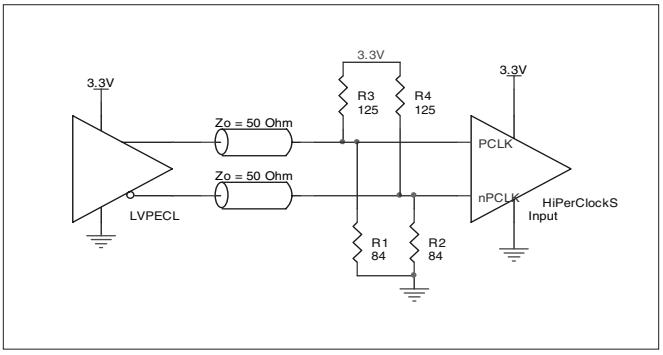


Figure 2C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

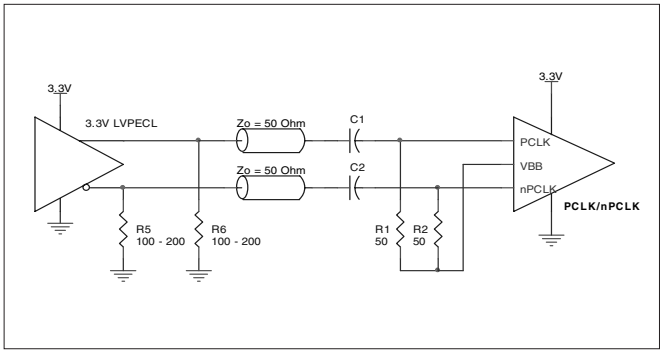


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

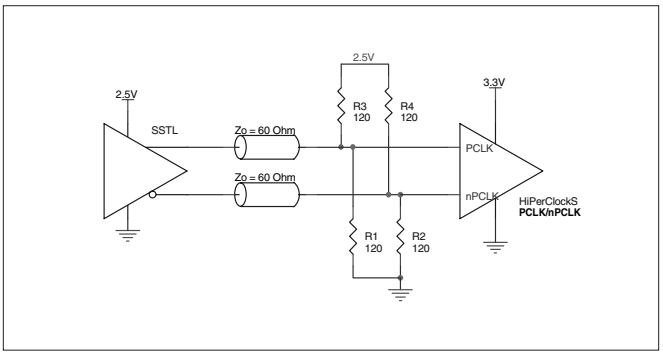


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

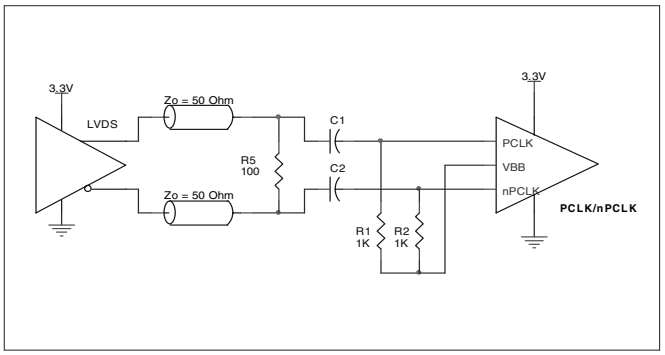


Figure 2F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Input:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

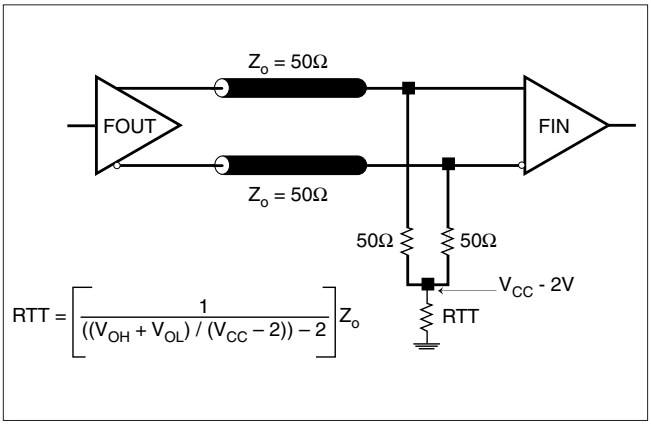


Figure 3A. LVPECL Output Termination

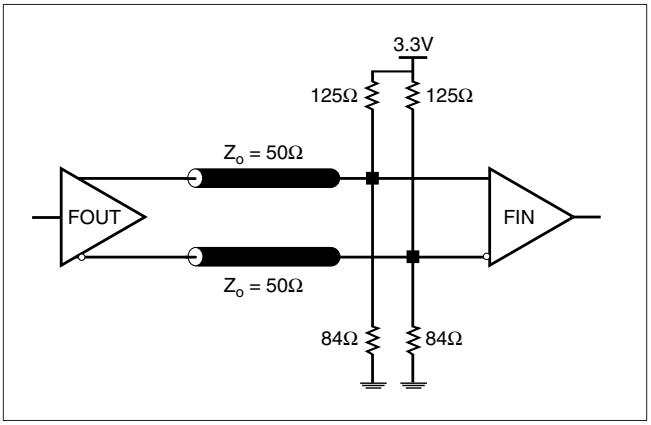


Figure 3B. LVPECL Output Termination

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

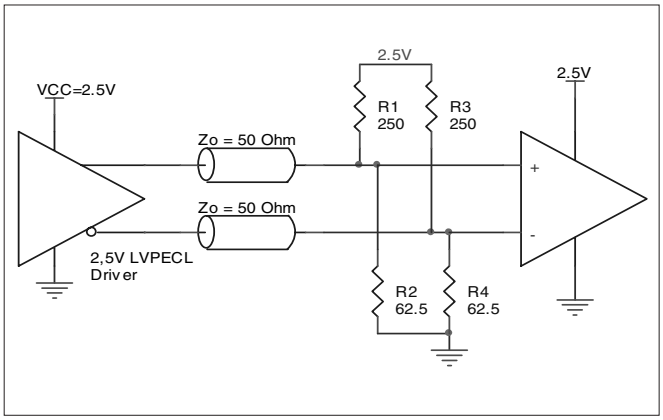


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

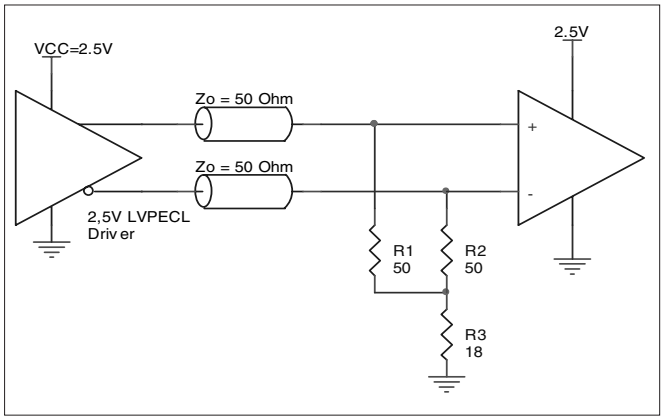


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

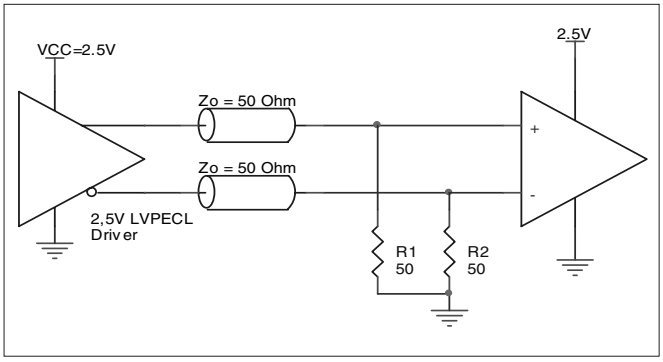


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

THERMAL RELEASE PATH

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 5.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

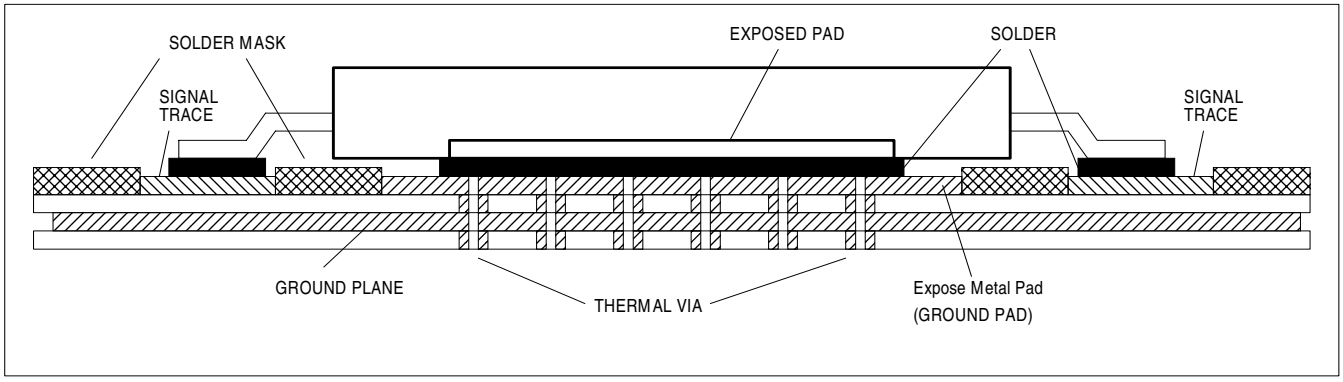


FIGURE 5. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE

Application Schematic Example

Figure 6 shows an example of ICS85301 application schematic. This device can accept different types of input signal. In this example, the input is driven by a LVDS driver. The decoupling capacitor should be located as close as possible to the power pin.

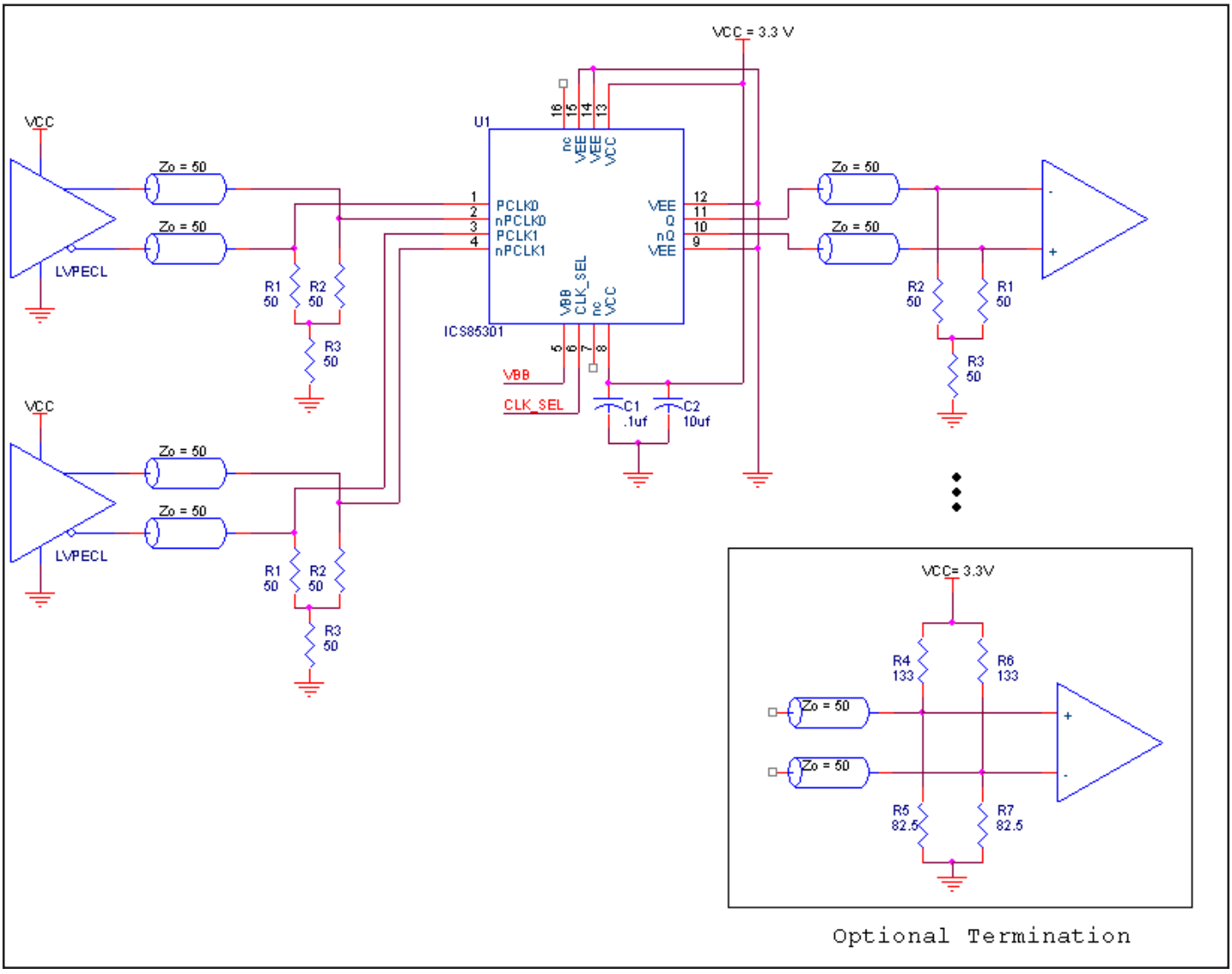


Figure 6. ICS85301 Application Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85301.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85301 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 26mA = **90.09mW**
- Power (outputs)$_{MAX}$ = **32.2mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465, with all outputs switching) = 90.09mW + 32.2mW = **122.3mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 0 linear feet per minute and a multi-layer board, the appropriate value is 51.5°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.122W * 51.5°C/W = 91.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

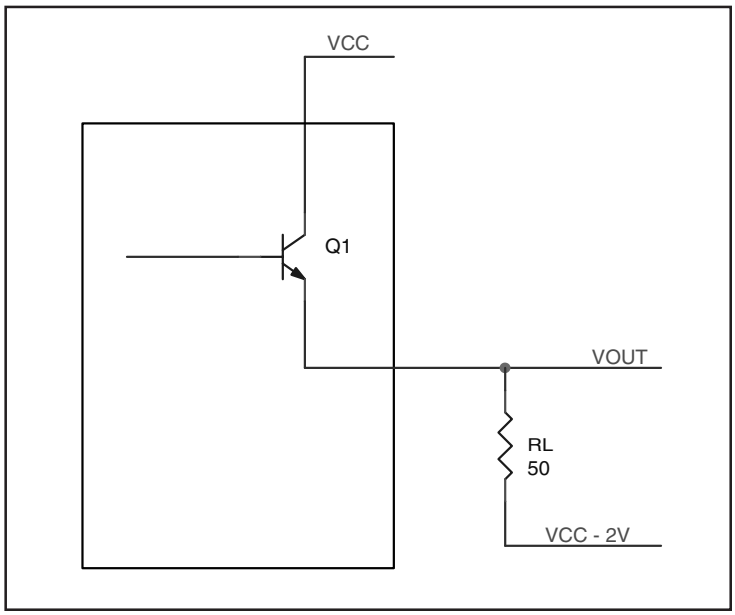


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.93V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.93}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.62V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.62V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.93V)/50\Omega] * 0.93V =$ **19.9mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.62V)/50\Omega] * 1.62V =$ **12.3mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.2mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85301 is: 137

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

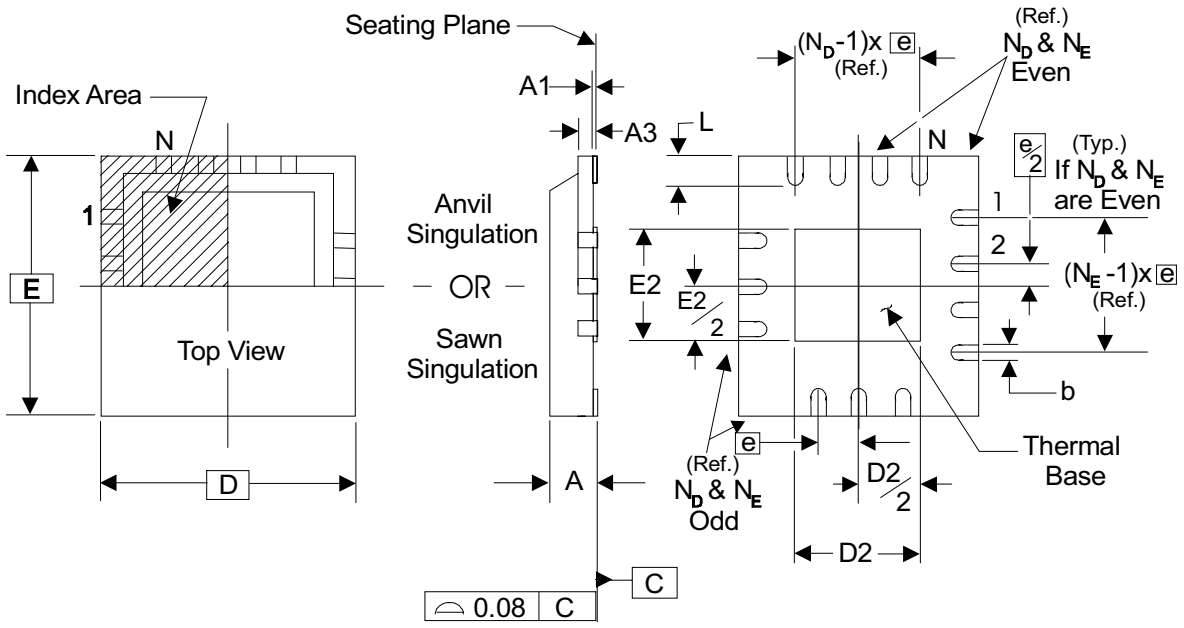


TABLE 8A. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	1.0	1.8
E	3.0	
E2	1.0	1.8
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Package Outline - G Suffix for 16 Lead TSSOP

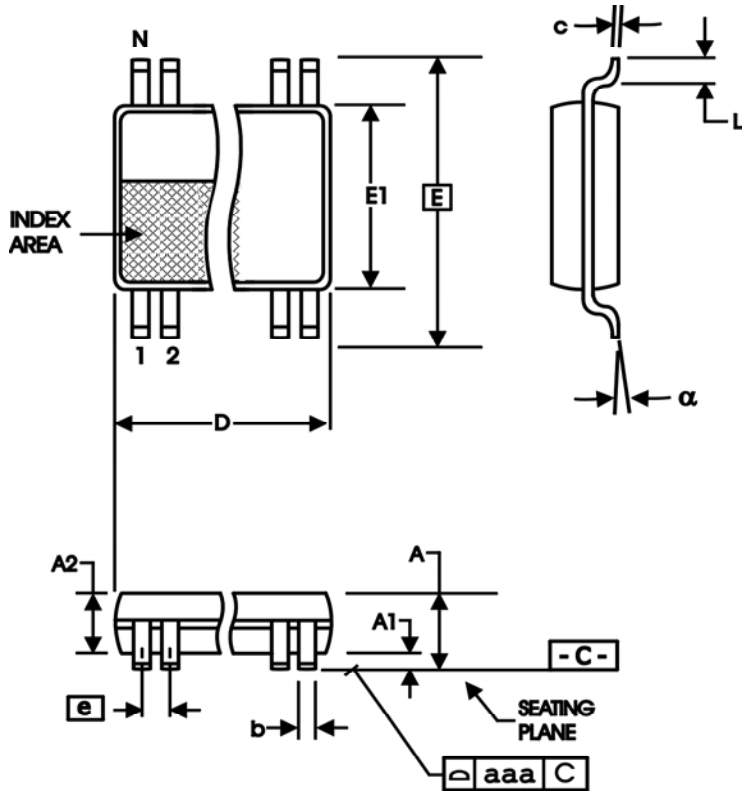


Table 8B. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85301AK	301A	16 Lead VFQFN	Tube	-40°C to 85°C
ICS85301AKT	301A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS85301AKLF	01AL	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
ICS85301AKLFT	01AL	16 Lead "Lead-Free" VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS85301AG	85301AG	16 Lead TSSOP	Tube	-40°C to 85°C
ICS85301AGT	85301AG	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS85301AGLF	85301AGL	16 Lead "Lead-Free" TSSOP	Tube	-40°C to 85°C
ICS85301AGLFT	85301AGL	16 Lead "Lead-Free" TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	17	Ordering Information Table - corrected count.	11/17/04
A			Added 16 Lead TSSOP package throughout the datasheet.	5/23/05
A	T9	10 18	Added *Recommendations for Unused Input Pins.* Ordering Information Table - added lead-free marking to ICS85301AGLF part number.	1/16/06
A	T9	18	Ordering Information Table - corrected Shipping Packaging for 16 lead VFQFN from Tray to Tube.	3/14/06
B	T4D	3	3.3V LVPECL DC Characteristic Table - added V_{SWING}. Changed V_{OH} from 2.01V min/2.535V max to V_{CC}-1.125V min/V_{CC}-0.93V max. Changed V_{OL} from 1.24V min/1.845V max to V_{CC}-1.895V min/V_{CC}-1.62V max.	4/5/06
	T4E	4	2.5V LVPECL DC Characteristic Table - added V_{SWING}. Changed V_{OH} from 1.25V min/1.705V max to V_{CC}-1.125V min/V_{CC}-0.93V max. Changed V_{OL} from 0.48V min/1.005V max to V_{CC}-1.895V min/V_{CC}-1.62V max.	
		13 - 14	Power Considerations - corrected power dissipation.	
B	T8A	12	Added *Thermal Release Path.*	12/22/06
		12	Updated Application Schematic Layout Example.	
		16	VFQFN Package Dimensions - corrected D2/E2 dimensions.	

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