Errata

IWR1642 Device Silicon Errata
Silicon Revisions 1.0 and 2.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR1642).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWRx (for example: **XI1642**QGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (IWR).

Device development evolutionary flow:

XI — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWR — Production version of the silicon die that is fully qualified.

XI devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the IWR1642 Radar Device's package symbolization.

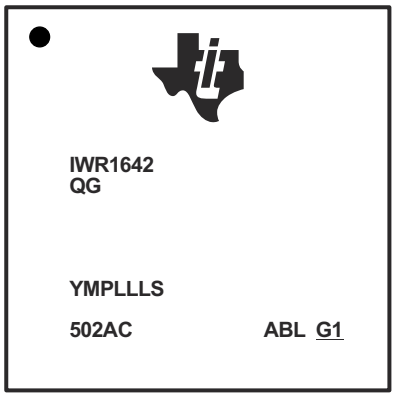

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - PLLL = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 502AC = IWR1642 ES2.0 Identifier
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects IWR1642 ES1.0.

5 Advisory to Silicon Variant / Revision Map

Table 5-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	IWR16xx	
		ES1.0	ES2.0
Main Subsystem			
MSS#10	Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled	X	
MSS#11	Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used	X	
MSS#12	MCAN Filter Event Interrupt not Connected to DMA	X	
MSS#14	Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	X	
MSS#16	Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification	X	
MSS#17	Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR	X	X
MSS#18 (1)	Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	X	X
MSS#19	DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario	X	X
MSS#20	Radar Frame Stuck due to Missing Synchronizer Logic in Hardware	X	X
MSS#22	CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields	X	X
MSS#37B	DCC Module Frequency Comparison can Report Erroneous Results	X	X
MSS#38A	GPIO Glitch During Power-Up	X	X
MSS#39	The state of the MSS DMA is left pending and uncleared on any DMA MPU fault	X	X
MSS#42	DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application.	X	X
MSS#43A	Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported	X	X
MSS#44	SYNC IN input pulse wider than 4usec can cause a FRC lockstep error	X	X
MSS#45	Bootup failure during the serial flash busy state	X	X
Analog / Millimeter Wave			
ANA#06	Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)	X	
ANA#08A	Doppler Spur Observed at Certain RF Frequencies	X	X
ANA#09A (1)	Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled	X	X
ANA#10A (1)	Unreliable Readings from Synthesizer Supply Voltage Monitor	X	X
ANA#11A	TX, RX Gain Calibrations Sensitive to Large External Interference	X	X
ANA#12A	Second Harmonic (HD2) Present in the Receiver	X	X
ANA#15	Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output	X	X
ANA#16	LVDS Coupling to Clock System	X	X
ANA#17A	On-Board Supply Ringing Induced Spur	X	X
ANA#18B	Spurs Caused due to Digital Activity Coupling to XTAL	X	X
ANA#20	Occasional Failures Observed During Calibration of the Radar Subsystem	X	X
ANA#21A	Out of Band Radiated Spectral Emission	X	X
ANA#22A	Overshoot and Undershoot During Inter-Chirp Idle Time	X	X
ANA#24A	40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum	X	X
ANA#27	Digital Temperature Sensor Having Higher Error	X	X
DSP Subsystem			
DSS#01	Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled	X	
DSS#02	L1P Parity Error not Connected to ESM	X	
DSS#03	Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported	X	

Table 5-1. Advisory to Silicon Variant / Revision Map (continued)

Advisory Number	Advisory Title	IWR16xx	
		ES1.0	ES2.0
DSS#04	Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory	X	
DSS#05	Byte Writes not Supported to L3 If ECC is Enabled	X	
DSS#06	Available L3 RAM for Customer Application is Lesser by 128KB	X	
DSS#07	Temperature Sensor Located Near DSP not Working	X	

(1) Applies to SIL Targeted devices.

6 Known Design Exceptions to Functional Specifications

MSS#10	***Partial Write After a Full Data Width Write Fails to Mailbox Memory if ECC is Enabled***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Partial data write after a full data width write would result is wrong data being written into the Mailbox memory if ECC is enabled.
Workaround(s):	None. Silicon update will be provided by TI.

MSS#11	***Clock Monitoring Logic Core Clock Comparator (CCCB) for CPU Clock Cannot be Used***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Clock used for the Watchdog Timer (WDT) is same as the CPU clock. CCCB can be dedicated to monitor CPU clock against a reference clock like XTAL/RCOSC to generate a WDT reset if CPU clock fails. However, CCCB does not consistently generate an error if the CPU clock stops ticking
Workaround(s):	None. Silicon update will be provided by TI.

MSS#12	*MCAN Filter Event Interrupt not Connected to DMA*
Revision(s) Affected:	IWR1642 ES1.0
Description:	MCAN filter event interrupt is only connected to MSS VIM and not connected to MSS DMA. If a DMA transfer operation is expected to happen on this interrupt , MSS CR4 will have to trigger the DMA
Workaround(s):	None. Silicon update will be provided by TI.

MSS#14 ***Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock***

Revision(s) Affected: IWR1642 ES1.0

Description: Asynchronous assertion of SoC warm reset through WARM_RESET pin, SW reset, watchdog reset, or Debug reset may not reliably work and may also result in a system hang scenario.

Workaround(s): MSS VCLK must be switched from PLL clock to REFCLK by following the prescribed software sequence before a warm reset is issued.

MSS#16 ***Delay Time, ETM Trace Clock to ETM Data Valid does not Meet Datasheet Specification***

Revision(s) Affected: IWR1642 ES1.0

Description: Delay time, ETM trace clock to ETM data valid does not meet datasheet specification below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	1	7	ns
Delay time, ETM trace clock low to ETM data valid	1	7	ns

In IWR1642 ES1.0, Delay time, ETM trace clock to ETM data timing that is being met is as given below:

PARAMETER	MIN	MAX	UNIT
Delay time, ETM trace clock high to ETM data valid	–0.5	7	ns
Delay time, ETM trace clock low to ETM data valid	–0.5	7	ns

Workaround(s): None. Silicon update will be provided by TI.

MSS#17 ***Invalid Pre-fetch from MSS CR4 Processor (due to Speculative Read Operation from Tightly Coupled Memory Instance) Leads to Generation of MSS_ESM Group 3 Channel 7: MSS_TCMA_FATAL_ERR***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The CR4 processor may perform an invalid pre-fetch access due to speculative TCM read leading to an invalid address access. This can result in a TCERROR and also a 2-bit ECC fatal error. The TCERROR is ignored by the processor since these correspond to instructions that are pre-fetched but never executed. However, the invalid MSS_TCMA_FATAL_ERR is generated on the ESM group3 channel-7.

Implication: In case of a genuine TCMA ECC fatal error, nERROR will not be generated directly through ESM.

Workaround(s): Mask Group 3 channel 7: MSS_TCMA_FATAL_ERR to ESM can be masked by writing into MSS_RCM:ESMGATE0 register. CR4F abort handler should handle the nERROR generation

OR

Disable branch prediction for MSS-CR4F

MSS#18 ***Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

Workaround(s): The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

MSS#19 ***DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70 for DMA1 and VIM Interrupt Channel-51 for DMA2 .This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.

Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.

Workaround(s): The MSS CR4F processor will have to invoke a warm reset or generate an nERROR if it receives a DMA BER error.

MSS#20 ***Radar Frame Stuck due to Missing Synchronizer Logic in Hardware***

Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	Radar Sub System Internal Frame Clock is triggered by rlSensorStart API which starts the Radar Frame. Occasionally the rlSensorStart API does not trigger the clock due to missing synchronizer logic in hardware. *Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.*
Workaround(s):	The issue is frequent if FRC clock source is changed. Ensure that FRC Clock source is not changed.

MSS#22 ***CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields***

Revision(s) Affected: IWR1642 ES1.0 and IWR1642 ES2.0

Description: Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission
- A new transmission is requested before the 3rd bit of Intermission is reached
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2)

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The M_CAN will start arbitration with wrong ID, format, and DLC on the next bit
- In case the ID wins arbitration, a CAN message with valid CRC is transmitted
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, no error is detected by the transmitting M_CAN

The erratum is limited to the case when M_CAN is in state "Receiver" (PSR.ACT = "10") with no pending transmission and a new transmission is requested before the 3rd bit of Intermission is reached and this 3rd bit of intermission is seen dominant.

When a transmission is requested by the CPU, the Tx Message Handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated between the sample points of the 2nd and 3rd bit of Intermission and if that 3rd bit of intermission is seen dominant.

This dominant level at the 3rd bit of Intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

Workaround(s): Request a new transmission only if another transmission is already pending or when the M_CAN is not in state "Receiver" (when PSR.ACT ≠ "10").

Another option would be to add a checksum to the data field covering arbitration and control fields of the message to be transmitted.

MSS#37B	*DCC Module Frequency Comparison can Report Erroneous Results*
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.
Workaround(s):	Multiple measurements can be taken for the same clock pairs and abnormal frequencies reported can be ignored Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

MSS#38A	***GPIO Glitch During Power-Up***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*), if the 3.3V supply powers up before the 1.8V supply. This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.
Workaround(s):	Powering up the 1.8V supply before the 3.3V supply resolved the issue. Incase that is not feasible, AND the GPIO is used for critical controls where glitch cannot be tolerated, the GPIO output should be gated by the nRESET signal of the xWR device. Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

MSS#39	***The state of the MSS DMA is left pending and uncleared on any DMA MPU fault***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	The state of the MSS DMA is left pending and uncleared on any DMA MPU fault. The transfer that caused this MPU fault is left pending inside the DMA IP. Any trigger on DMA REQ lines (could be caused by any module/IP that is hooked up to DMA in h/w) can re-trigger DMA to start executing the above pending transfer irrespective of whether that trigger is actually valid/enabled in DMA or that module/IP
Workaround(s):	For devices where the Boot ROM is executing the MSS DMA MPU Self tests. As part of application initialization, if the MSS DMA will be used, the following register field should be used to reset the MSS DMA IP so that the uncleared transfer is reset 1. Write MSS_RCM:SOFTRST1[31:24] 0xAD 2. Write MSS_RCM:SOFTRST1[31:24] 0x0 It is not recommended to use this configuration at any another instance other than that recommended here in this Errata. On an actual Real time MPU Error, this error should be treated as a non-recoverable error and a warm reset should be issued to recover.

MSS#42	***DSP L2 memory initialisation can reoccur on execution DSP self test (STC) OR DSP Power cycling execution by application.***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	MSS Boot ROM Powers on DSP, Performs a Memory Initialisation of DSP L2 and downloads the program code to L2 memory. If the user application executes the STC or DSP power cycle, memory init is triggered again, hence erasing the L2 memory contents.
Workaround(s):	The workaround for Mem init would be to perform a Dummy mem init to reset a latch within the IP while keeping the destination domain in reset. This can be done by the application using the below sequence before running STC or DSP power cycling: 1. Set the GEM_CLK_EN_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG2 register Bit 7 as ‘1’. 2. Set the GEM_GRSTN_GATE_BYPASS_CTRL bit in the TOPRCM-> GEMPWRSMCFG1 Bit 9 register as ‘1’. 3. Write a value of 0xFFFF in , DSS_REG ->L2MEMINITCFG1 register. 4. Write a value of 0xF in , DSS_REG ->L2MEMINITCFG2 register 5. Write a value of 0x0 in TOPRCM-> GEMPWRSMCFG1-> PWRSMOUTBYPCTRL register.

MSS#43A	***Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	The main subsystem has PCR interconnect that manages the accesses to the peripheral registers and peripheral memories, and provides a global reset for all peripherals. The read-data from PCR is getting corrupted before handing it of to VBUSP interconnect. So any partial write to PCR-registers is not reliable. Peripheral access is blocked by writing to internal registers which is not feasible. Shared PCS region protection is also not supported
Workaround(s):	No workaround

MSS#44	***SYNC IN input pulse wider than 4usec can cause a FRC lockstep error***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse if > 4usec, it could cause MSS ESM group 1 fault with FRC lockstep error.
Workaround(s):	The pulse width of the external SYNC IN signal should be >25nsec and < 5usec

MSS#45	***Bootup failure during the serial flash busy state***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	If the radar device is rebooted internally or externally while the serial flash is busy completing a previous operation, like erase, format etc, the radar device might fail to bootup since the serial flash would not respond to the commands from the bootloader during the bootup process.
Workaround(s):	The user application should make sure if its triggering an internal reset due to watch dog expiry or other reasons, it should reset the serial flash to bring it to a known state or wait for completion of any pending issued commands to serial flash before it resets the XWR device.

ANA#06	***Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)***
Revision(s) Affected:	IWR1642 ES1.0
Description:	The return loss measurement on TX S11 is < –9dB and the return loss measurement on RX S11 is < –6.5dB. The accepted value is < –10dB.
Workaround(s):	None. TI expects to provide an update along with the next silicon revision.

ANA#08A	***Doppler Spur Observed at Certain RF Frequencies***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	When the instantaneous FMCW Ramp frequency nears certain specific RF frequencies, there can be coupling between the synthesizer's reference and its output, and manifest as frequency glitches or spurs in TX output spectrum. Implication: In FMCW radar 2D signal processing, this can lead to spurs in a fixed Doppler bin at all range bins. This situation can occur with narrow band chirps, if the FMCW ramp includes or nears 76.8-, 77.4-, 78-, 79.2-, 80.4-, 81-GHz RF frequencies. The affected Doppler bin is a function of chirp timing and RF frequency properties.
Workaround(s):	Use the device's dithering features to vary idle time, RF frequency and ramp end times to spread the spurs significantly in Doppler dimension so that it does not get detected as spurious targets. Using larger chirp band widths also reduces the spur level.

ANA#09A	***Synthesizer Frequency Nonlinearity around 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	When the synthesizer (chirp) frequency monitor is enabled and the synthesizer chirp is around 76.8 GHz, the frequency error can be as high as 500 kHz due to coupling between the monitor and the synthesizer. The RF frequencies impacted are 500Mhz around 76.8Ghz (76.8 ± 0.5 GHz). *Implication: Increased nonlinearity in the chirp can lead to up to 20 dB degradation in the noise floor surrounding large objects. This leads to potential loss of dynamic range when large and small objects are present simultaneously.*
Workaround(s):	1. Disable the synthesizer frequency monitor during profiles where the LO crosses 76.8 ± 0.5 GHz. 2. Use non-functional chirps to detect nonlinearities (instead of high instantaneous frequency errors) in the synthesizer by inserting dummy chirps (where RX data is not used) after functional chirps (where RX data is consumed).

ANA#10A	***Unreliable Readings from Synthesizer Supply Voltage Monitor***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior. *Implication: The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.*
Workaround(s):	Ignore the field STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

ANA#11A	***TX, RX Calibrations Sensitive to Large External Interference***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	External interference present on the RX or TX pins, during the period of the device calibration at RfInit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration. It also impacts run-time Tx output power calibration in CLPC mode.
Workaround(s):	**Workaround #1:** The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed. **Workaround #2:** Another workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored. For the runtime Tx output power calibrations, OLPC mode can be used instead of the CLPC mode.

ANA#12A	***Second Harmonic (HD2) Present in the Receiver***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc , referenced to the power level of the intended tone at the LNA input.
Workaround(s):	No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons: 1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer). 2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#15	***Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -10dBm.
Workaround(s):	Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.

ANA#16	*LVDS Coupling to Clock System*
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).
Workaround(s):	The spur will not be present, when the LVDS is not used.

ANA#17A	***On-Board Supply Ringing Induced Spur***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur (~130KHz) in the FMCW synthesizer output spectrum.
Workaround(s):	**Workaround #1:** Disable inter-chirp duty cycling of the RX. ***or*** **Workaround #2:** Design the power supply to damp out the ringing on the rails to the device.

ANA#18B ***Spurs Caused due to Digital Activity Coupling to XTAL***

Revision(s) Affected: IWR1642 ES1.0 and ES2.0

Description: Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate (Fs). The strongest of these spurs have been observed when Fs is close to 10, 12.5, 18, 18.75,20, 25, Msps. In these ranges, an IF spur can appear at Fs-10 Mhz, 2Fs-40MHz, 4Fs-40 MHz, 4Fs-100 MHz, 8Fs-100 MHz , 2Fs-37.5 MHz, 2Fs-36 MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

Workaround(s):

Workaround #1:

Avoid sampling rates close to these numbers (10, 12.5, 18, 18.75, 20, 25 Msps) or use exactly these numbers (spur is at 0 Hz in the latter case).

Workaround #2:

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

ANA#20	***Occasional Failures Observed During Calibration of the Radar Subsystem***
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.
Workaround(s):	**Workaround #1:** Any APLL calibration failure needs to be responded with a reset cycle. ***or*** **Workaround #2:** Any SYNTH calibration failure reported by the BSS will require an RFinit.

ANA#21A	***Out of Band Radiated Spectral Emission***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.
Workaround(s):	A grounded metallic shield around the device (excluding the antenna region) can be used to reduce the emission levels. Microwave absorber materials could also be placed on the device to reduce the emissions.

ANA#22A	***Overshoot and Undershoot During Inter-Chirp Idle Time***
Revision(s) Affected:	IWR1642 ES1.0 and ES2.0
Description:	At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.
Workaround(s):	To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

ANA#24A	*40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum*
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	Harmonics of 40 MHz from osc-clkout can be coupled onto the synthesizer and can cause low amplitude spurs in the 2D-FFT spectrum. These spurs are at fixed doppler bin, across all range bins.
Workaround(s):	For single chip usecases, where OSC CLKOUT is not used , OSC CLKOUT output can be disabled.

ANA#27	*Digital Temperature Sensor Having Higher Error*
Revision(s) Affected:	IWR1642 ES1.0 and IWR1642 ES2.0
Description:	Due to the single-ended nature of the digital temperature sensors, as compared to the differential design of analog temperature sensors (that is, TX, RX, and PM), it is vulnerable to noise and can have higher error than the analog temperature sensors.
Workaround(s):	Use only the analog temperature sensor values (TX and RX) in the algorithm. The digital temperature sensor value can be ignored.

DSS#01	***Access to L3 Region Above Allocated Region may Result in Double Bit ECC Error if ECC is Enabled***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Access to L3 region above allocated region may result in a Double Bit ECC error in addition to the data abort if ECC is enabled.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#02	***L1P Parity Error not Connected to ESM***
Revision(s) Affected:	IWR1642 ES1.0
Description:	L1P parity error is only connected to DSP and not connected to MSS ESM.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#03	***Different Number of Chirps in ADC Buffer's Ping and Pong Memory is not Supported***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Different number of chirps in ADC buffer's ping and pong memory is not supported. They need to be programmed to a same value and the configuration for number of chirps in Ping and Pong can only be changed at Sub-Frame boundary.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#04	***Partial Write After Full Data Width Write Fails to HS RAM, ADC Buffer and Data Transfer Memory if ECC is Enabled for that Memory***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Partial data write after a full data width write would result in wrong data being written into HS RAM , ADC buffer and Data Transfer memory if ECC is enabled for that memory.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#05	***Byte Writes not Supported to L3 If ECC is Enabled***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Byte writes are not supported to L3 memory when ECC is enabled. ECC invalidation does not work correctly in this scenario.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#06	***Available L3 RAM for Customer Application is Lesser by 128KB***
Revision(s) Affected:	IWR1642 ES1.0
Description:	Due to available RAM being used for Radar block development, RAM available for user application is limited to 640 KB instead of 768 KB.
Workaround(s):	None. Silicon update will be provided by TI.

DSS#07	***Temperature Sensor Located Near DSP not Working***
Revision(s) Affected:	IWR1642 ES1.0
Description:	The temperature sensor that is located near the DSP is not working in IWR1642 ES1.0. This is a known bug that will be fixed in ES2.0. There are eight temperature sensors located throughout the analog, all of which are working and accessible via an API call.
Workaround(s):	None. Silicon update will be provided by TI.

7 Trademarks

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8 Revision History

Changes from April 27, 2018 to May 31, 2021 (from Revision B (April 2018) to Revision C (May 2021)) Page

- ***(Advisory to Silicon Variant / Revision Map):*** Added ANA#11A, ANA#12A, ANA#15 through ANA#18B, ANA#20, ANA#21A, ANA#22A, ANA24A, ANA27 advisories under Analog / Millimeter Wave, all silicon revisions.....5
- ***(Advisory to Silicon Variant / Revision Map):*** Added MSS#20, MSS#22, MSS#37B, MSS#38A, MSS#39 and MSS#42 through MSS#45 advisories under Main Subsystem, all silicon revisions.....5
- ***(Advisory to Silicon Variant / Revision Map):*** Updated/modified ANA#08A, ANA#09A, ANA#10A advisories under Analog / Millimeter Wave, all silicon revisions.....5

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