AK8158A

Multiclock Generator with VCXO

1. General Description

The AK8158A is a member of AKM's low power multi clock generator family designed for a feature rich DTV or STB, requiring a range of system clocks with high performance. The AK8158A generates different frequency clocks from a 27MHz crystal oscillator and provides them to up to four outputs configured by pin-setting. The on-chip VCXO accepts a voltage control input to allow the output clocks to vary by ±110 ppm for synchronizing to the external clock system. Both circuitries of VCXO and PLL in AK8158A are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8158A is available in a 20-pin QFN package.

2. Features

- 27MHz Crystal Input
- Four Frequency-Selectable Clock Outputs
- One 27MHz-Reference Output
- Selectable Clock out Frequencies:
  - 74.1758, 74.250MHz
  - 25.000MHz
  - 4.9152, 12.000, 24.000,24.576MHz
  - 33.333MHz
- Built-in VCXO
  - Pull Range: ±110ppm (Min.)
- Low Jitter Performance
  - Period Jitter:
    30psec typ. (1σ) at CLK1-4
  - Long Term Jitter:
    150psec typ. (1σ) 74.1758MHz
    30psec typ. (1σ) at REFOUT
- Low Current Consumption:
  16.5mA typ. at 3.3V
- Supply Voltage:
  2.85 – 3.6V
- Operating Temperature Range:
  -20 to +85°C
- Package:
  20-pin QFN (Lead free)
- Application:
  - Digital TV Sets
  - Personal Video Recorders
  - Set Top Boxes
  - Multi Media Receivers
  - Closed-Circuit Television

3. Table of Contents

4. Block Diagram and Functions

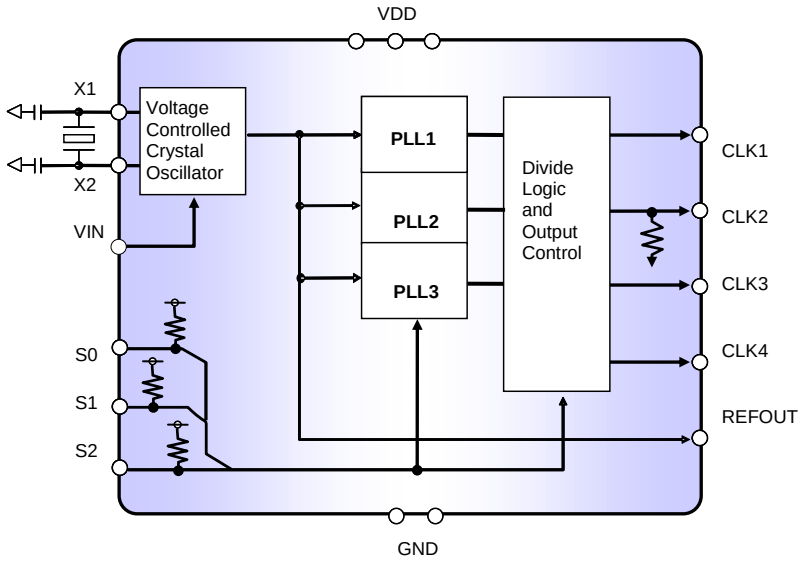


Figure 1. AK8158A Multi Clock Generator

5. Pin Configurations and Functions

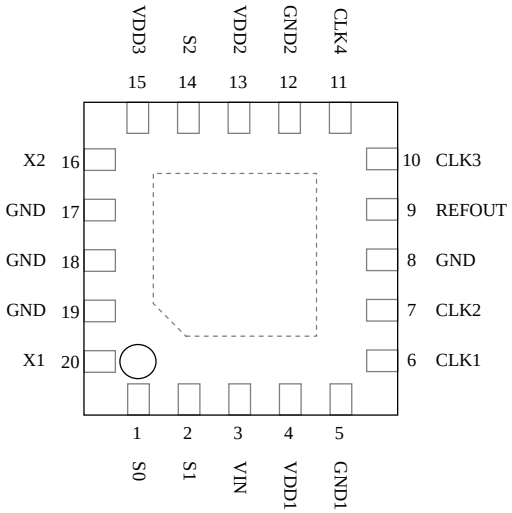


Figure 2. AK8158A Package: 20-Pin QFN(Top View)

Pin No.	Pin Name	Pin Type	Description
1	S0	IN	Clock Out Frequency Select 0, See Table 1 for the selection (2)
2	S1	IN	Clock Out Frequency select 1, See Table 1 for the selection (2)
3	VIN	IN	VCXO Control Voltage Input
4	VDD1	--	Power Supply 1
5	GND1	--	Ground 1
6	CLK1	OUT	Clock output 1, See Table 1 for its selectable frequency
7	CLK2	OUT	Clock output 2, See Table 1 for its selectable frequency (3)
8	GND	--	Connect to Ground
9	REFOUT	OUT	Reference Clock Output of VCXO based on 27.000MHz Crystal
10	CLK3	OUT	Clock output 3, See Table 1 for its selectable frequency
11	CLK4	OUT	Clock output 4, See Table 1 for its selectable frequency
12	GND2	--	Ground 2
13	VDD2	--	Power Supply 2
14	S2	IN	Clock Out Frequency select 1, See Table 1 for the selection (2)
15	VDD3	--	Power Supply 3
16	X2	XI	Crystal connection, Connect to 27.000MHz crystal Or external clock input (minimum 1Vpp input).
17	GND	--	Connect to Ground
18	GND	--	Connect to Ground
19	GND	--	Connect to Ground
20	X1	XO	Crystal connection, Connect to 27.000MHz crystal Please open when an external clock input is used

Note:

(1) The heatsink pad on the bottom surface of the package can be open or be connected to GND.

(2) Internal pull up 360kΩ

(3) Internal pull down 510kΩ

6. Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage (1)	VDD		2.85	3.3	3.6	V
Output Load Capacitance	Cp1	Pin: CLK1-4			15	pF
	Cp2	Pin: REFOUT			25	pF

Note:

(1) Power to VDD1, VDD2 and VDD3 requires to be supplied from a single source. A decoupling capacitor of 0.1µF for power supply line should be installed close to each VDD pin.

8. Electrical Characteristics

DC Characteristics

All specifications at VDD: over 2.85 to 3.6V, Ta: -20 to +85°C, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: S0, S1, S2	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: S0, S1, S2			0.3VDD	V
Input Current 1	I_L1	Pin: S0, S1, S2	-20		+1.5	μA
Input Current 2	I_L2	Pin: VIN	-3		+3	μA
High Level Output Voltage	V_{OH}	Pin: CLK1-4, REFOUT I_{OH} = -4mA (1)	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK1-4, REFOUT I_{OL} = +4mA (1)			0.2VDD	V
Current Consumption	I_{DD}	No load Clock out selection by note (2) Ta = 25°C		18.0		mA
		No load Clock out selection by note (3) Ta = 25°C		16.5		mA

Note:

(1) Polarity(-): Outgoing current from device
Polarity(+): Incoming current to device

(2) Pin setting for output clock selection: [S2:S0] = “HLL”

(3) Pin setting for output clock selection: [S2:S0] = “HLH”

AC Characteristics

All specifications at VDD: over 2.85 to 3.6V, Ta: over -20 to +85°C, 27MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency				27.0000		MHz
VCXO Pullable Range (3)		VIN at over 0 to VDD V	±110			ppm
VCXO Gain	G_{VCXO}	VIN range at 1.5V±1.0V		150		ppm/V
Period Jitter (4)		CLK1-4		30		ps
Long Term Jitter (4)		CLK1 at 74.1758MHz 1000 cycle delay		150		ns
		REFOUT at 27.000MHz 1000 cycle delay		30		ps
Output Clock Duty Cycle		Pin: CLK1-4 (1)	45	50	55	%
		Pin: REFOUT (2)	40	50	60	%
Output Clock Rise Time	t_{rise}	Pin: CLK1-4 (1)		1.5	4	ns
		Pin: REFOUT (2)		2.5	4	ns
Output Clock Fall Time	t_{fall}	Pin: CLK1-4 (1)		1.5	4	ns
		Pin: REFOUT (2)		2.5	4	ns
Power-up Time		Pin: CLK1-4 (1)		1	2	ms
Output Transition Time (5)		Pin: CLK1 at 74.25 or 74.175MHz		90	140	μs

Note:

(1) Measured with load capacitance of 15pF
(2) Measured with load capacitance of 25pF
(3) Pullable range depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. Min. ±110ppm is applied to AKM's authorized test condition.
(4) 1σ in 10000 sampling or more
(5) Time to settle output into ±20ppm of specified frequency

9. Functional Descriptions

Output clock frequency selection

The AK8158A generates a range of low-jitter and hi-accuracy clock frequencies with three built-in PLLs and provides to up to four assigned outputs. A frequency selection at assigned output pin is configured by pin-setting of S0 (Pin 1), S1 (Pin 2), and S2 (Pin 14).
The selectable frequency is shown in
Table 1..

Table 1. Clock output Frequency

Selection Pin			Clock Output Frequency (MHz)			
S2 (Pin 14)	S1 (Pin 2)	S0 (Pin 1)	CLK1 (Pin 6)	CLK2 (Pin 7)	CLK3 (Pin 10)	CLK4 (Pin 11)
L	L	L	74.250	25.000	24.000	33.333
L	L	H	74.250	25.000	12.000	33.333
L	H	L	74.1758	25.000	24.000	33.333
L	H	H	74.1758	25.000	12.000	33.333
H	L	L	74.250	25.000	24.576	33.333
H	L	H	74.250	OFF	24.000	33.333
H	H	L	74.1758	25.000	24.576	33.333
H	H	H	74.1758	25.000	4.9152	33.333

Voltage Control Crystal Oscillator (VCXO)

The AK8158A has a voltage control crystal oscillator (VCXO), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system. VIN (Pin 3) accepts DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by crystal characteristic, on-chip load capacitor, and stray capacitance of PCB. The AK8158A is designed to range ±110ppm of primary frequency in AKM's authorized condition.

10. Recommended External Circuits

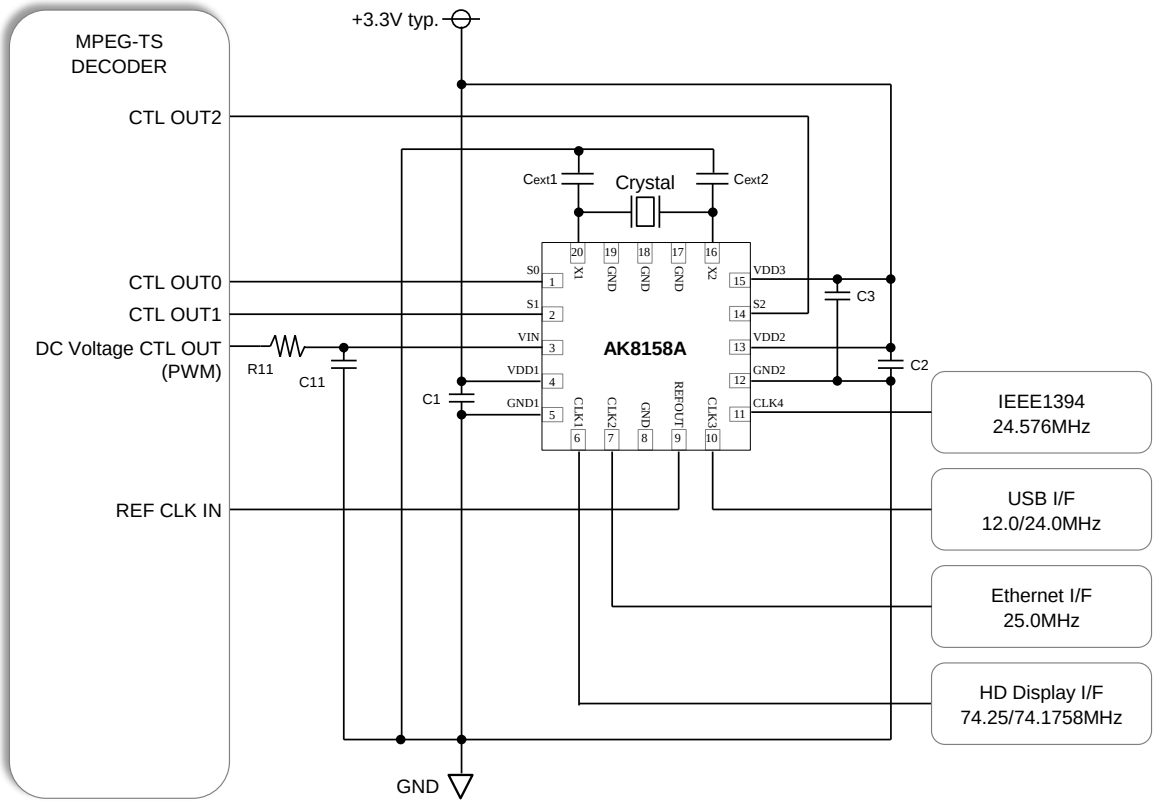


Figure 3: Typical Connection Diagram

C1, C2, C3: 0.1μF
Cext1, Cext2: Depends on crystal characteristics. Refer the specification of the crystal.
R11, C11: In case of interface by PWM. For right configuration, refer the specification of the applied processor.

PCB Layout Consideration

The AK8158A is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure ..

Power supply line – AK8158A has three power supply pins (VDD1-3) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

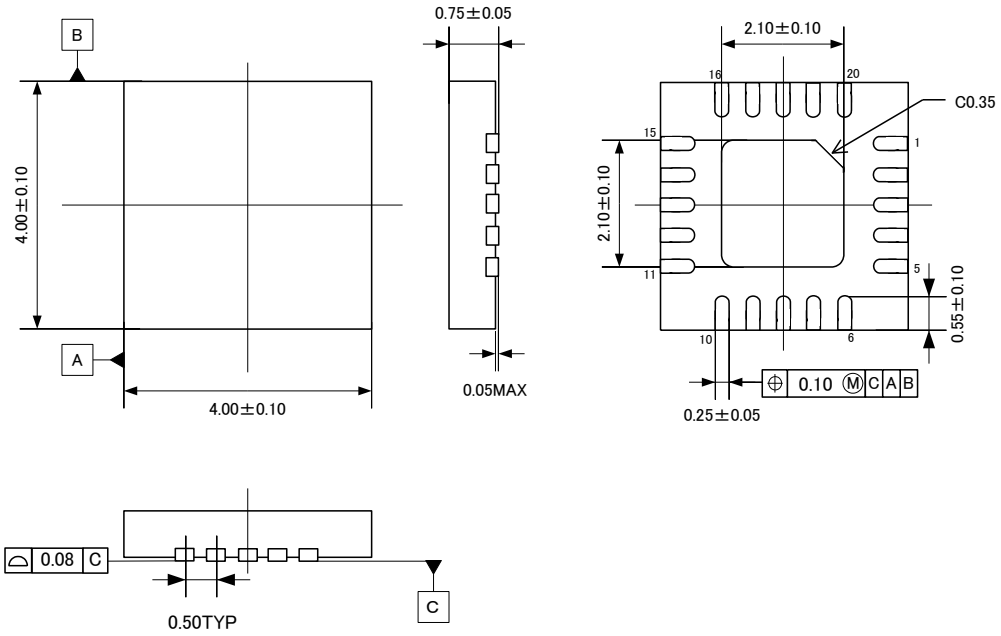
Ground pin connection – AK8158A has two ground pins (GND1-2). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1μF decoupling capacitors placed at VDD1, VDD2, and VDD3 should be grounded at close to the GND1pin, the GND2 pin, and the GND2, respectively.

Crystal connection – Proper oscillation performance and pullable range are susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form X1 (Pin 20) and X2 (Pin 16) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

11. Package

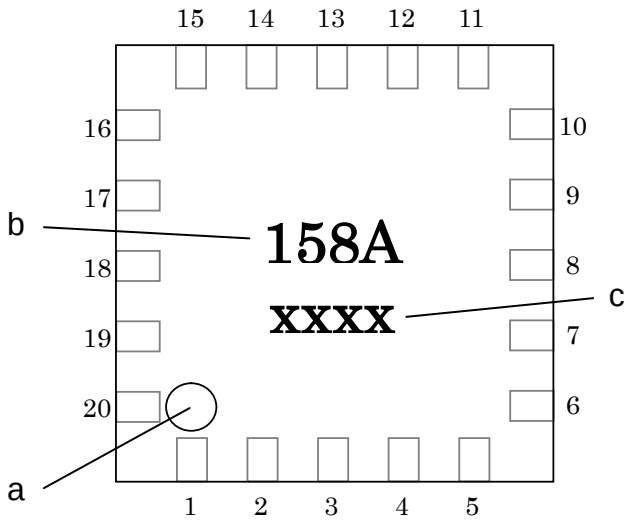
Outline Dimensions

20pin QFN (Unit: mm)



Marking

a: #1 Pin Index
b: Part number
c: Date code (4 digits: YWWL, Year/Weak/Lot No.)



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