

## 500-kHz Half-Bridge DC/DC Controller with Integrated Secondary Synchronous Rectification Drivers

### DESCRIPTION

Si9122 is a dedicated half-bridge IC ideally suited to fixed telecom applications where efficiency is required at low output voltages (e.g. < 3.3 V). Designed to operate within the fixed telecom voltage range of 33 to 72 V, the IC is capable of controlling and driving both the low and high-side switching devices of a half bridge circuit and also controlling the switching devices on the secondary side of the bridge. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in the efficiency can be achieved as compared with conventional Schottky diodes. Control of the secondary devices is by means of a pulse transformer and a pair of inverters. Such a system has efficiencies well in excess of 90 % even for low output voltages. On-chip control of the dead time delays between the primary and secondary synchronous signals keep efficiencies high and prevent accidental destruction of the power transformer. An external resistor sets the switching frequency from 200 kHz to 625 kHz.

Si9122 has advanced current monitoring and control circuitry which allow the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorting and also provides constant current into large capacitive loads during start-up or when paralleling power supplies. Current sensing is by means of a sense resistor on the low-side primary device.

### FEATURES

- 12 V to 72 V input voltage range
- Integrated half-bridge primary drivers (1 A drive capability)
- Secondary synchronous signals with programmable deadtime delay
- Voltage mode control
- Voltage feedforward compensation
- High voltage pre-regulator operates during start-up
- Current sensing on low-side primary device
- Frequency foldback eliminates constant current tail
- Advanced maximum current control during start-up and shorted load
- Low input voltage detection
- Programmable soft-start function
- Over temperature protections



RoHS  
COMPLIANT

### APPLICATIONS

- Network cards
- Power supply modules

### FUNCTIONAL BLOCK DIAGRAM

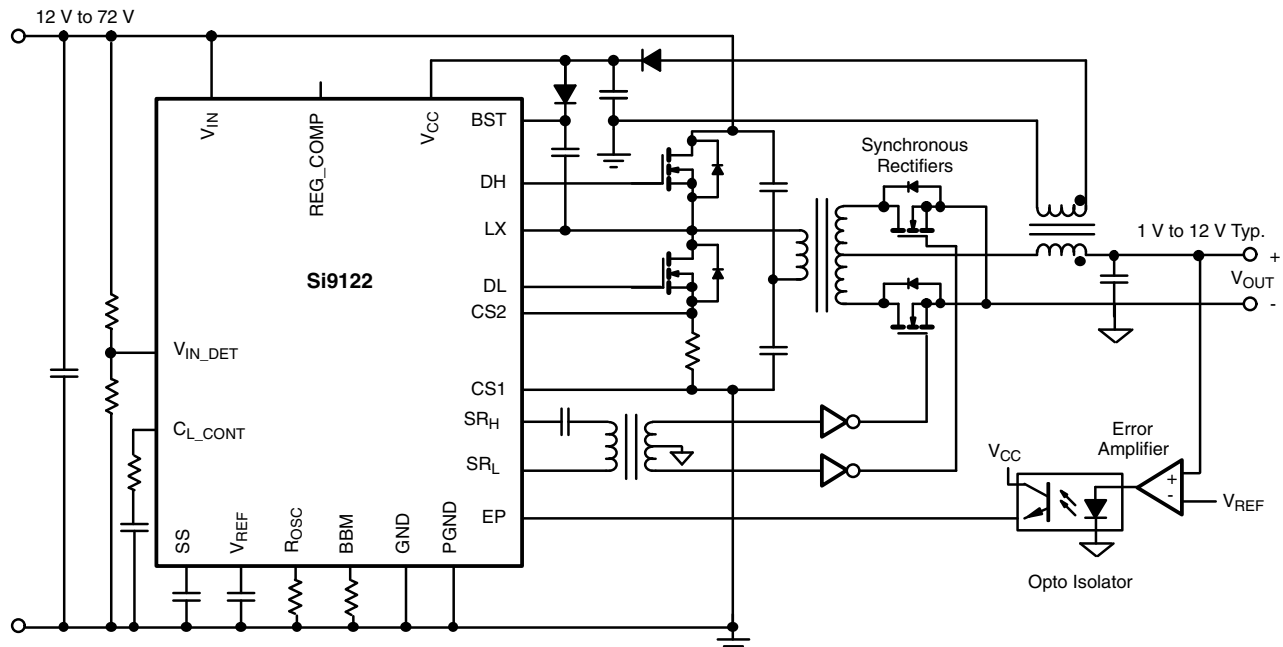


Figure 1.

## TECHNICAL DESCRIPTION

Si9122 is a voltage mode controller for the half-bridge topology. With 100 V depletion mode MOSFET capability, the Si9122 is capable of powering directly from the high voltage bus to  $V_{CC}$  through an external PNP pass transistor, or may be powered through an external regulator directly through the  $V_{CC}$  pin. With PWM control, Si9122 provides peak efficiency throughout the entire line and load range. In order to simplify the traditional secondary synchronous rectification, Si9122 provides intelligent gate drive signals to control the secondary MOSFETs. With independent gate drive signals from the controller, transformer design is no longer limited by the gate to a source rating of the MOSFETs. Si9122 provides constant  $V_{GS}$  voltage, independent of line voltage to minimize the gate charge loss as well as conduction loss. A break-before-make function is included to

prevent shoot through current or transformer shorting. Adjustable Break-Before-Make time is incorporated into the IC and is programmable by an external resistor value.

Si9122 is packaged in TSSOP-20 and MLP65-20 packages. Both TSSOP-20 and MLP65-20 packages are available in lead (Pb)-free option. In order to satisfy the stringent ambient temperature requirements, Si9122 is rated to handle the industrial temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ . When a situation arises which results in a rapid increase in primary (or secondary current) such as output shorted or start-up with a large output capacitor, control of the PWM generator is handed over to the current loop. Monitoring of the load current is by means of a sense resistor on the primary low-side switch.

## DETAILED BLOCK DIAGRAM

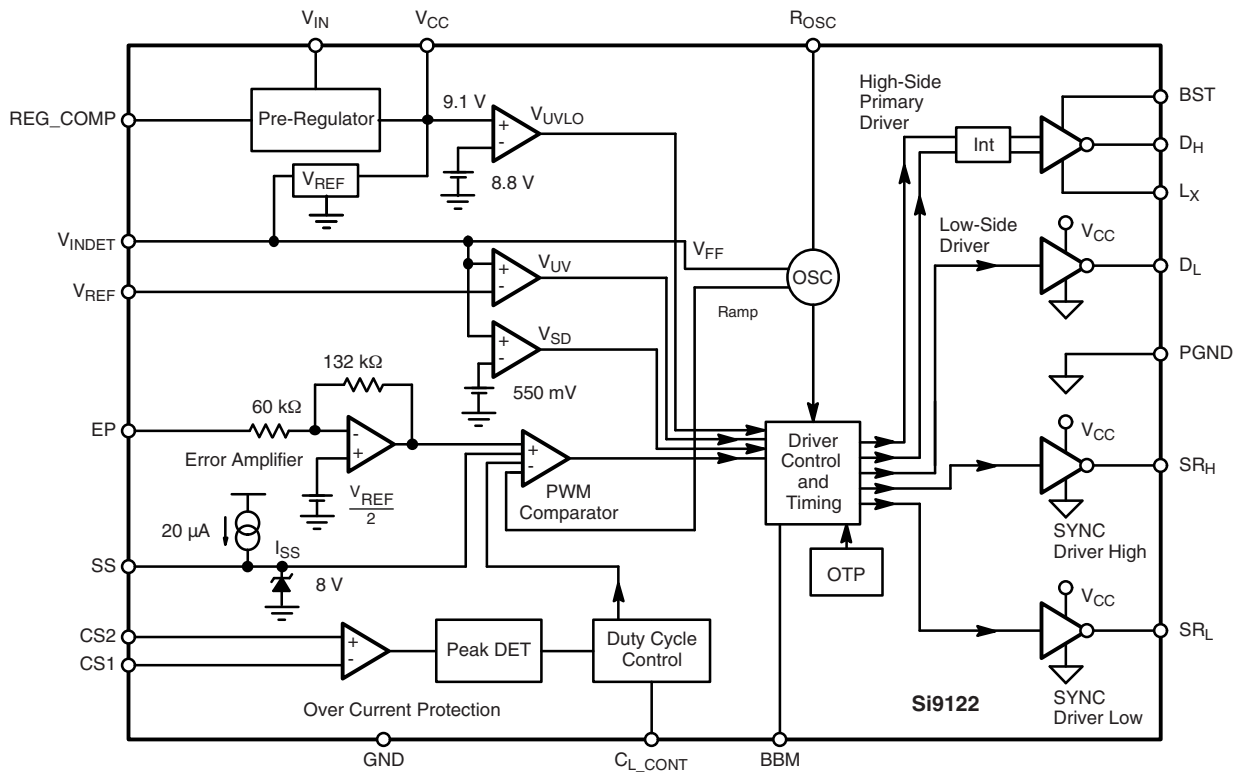


Figure 2.



<b>ABSOLUTE MAXIMUM RATINGS</b> All voltages referenced to GND = 0 V			
Parameter		Limit	Unit
$V_{IN}$ (Continuous)		75	V
$V_{IN}$ (100 ms)		100	
$V_{CC}$		14.5	
$V_{BST}$	Continuous	90	
	100 ms	115	
$V_{LX}$		75	
$V_{BST} - V_{LX}$		15	
$V_{REF}$ $R_{OSC}$		- 0.3 to $V_{CC} + 0.3$	
Logic Inputs		- 0.3 to $V_{CC} + 0.3$	
Analog Inputs		- 0.3 to $V_{CC} + 0.3$	
HV Pre-Regulator Input Current (Continuous)		5	mA
Storage Temperature		- 65 to 150	°C
Operating Junction Temperature		150	
Power Dissipation <sup>a</sup>	TSSOP-20	850	mW
	MLP65-20	2500	
Thermal Impedance ( $\Theta_{JA}$ )	TSSOP-20 <sup>b</sup>	75	°C/W
	MLP65-20 <sup>c</sup>	38	

Notes:

- a. Device Mounted on JEDEC compliant 1S2P test board.
- b. Derate - 14 mW/°C above 25 °C.
- c. Derate - 26 mW/°C above 25 °C.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

<b>RECOMMENDED OPERATING RANGE</b> All voltages referenced to GND = 0 V			
Parameter		Limit	Unit
$V_{IN}$		12 to 72	V
$C_{VIN1} \parallel C_{VIN2}$		100 $\mu$ F/ESR $\leq$ 100 m $\Omega$ , 0.1 $\mu$ F	
$V_{CC}$ Operating		10 to 13.2	V
$C_{VCC}$		4.7	$\mu$ F
$f_{OSC}$		200 to 600	kHz
$R_{OSC}$		24 to 72	k $\Omega$
$R_{BBM}$		22 to 50	
$C_{BBM}^h$		> 680	pF
$C_{SS}$		4.7	nF
$C_{REF}$		0.1	$\mu$ F
$C_{BOOST}$		0.1	
$C_{LOAD}$		150	
Analog Inputs		0 V to $V_{CC} - 2$ V	V
Digital Inputs		0 V to $V_{CC}$	
Reference Voltage Output Current		0 to 2.5	mA

<b>SPECIFICATIONS<sup>a</sup></b>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{\text{NOM}} = 500 \text{ kHz}$ , $V_{\text{IN}} = 72 \text{ V}$ $V_{\text{INDET}} = 7.2 \text{ V}$ ; $10 \text{ V} \leq V_{\text{CC}} \leq 13.2 \text{ V}$	Limits - 40 to 85 °C			Unit	
			Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>		
<b>Reference (3.3 V)</b>							
Output Voltage	$V_{\text{REF}}$	$V_{\text{CC}} = 12 \text{ V}$ , 25 °C Load = 0 mA	3.2	3.3	3.4	V	
Short Circuit Current	$I_{\text{SREF}}$	$V_{\text{REF}} = 0 \text{ V}$			- 50	mA	
Load Regulation	dVr/dir	$I_{\text{REF}} = 0$ to - 2.5 mA		- 30	- 75	mV	
Power Supply Rejection	PSRR	at 100 Hz		60		dB	
<b>Oscillator</b>							
Accuracy (1 % $R_{\text{OSC}}$ )		$R_{\text{OSC}} = 30 \text{ k}\Omega$ , $f_{\text{NOM}} = 500 \text{ kHz}$	- 20		20	%	
Max Frequency <sup>i</sup>	$F_{\text{MAX}}$	$R_{\text{OSC}} = 22.6 \text{ k}\Omega$	500	625	750	kHz	
Foldback Frequency <sup>d</sup>	$F_{\text{FOBK}}$	$f_{\text{NOM}} = 500 \text{ kHz}$ , $V_{\text{CS2}} - V_{\text{CS1}} > 150 \text{ mV}$		100			
<b>Error Amplifier</b>							
Input Bias Current	$I_{\text{BIAS}}$	$V_{\text{EP}} = 0 \text{ V}$	- 40		- 15	$\mu\text{A}$	
Gain	$A_{\text{V}}$			- 2.2		V/V	
Bandwidth	BW			5		MHz	
Power Supply Rejection	PSRR	at 100 Hz		60		dB	
Slew Rate	SR			0.5		V/ $\mu\text{s}$	
<b>Current Sense Amplifier</b>							
Input Voltage CM Range	$V_{\text{CM}}$	$V_{\text{CS1}} - \text{GND}$ , $V_{\text{CS2}} - \text{GND}$		$\pm 150$		mV	
Input Amplifier Gain	$A_{\text{VOL}}$			17.5		dB	
Input Amplifier Bandwidth	BW			5		MHz	
Input Amplifier Offset Voltage	$V_{\text{OS}}$			$\pm 5$		mV	
CL_CONT Current	$I_{\text{CL\_CONT}}$	$dV_{\text{CS}} = 0$		120		$\mu\text{A}$	
		$dV_{\text{CS}} = 100 \text{ mV}$		0			
		$dV_{\text{CS}} = 170 \text{ mV}$		> 2			mA
Lower Current Limit Threshold	$V_{\text{TLCL}}$	$I_{\text{PD}} = I_{\text{PU}} - I_{\text{CL\_CONT}} = 0$ See Figure 6		100		mV	
Upper Current Limit Threshold	$V_{\text{THCL}}$	$I_{\text{PD}} > 2 \text{ mA}$		150			
Hysteresis		$I_{\text{PU}} < 500 \mu\text{A}$		- 50			
CL_CONT Clamp Level	$C_{\text{L\_CONT}}(\text{min})$	$I_{\text{PU}} = 500 \mu\text{A}$	0.6		1.5	V	
<b>PWM Operation</b>							
Duty Cycle <sup>e</sup>	$D_{\text{MAX}}$	$f_{\text{OSC}} = 500 \text{ kHz}$	$V_{\text{EP}} = 0 \text{ V}$	90	92	95	%
	$D_{\text{MIN}}$		$V_{\text{EP}} = 1.75 \text{ V}$		< 15		
		$V_{\text{CS2}} - V_{\text{CS1}} > 150 \text{ mV}$			3		
<b>Pre-Regulator</b>							
Input Voltage	+ $V_{\text{IN}}$	$I_{\text{IN}} = 10 \mu\text{A}$			72	V	
Input Leakage Current	$I_{\text{LKG}}$	$V_{\text{IN}} = 72 \text{ V}$ , $V_{\text{CC}} > V_{\text{REG}}$			10	$\mu\text{A}$	
Regulator Bias Current	$I_{\text{REG1}}$	$V_{\text{IN}} = 72 \text{ V}$ , $V_{\text{INDET}} < V_{\text{SD}}$		86	200		
	$I_{\text{REG2}}$	$V_{\text{IN}} = 72 \text{ V}$ , $V_{\text{INDET}} > V_{\text{REF}}$		8	14	mA	
Regulator_Comp	$I_{\text{SOURCE}}$	$V_{\text{CC}} = 12 \text{ V}$	- 29	- 19	- 9	$\mu\text{A}$	
	$I_{\text{SINK}}$		50	82	110		
Pre-Regulator Drive Capacity	$I_{\text{START}}$	$V_{\text{CC}} < V_{\text{REG}}$	20			mA	



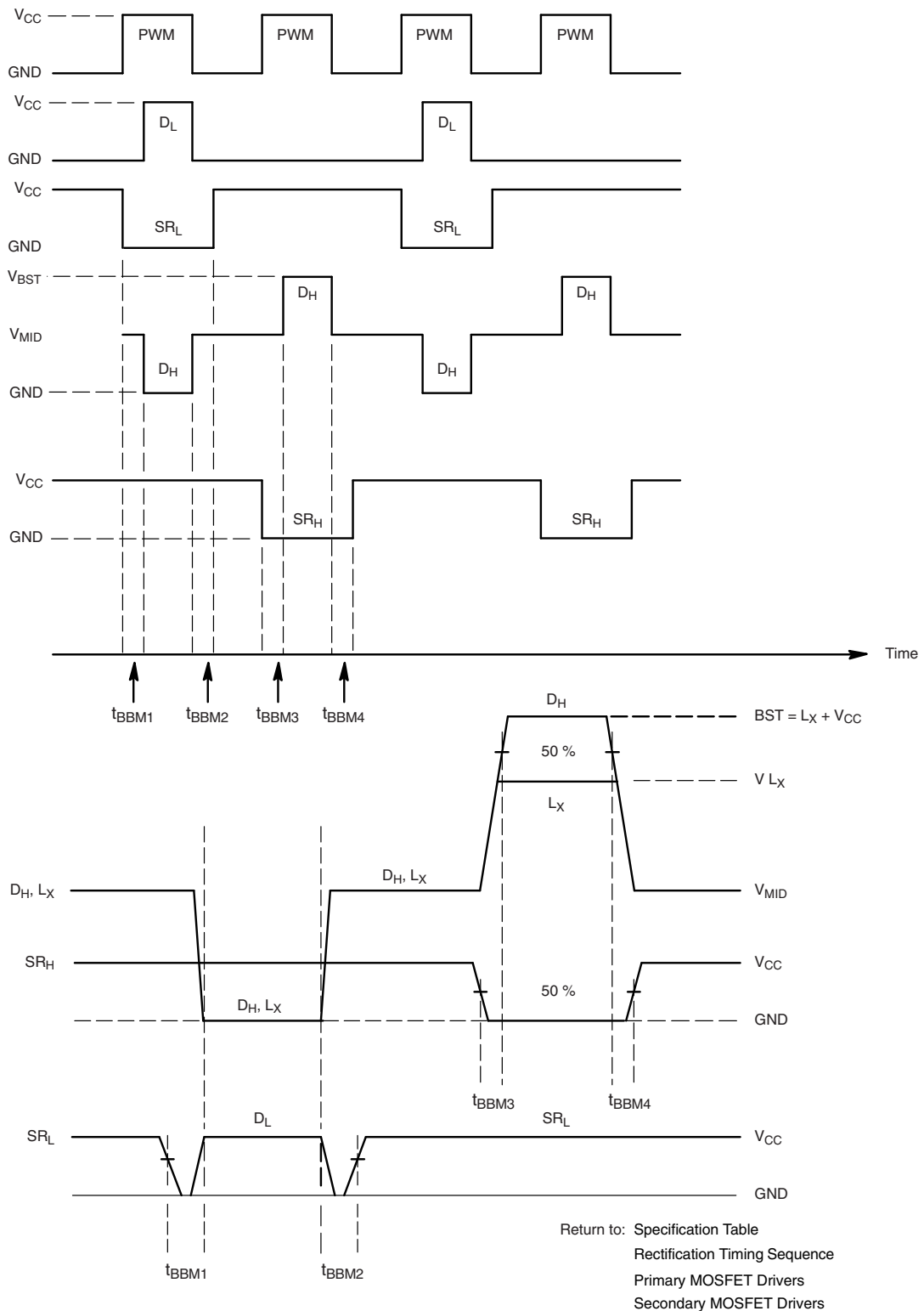
SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 72 \text{ V}$ $V_{INDET} = 7.2 \text{ V}$ ; $10 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$	Limits - 40 to 85 °C			Unit	
			Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>		
<b>Pre-Regulator</b>							
$V_{CC}$ Pre-Regulator Turn Off Threshold Voltage	$V_{REG1}$	$V_{INDET} > V_{REF}$	$T_A = 25 \text{ °C}$	7.4	9.1	10.4	V
	$V_{REG2}$	$V_{INDET} = 0 \text{ V}$		8.5	9.1	9.7	
Undervoltage Lockout	$V_{UVLO}$	$V_{CC}$ Rising	$T_A = 25 \text{ °C}$	7.15	8.8	9.8	
				8.1	8.8	9.3	
$V_{UVLO}$ Hysteresis <sup>9</sup>	$V_{UVLOHYS}$				0.5		
<b>Soft-Start</b>							
Soft-Start Current Output	$I_{SS}$	Start-Up Condition		12	20	28	μA
Soft-Start Completion Voltage	$V_{SS\_COMP}$	Normal Operation		7.35	8.05	8.85	V
<b>Shutdown</b>							
$V_{INDET}$ Shutdown FN	$V_{SD}$	$V_{INDET}$ Rising		350	550	720	mV
$V_{INDET}$ Hysteresis		$V_{INDET}$			200		
<b><math>V_{INDET}</math> Input Threshold Voltages</b>							
$V_{INDET} - V_{IN}$ Under Voltage	$V_{UV}$	$V_{INDET}$ Rising		3.13	3.3	3.46	V
$V_{UV}$ Hysteresis		$V_{INDET}$		0.23	0.3	0.35	
<b>Over Temperature Protection</b>							
Activating Temperature		$T_J$ Increasing			160		°C
De-Activating Temperature		$T_J$ Decreasing			130		
<b>Converter Supply Current (<math>V_{CC}</math>)</b>							
Shutdown	$I_{CC1}$	Shutdown, $V_{INDET} = 0 \text{ V}$		50		350	μA
Switching Disabled	$I_{CC2}$	$V_{INDET} < V_{REF}$		4	8	12	mA
Switching w/o Load	$I_{CC3}$	$V_{INDET} > V_{REF}$ , $f_{NOM} = 500 \text{ kHz}$		5	10	15	
Switching with $C_{LOAD}$	$I_{CC4}$	$V_{CC} = 12 \text{ V}$ , $C_{DH} = C_{DL} = 3 \text{ nF}$ $C_{SRH} = C_{SRL} = 0.3 \text{ nF}$			21		
<b>Output MOSFET DH Driver (High-Side)</b>							
Output High Voltage	$V_{OH}$	Sourcing 10 mA		$V_{BST} - 0.3$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA				$V_{LX} + 0.3$	
Boost Current	$I_{BST}$	$V_{LX} = 72 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$		1.3	1.9	2.7	mA
$L_X$ Current	$I_{LX}$	$V_{LX} = 72 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$		- 1.3	- 0.7	- 0.4	
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10 \text{ V}$			- 1.0	- 0.75	A
Peak Output Sink	$I_{SINK}$			0.75	1.0		
Rise Time	$t_r$	$C_{DL} = 3 \text{ nF}$			35		ns
Fall Time	$t_f$				35		
<b>Output MOSFET DL Driver (Low-Side)</b>							
Output High Voltage	$V_{OH}$	Sourcing 10 mA		$V_{CC} - 0.3$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA				0.3	
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10 \text{ V}$			- 1.0	- 0.75	A
Peak Output Sink	$I_{SINK}$			0.75	1.0		
Rise Time	$t_r$	$C_{DH} = 3 \text{ nF}$			35		ns
Fall Time	$t_f$				35		

SPECIFICATIONS <sup>a</sup>						
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 72 \text{ V}$ $V_{INDET} = 7.2 \text{ V}$ ; $10 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$	Limits - 40 to 85 °C			Unit
			Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>Synchronous Rectifier (SRH, SRL) Drivers</b>						
Output High Voltage	$V_{OH}$	Sourcing 10 mA	$V_{CC} - 0.4$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA			0.4	V
Break-Before-Make Time <sup>f</sup>	$t_{BBM1}$	$T_A = 25 \text{ °C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , See Figure 3		55		ns
	$t_{BBM2}$			40		
	$t_{BBM3}$	$T_A = 25 \text{ °C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , $L_X = 72 \text{ V}$		35		
	$t_{BBM4}$			55		
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10 \text{ V}$		- 100		mA
Peak Output Sink	$I_{SINK}$			100		
Rise Time	$t_r$	$C_{SRH} = C_{SRL} = 0.3 \text{ nF}$		35		ns
Fall Time	$t_f$			35		
<b>Voltage Mode</b>						
Error Amplifier	$t_{d1DH}$	Input to High-Side Switch Off		< 200		ns
	$t_{d2DL}$	Input to Low-Side Switch Off		< 200		
<b>Current Mode</b>						
Current Amplifier	$t_{d3DH}$	Input to High-Side Switch Off		< 200		ns
	$t_{d4DL}$	Input to Low-Side Switch Off		< 200		

## Notes:

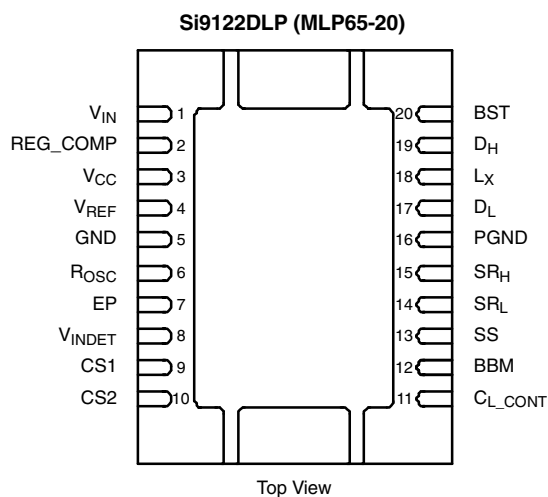
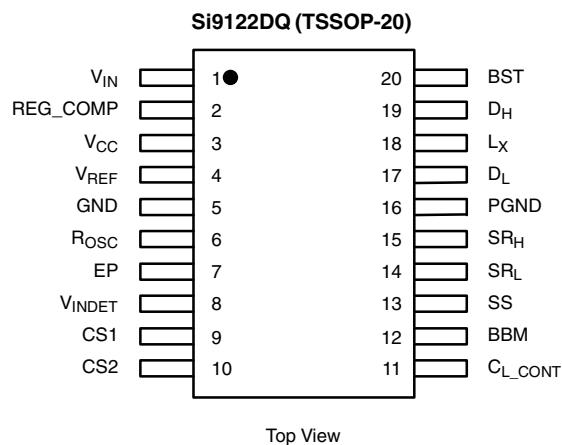
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (- 40 °C to 85 °C).
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $F_{MIN}$  when  $V_{CL\_CONT}$  at clamp level. Typical foldback frequency change + 20 %, - 30 % over temperature.
- Measured on SRL or SRH outputs.
- See figure 3 for Break-Before-Make time definition.
- $V_{UVLO}$  tracks  $V_{REG1}$  by a diode drop.
- $C_{BBM}$  may be required to reduce noise into BBM pin for non-optimum layout.
- Guaranteed by design and characterization, not tested in production.

**TIMING DIAGRAM FOR MOS DRIVERS**



**Figure 3.**

## PIN CONFIGURATION



## ORDERING INFORMATION

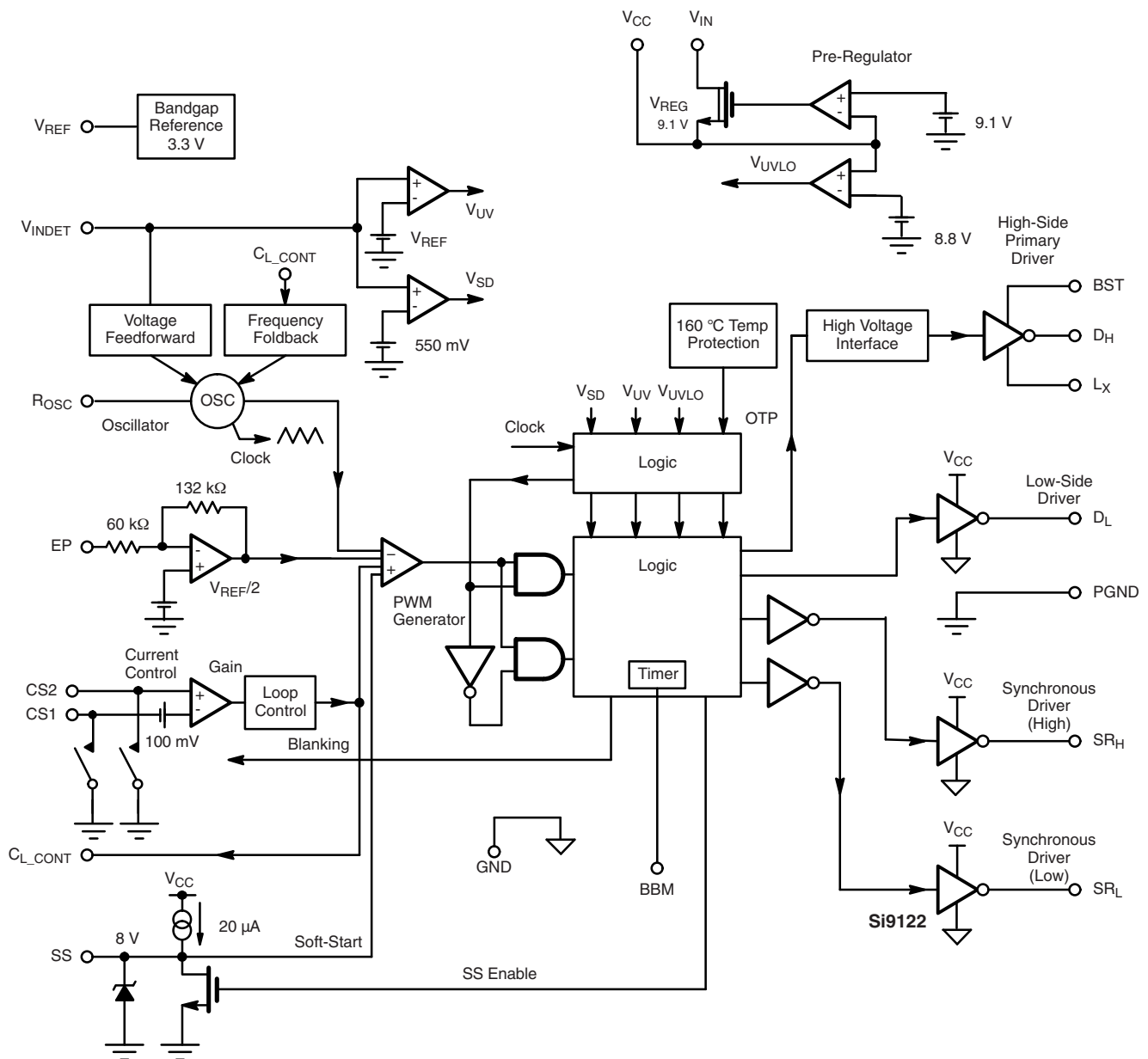
Lead (Pb)-free Part Number	Temperature Range	Package
Si9122DQ-T1-E3	- 40 °C to 85 °C	TSSOP-20
Si9122DLP-T1-E3		MLP65-20

Eval Kit	Temperature Range	Board Type
Si9122DB Issue 3	- 10 °C to 70 °C	Surface Mount and Thru-Hole

## PIN DESCRIPTION

Pin Number	Name	Function
1	$V_{IN}$	Input supply voltage for the start-up circuit
2	REG_COMP	Control signal for an external pass transistor
3	$V_{CC}$	Supply voltage for internal circuitry
4	$V_{REF}$	3.3 V reference, decoupled with 1 $\mu$ F capacitor
5	GND	Ground
6	$R_{OSC}$	External resistor connection to oscillator
7	EP	Voltage control input
8	$V_{INDET}$	$V_{IN}$ under voltage detect and shutdown function input. Shuts down or disables switching when $V_{INDET}$ falls below preset threshold voltages and provides the feed forward voltage.
9	CS1	Current limit amplifier negative input
10	CS2	Current limit amplifier positive input
11	$C_{L\_CONT}$	Current limit compensation
12	BBM	Programmable break-before-make time connection to an external resistor to set time delay
13	SS	Soft-start control - external capacitor connection
14	SR <sub>L</sub>	Signal transformer drive, sequenced with the primary side
15	SR <sub>H</sub>	Signal transformer drive, sequenced with the primary side
16	PGND	Power ground
17	D <sub>L</sub>	Low-side gate drive signal - primary
18	L <sub>X</sub>	High-side source and transformer connection node
19	D <sub>H</sub>	High-side gate drive signal - primary
20	BST	Bootstrap voltage to drive the high-side N-Channel MOSFET switch




**Figure 4. Detailed Functional Block**

## DETAILED OPERATION

### Start-Up

When  $V_{INEXT}$  rises above 0 V, the internal pre-regulator begins to charge up the  $V_{CC}$  capacitor. Current into the external  $V_{CC}$  capacitor is limited to typically 40 mA by the internal DMOS device. When  $V_{CC}$  exceeds the UVLO voltage of 8.8 V a soft-start cycle of the switch mode supply is initiated. The  $V_{CC}$  supply continues to be charged by the pre-regulator until  $V_{CC}$  equals  $V_{REG}$ . During this period, between  $V_{UVLO}$  and  $V_{REG}$ , excessive load current will result in  $V_{CC}$  falling below  $V_{UVLO}$  and stopping switch mode operation. This situation is avoided by the hysteresis between  $V_{REG}$  and  $V_{UVLO}$  and correct sizing of the  $V_{CC}$

capacitor, bootstrap capacitor and the soft-start capacitor. The value of the  $V_{CC}$  capacitor should therefore be chosen to be capable of maintaining switch mode operation until the  $V_{CC}$  can be supplied from the external circuit (e.g via a power transformer winding and zener regulator). Feedback from the output of the switch mode supply charges  $V_{CC}$  above  $V_{REG}$  and fully disconnects the pre-regulator, isolating  $V_{CC}$  from  $V_{IN}$ .  $V_{CC}$  is then maintained above  $V_{REG}$  for the duration of switch mode operation. In the event of an over voltage condition on  $V_{CC}$ , an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND.

Care needs to be taken if there is a delay prior to the external circuit feeding back to the  $V_{CC}$  supply. To prevent excessive power dissipation within the IC it is advisable to use an external PNP device. A pin has been incorporated on the IC, (REG\_COMP) to provide compensation when employing the external device. In this case the  $V_{IN}$  pin is connected to the base of the PNP device and controls the current, while the REG\_COMP pin determines the frequency compensation of the circuit. The value of the REG\_COMP capacitor cannot be too big, otherwise it will slow down the response of the pre-regulator in the case that fault situations occur and pre-regulator needs to be turned on again. To understand the operation please refer to Figure 5.

The soft-start circuit is designed for the dc-dc converter to start-up in an orderly manner and reduce component stress on the IC. This feature is programmable by selecting an external  $C_{SS}$ . An internal 20  $\mu$ A current source charges  $C_{SS}$  from 0 V to the final clamped voltage of 8 V. In the event of UVLO or shutdown,  $V_{SS}$  will be held low ( $< 1$  V) disabling driver switching. To prevent oscillations, a longer soft-start time may be needed for high capacitive loads and high peak output current applications.

#### Reference

The reference voltage of Si9122 is set at 3.3 V. The reference voltage is de-coupled externally with 0.1  $\mu$ F capacitor. The  $V_{REF}$  voltage is 0 V in shutdown mode and has 50 mA source capability.

#### Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. Voltage feed forward is also included to take account of variations in supply voltage  $V_{IN}$ .

In the half-bridge topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side. The error information is thus passed to the power controller through an opto-coupling device. This information is inverted, hence 0 V represents the maximum duty cycle, whilst 2 V represents minimum duty cycle. The error information enters the IC via pin EP, and is passed to the PWM generator via an inverting amplifier. The relationship between Duty cycle and  $V_{EP}$  is shown in the Typical Characteristic Graph, Duty Cycle vs.  $V_{EP}$  25 °C, page 12. Voltage feedforward is implemented by taking the attenuated  $V_{IN}$  signal at  $V_{INDET}$  and directly modulating the duty cycle. The relationship between Duty cycle and  $V_{INDET}$  is shown in the Typical Characteristic Graph, Duty Cycle vs.  $V_{INDET}$ , page 16.

At start-up, i.e., once  $V_{CC}$  is greater than  $V_{UVLO}$ , switching is initiated under soft-start control which increases primary switch on-times linearly from  $D_{MIN}$  to  $D_{MAX}$  over the soft-start period. Start-up from a  $V_{INDET}$  power down is also initiated under soft-start control.

#### Half-Bridge and Synchronous Rectification Timing Sequence

The PWM signal generated within the Si9122 controls the low and high-side bridge drivers on alternative cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 1.2 V and PWM controlled switching begins. The first bridge driver to switch is always the low-side,  $D_L$  as this allows charging of the high-side boost capacitor.

The timing and coordination of the drives to the primary and secondary stages is very important and shown in Figure 3. It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high or the low-side switch are active. In this situation the transformer would effectively be presented with a short across the output. To avoid this, a dedicated break-before-make circuit is included which will generate non overlapping waveforms for the primary and the secondary drive signals. This is achieved by a programmable timer which delays the switching on of the primary driver relative to the switching off of the related secondary and subsequently delays the switching on of the secondary relative to the switching off of the related primary.

Typical variation in the  $t_{BBM3}$  and  $t_{BBM4}$  delay with  $L_X$  voltage is shown in graphs  $t_{BBM3}$ ,  $t_{BBM4}$  and for  $R_{BBM} = 33$  k $\Omega$ . This is due to a reduction in propagation delay through the high-side driver path as the  $L_X$  voltage increases and must be considered in setting the delay for the system level design. Variation of BBM time with  $R_{BBM}$  is shown in graph  $t_{BBM1}$  to  $t_{BBM4}$  vs.  $R_{BBM}$ .

#### Primary High- and Low-Side MOSFET Drivers

The drive voltage for the low-side MOSFET switch is provided directly from  $V_{CC}$ . The high-side MOSFET however requires the gate voltage to be enhanced above  $V_{IN}$ . This is achieved by bootstrapping the  $V_{CC}$  voltage onto the  $L_X$  voltage (the high-side MOSFET source). In order to provide the bootstrapping an external diode and capacitor are required as shown on the application schematic. The capacitor will charge up after the low-side driver has turned on. The switch gate drive signals  $D_H$  and  $D_L$  are shown in Figure 3.

#### Secondary MOSFET Drivers

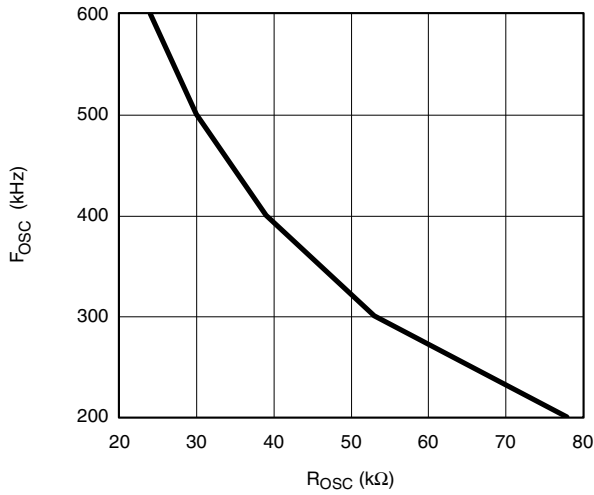
The secondary side MOSFETs are driven from the Si9122 via a center tapped pulse transformer and inverter drivers. The waveforms from the IC SRH and SRL are shown in Figure 3. Of importance is the relative voltage between SRH and SRL, i.e. that which is presented across the primary of the pulse transformer. When both potentials of SRL and SRH are equal then by the action of the inverting driver both secondary MOSFETs are left on.

#### Oscillator

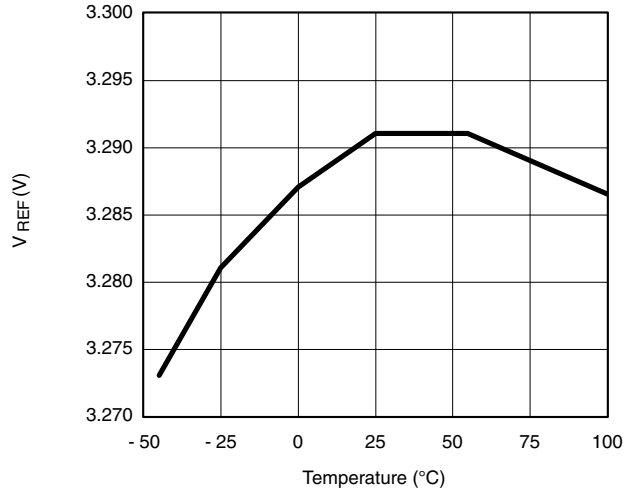
The oscillator is designed to operate at a nominal frequency of 500 kHz. The 500 kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore the switching frequency is programmable by attaching a resistor to the  $R_{OSC}$  pin. Under overload



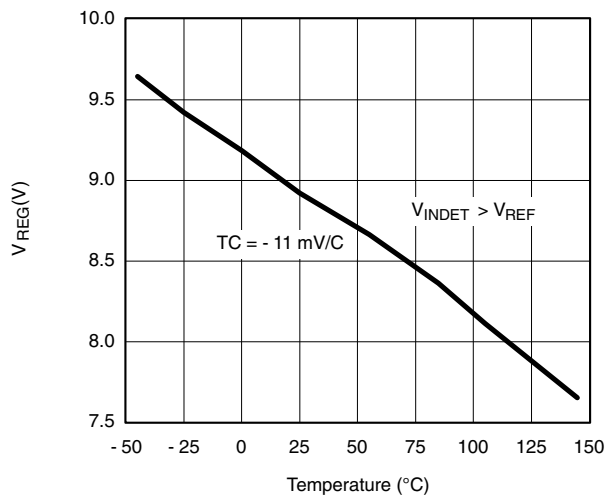
**TYPICAL CHARACTERISTICS**



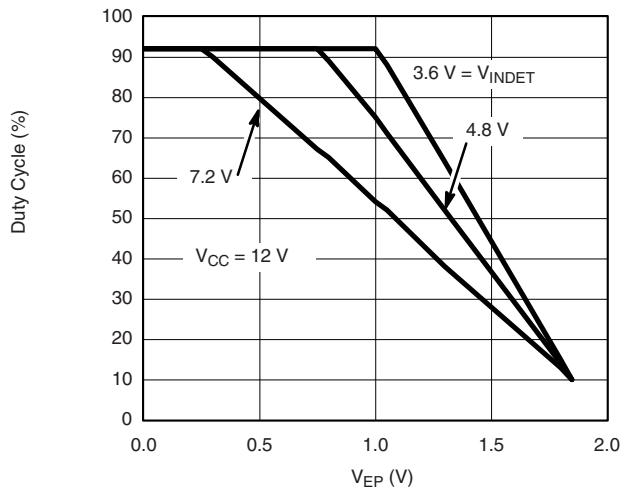
Fosc vs. Rosc at V<sub>CC</sub> = 12 V



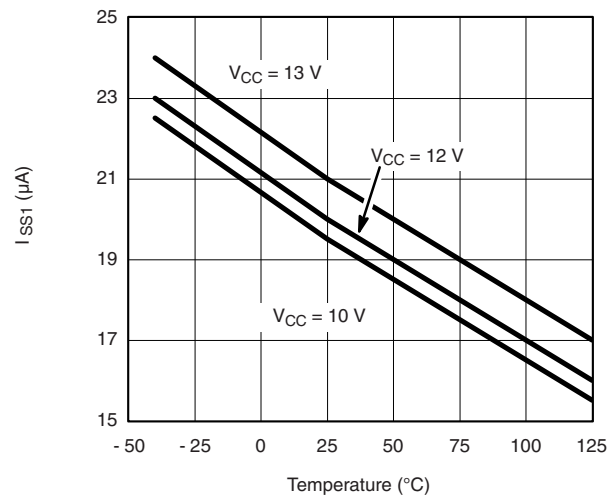
V<sub>REF</sub> vs. Temperature, V<sub>CC</sub> = 12 V



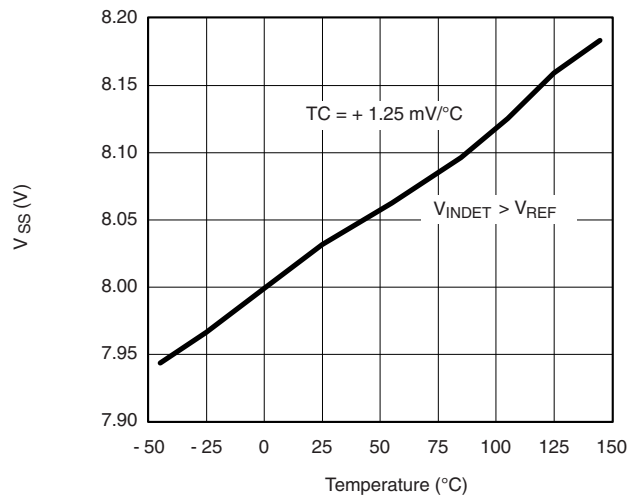
V<sub>REG</sub> vs. Temperature, V<sub>IN</sub> = 48 V



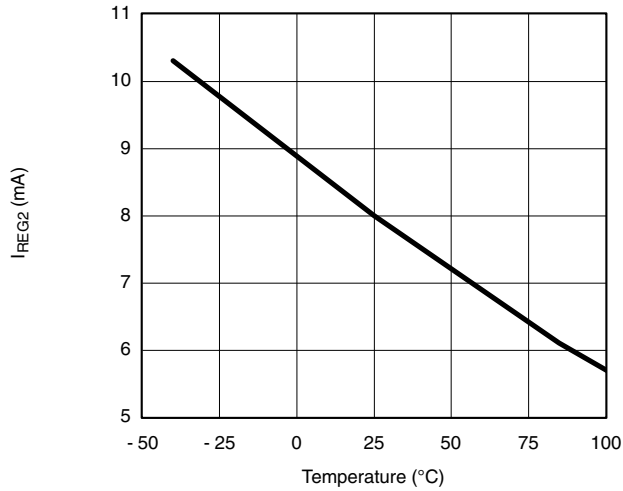
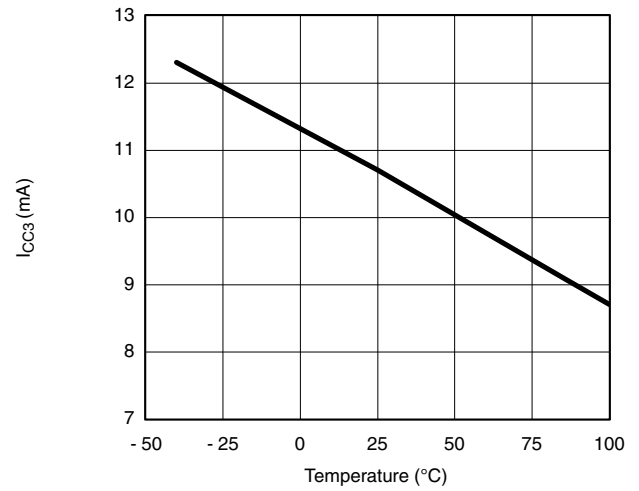
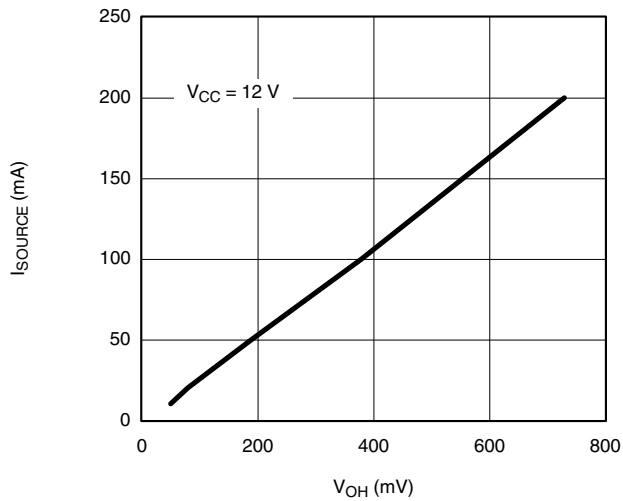
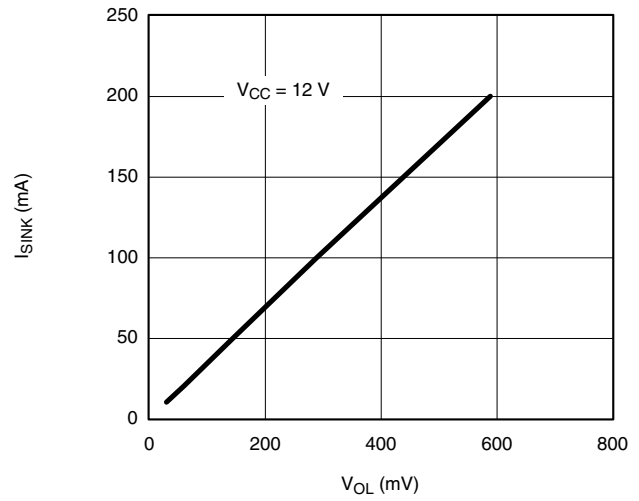
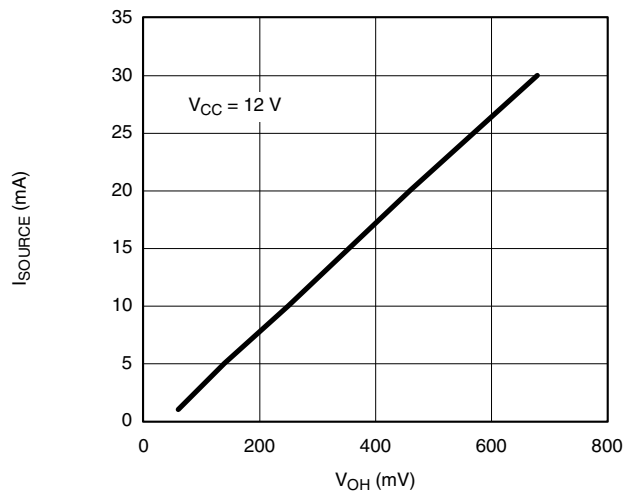
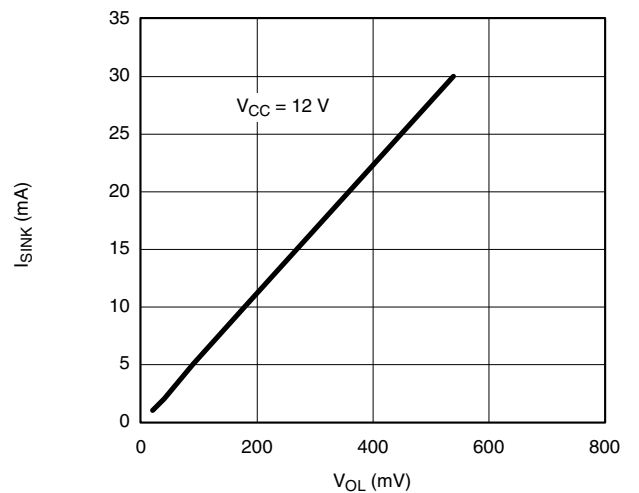
SRL, SRH Duty Cycle vs. V<sub>EP</sub>



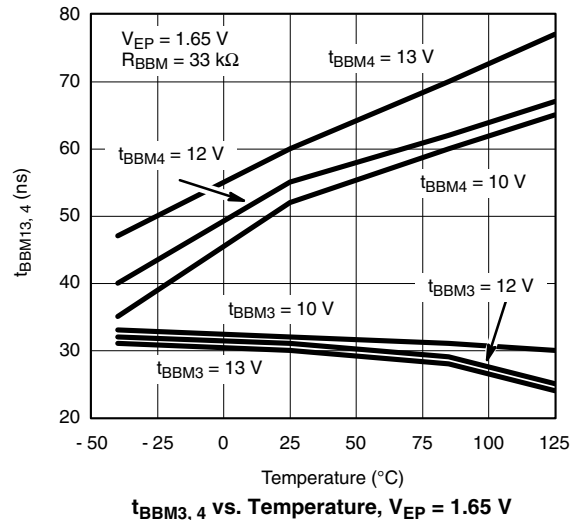
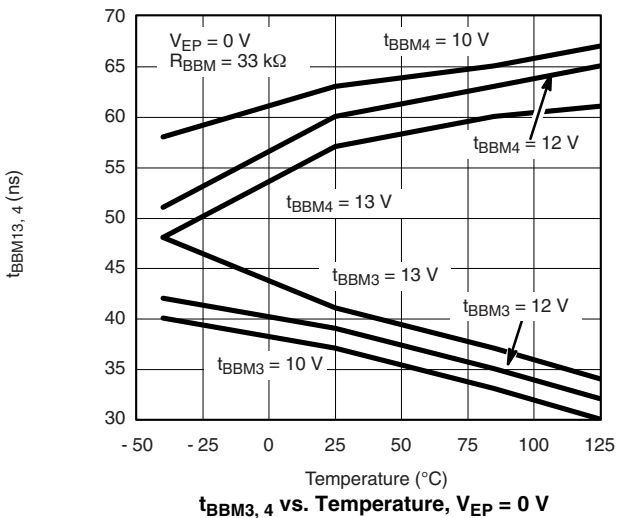
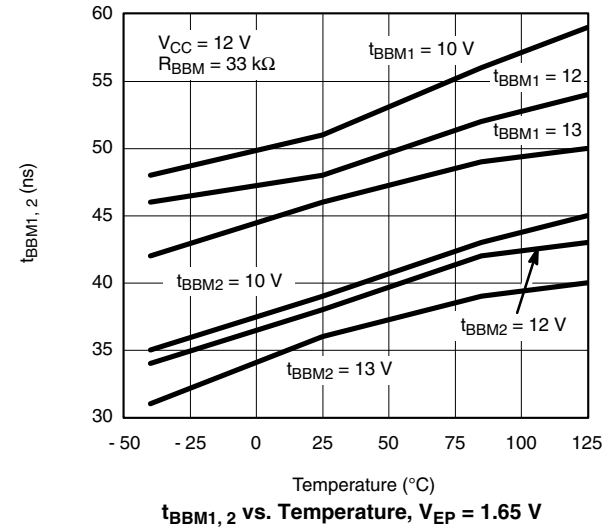
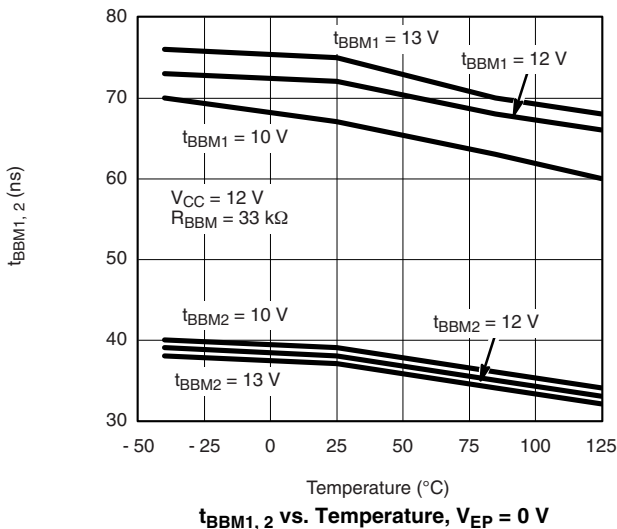
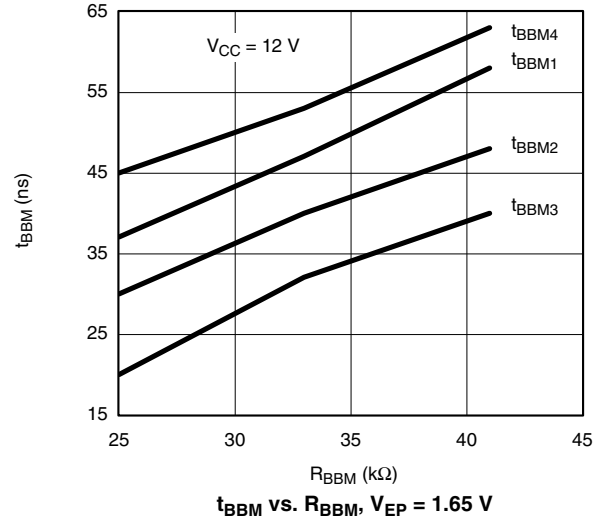
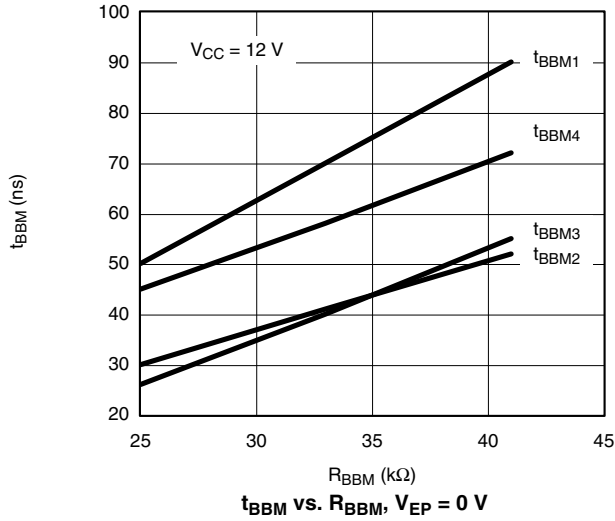
I<sub>SS</sub> vs. Temperature

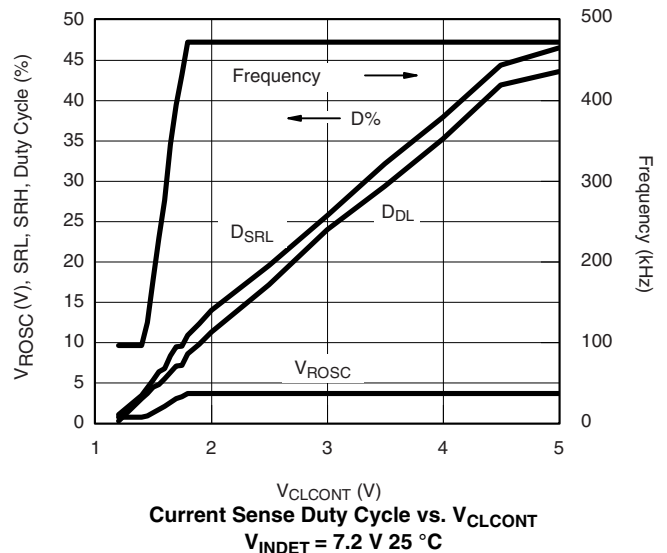
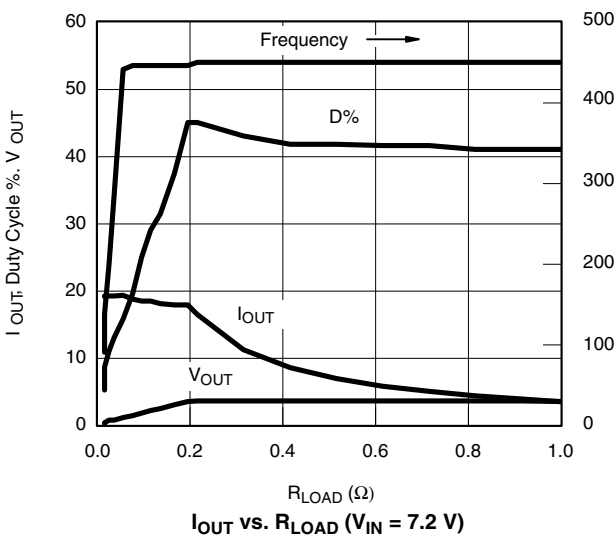
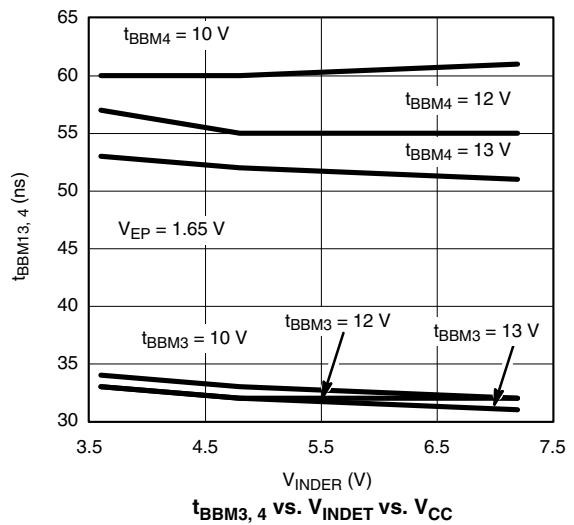
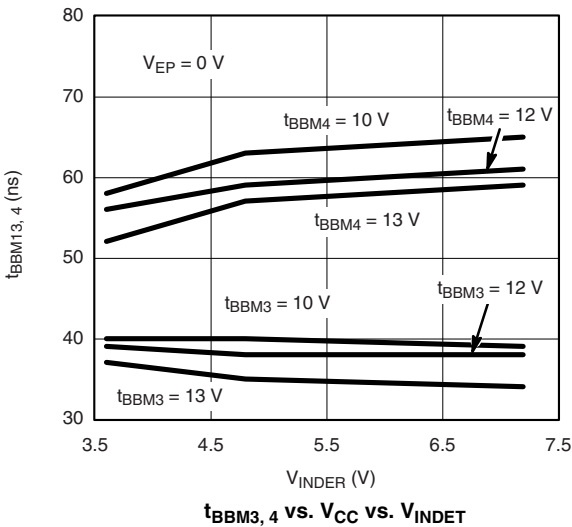
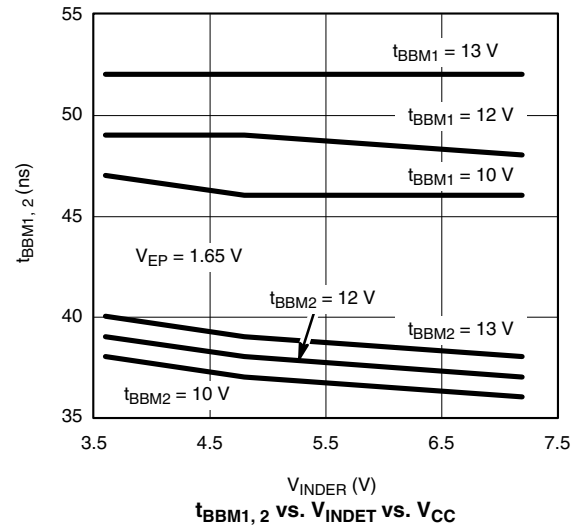
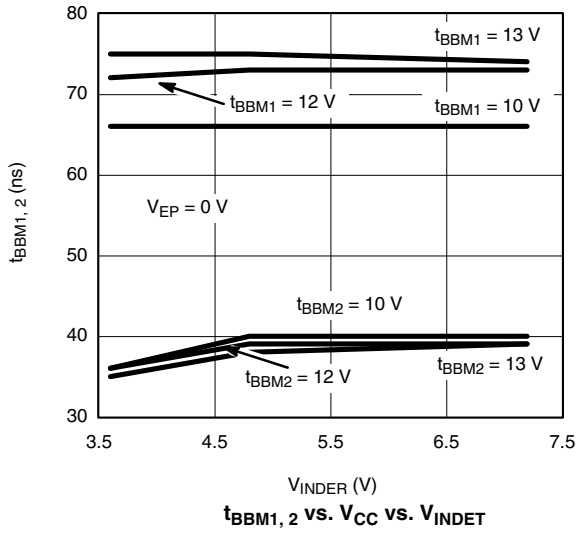


V<sub>SS</sub> vs. Temperature, V<sub>CC</sub> = 12 V

**TYPICAL CHARACTERISTICS**

**I<sub>REG2</sub> vs. Temperature**

**I<sub>CC3</sub> vs. Temperature**

**D<sub>H</sub>, D<sub>L</sub> I<sub>SOURCE</sub> vs. V<sub>OH</sub>**

**D<sub>H</sub>, D<sub>L</sub> I<sub>SINK</sub> vs. V<sub>OL</sub>**

**S<sub>RL</sub>, S<sub>RH</sub> I<sub>SOURCE</sub> vs. V<sub>OH</sub>**

**S<sub>RL</sub>, S<sub>RH</sub> I<sub>SINK</sub> vs. V<sub>OL</sub>**

**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS**


**TYPICAL WAVEFORMS**

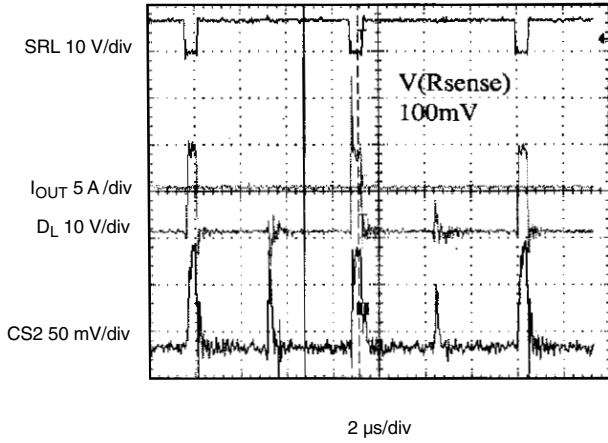


Figure 7. Foldback Mode,  $R_L = 0.02 \Omega$

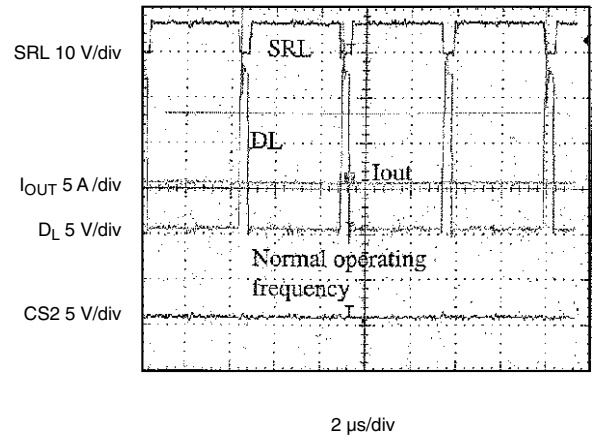


Figure 8. Normal Mode,  $R_L = 0.1 \Omega$

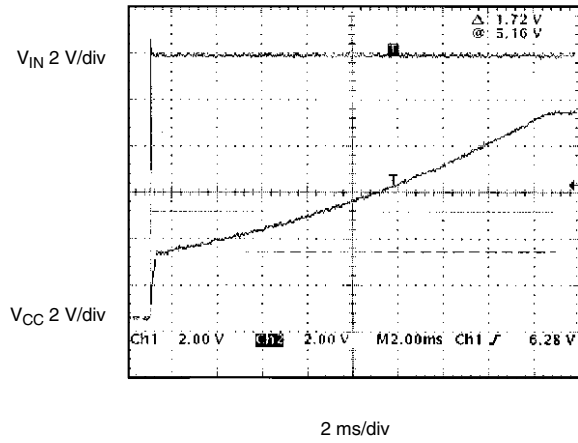


Figure 9.  $V_{CC}$  Ramp-Up

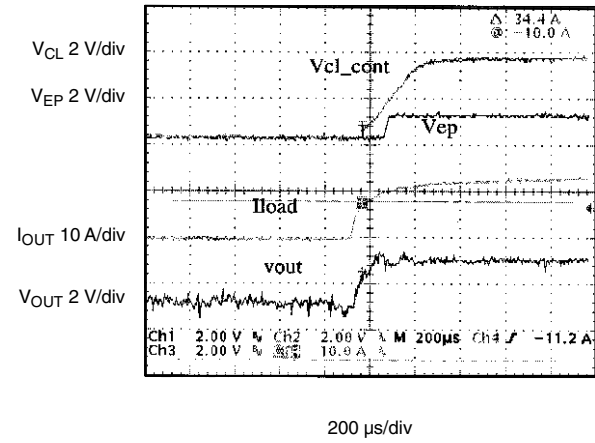


Figure 10. Overload Recovery - Minimum Overshoot

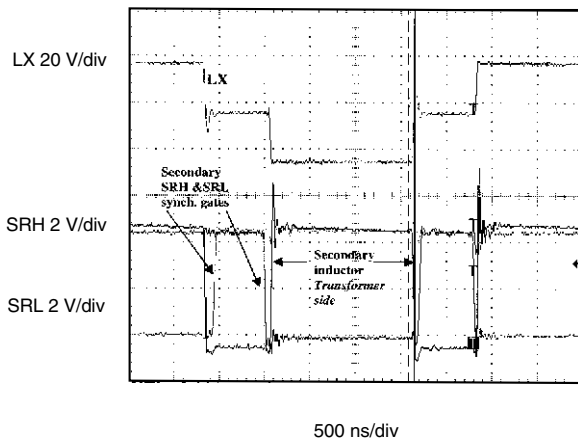


Figure 11. Effective BBM - Measured On Secondary

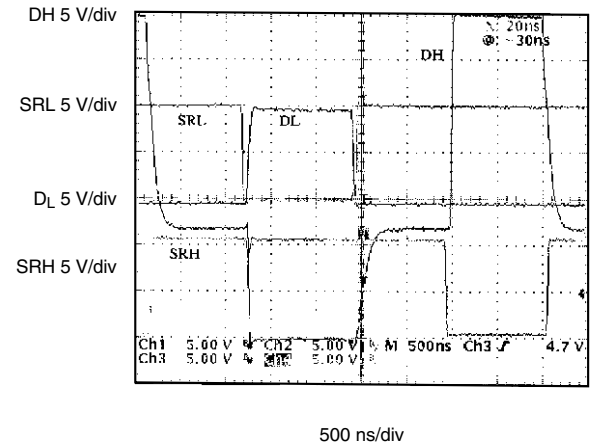
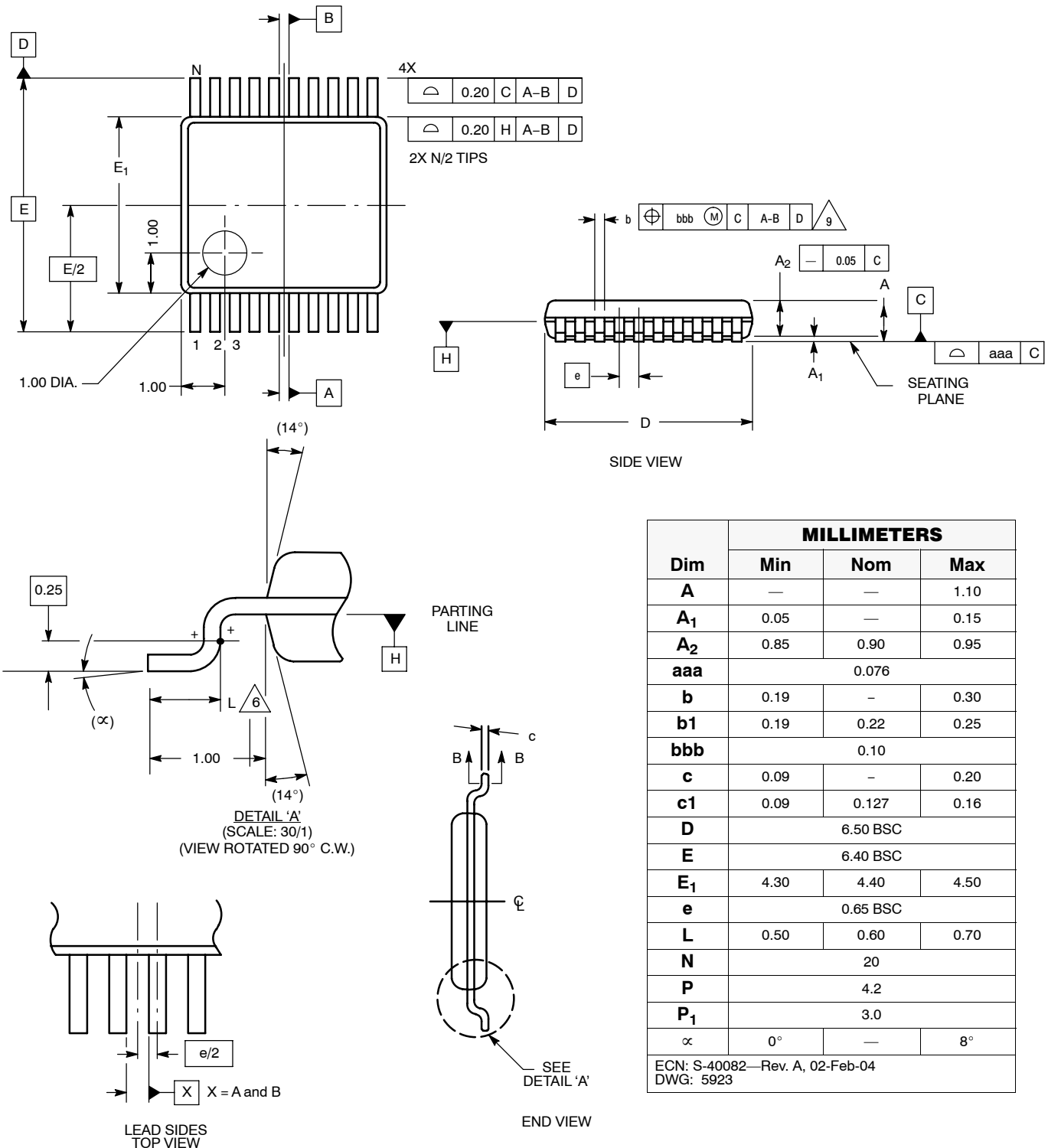


Figure 12. Drive Waveforms

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71815>.

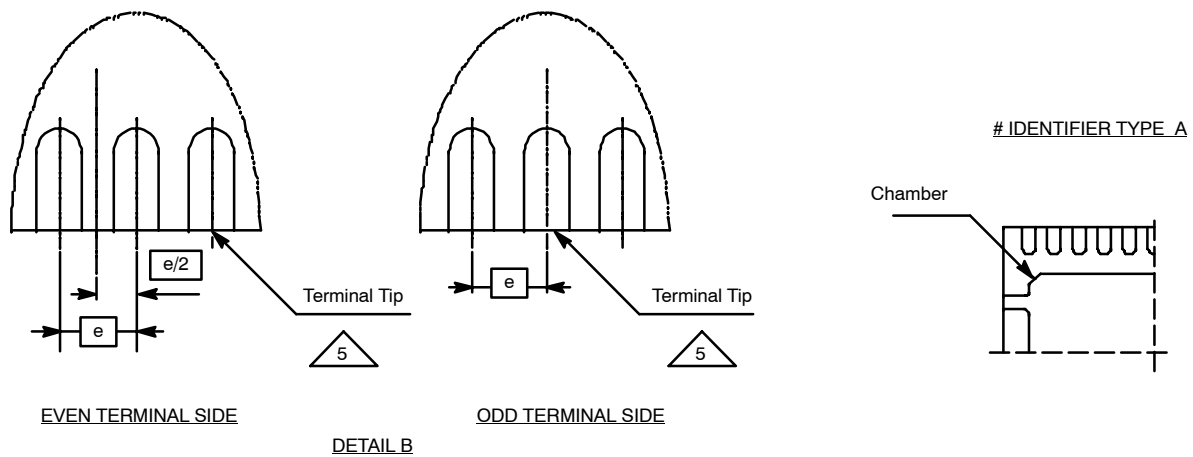
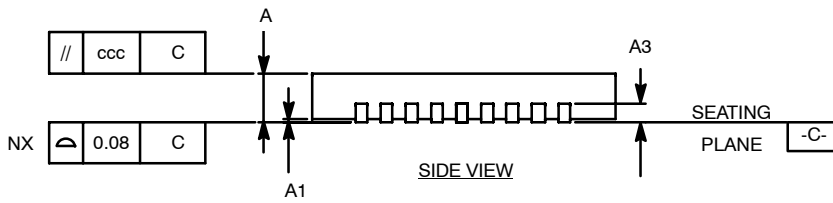
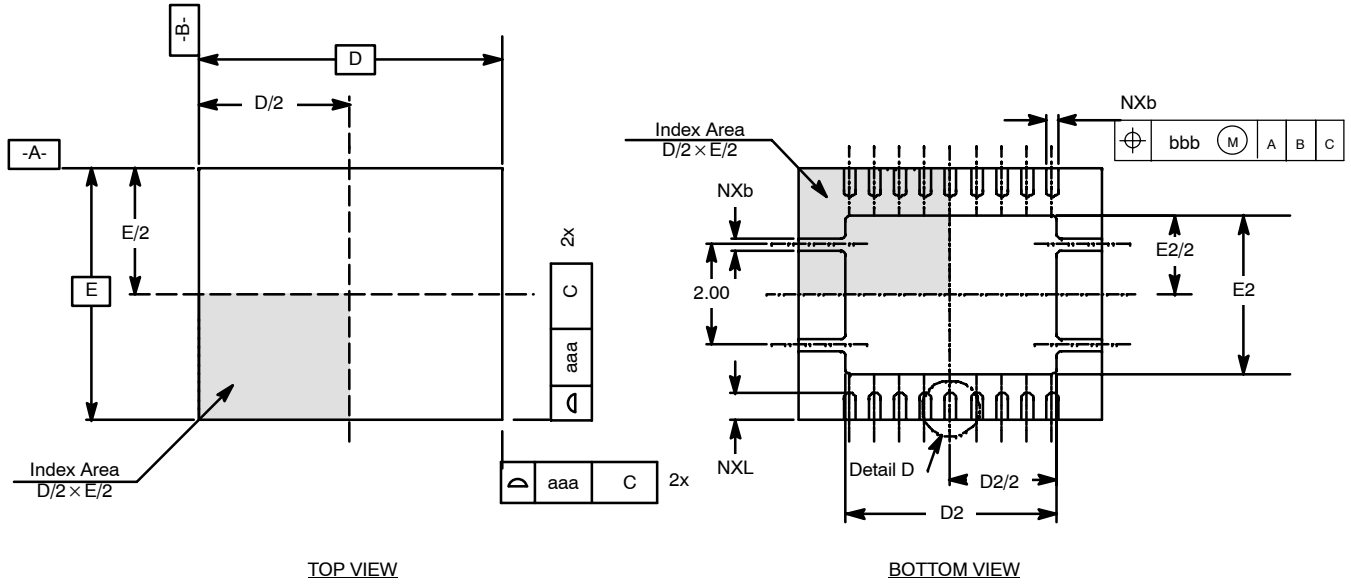


### TSSOP: 20-LEAD (POWER IC ONLY)





PowerPAK® MLP65-18/20 (POWER IC ONLY)





### PowerPAK MLP65-18/20 (POWER IC ONLY)

**N = 18/20 PITCH: 0.5 mm, BODY SIZE: 6.00 x 5.00**

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.031	0.035	0.039	1, 2
A1	0.00	0.02	0.05	0.000	0.001	0.002	1, 2
A2	0.00	0.65	1.00	0.000	0.003	0.004	1, 2
A3	0.20 REF			0.008 REF			
aaa	-	0.15	-	-	0.006	-	
b	0.18	0.25	0.30	0.007	0.010	0.012	8
bbb	-	0.10	-	-	0.004	-	
C'	-	0.225	-	-	0.009	-	4, 10
ccc	-	0.10	-	-	0.004	-	
D	6.00 BSC			0.236 BSC			1, 2
D2	4.00	4.15	4.25	0.157	1.63	0.167	1, 2
E	5.00 BSC			0.197 BSC			1, 2
E2	3.00	3.15	3.25	0.118	0.124	0.128	1, 2
e	-	0.50	-	-	0.020	-	
L	0.45	0.55	0.65	0.018	0.022	0.026	1, 2
N	18, 20			18, 20			1, 2
ND(18)	9			9			1, 2
NE(18)	0			0			1, 2
ND(20)	10			10			1, 2
NE(20)	0			0			1, 2

\* Use millimeters as the primary measurement.

ECN: S-41946—Rev. A, 18-Oct-04  
DWG: 5939

#### NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JEDEC publication 95 SSP-022. Details of terminal #1 identifier are optional, but must be located within the zone indicated. A dot can be marked on the top side by pin 1 to indicate orientation.
5. ND and NE refer to the number of terminals on the D and E side respectively.
6. Depopulation is possible in a symmetrical fashion.
7. NJR refers to NON JEDEC REGISTERED.
8. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
9. Coplanarity applies to the exposed heat slug as well as the terminal.
10. The 45° chamfer dimension C' is located by pin 1 on the bottom side of the package.



## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.