SC1894 Hardware Design Guide

User Guide

UG6344; Rev 2.0; 10/16

Abstract

This document provides PCB design guidelines and circuit-optimization techniques to simplify the hardware integration of the SC1894.

Table of Content

List of Tables

List of Figures

1. Introduction

1.1. Scope

This document provides PCB design guidelines and circuit optimization techniques to enable the designer to implement successful, right-the-first-time SC1894 hardware integration. This ensures fast and trouble-free circuit optimization, using the same techniques used for the SC1894 reference design, which has been thoroughly validated over the SC1894 data sheet limits to achieve optimum performance.

The first sections of this document describe the SC1894 reference design (see Section 2.2 and 3).

The remaining sections are organized to address all design/layout topics in order of priority. The designer should follow the flow described below to ensure optimum integration:

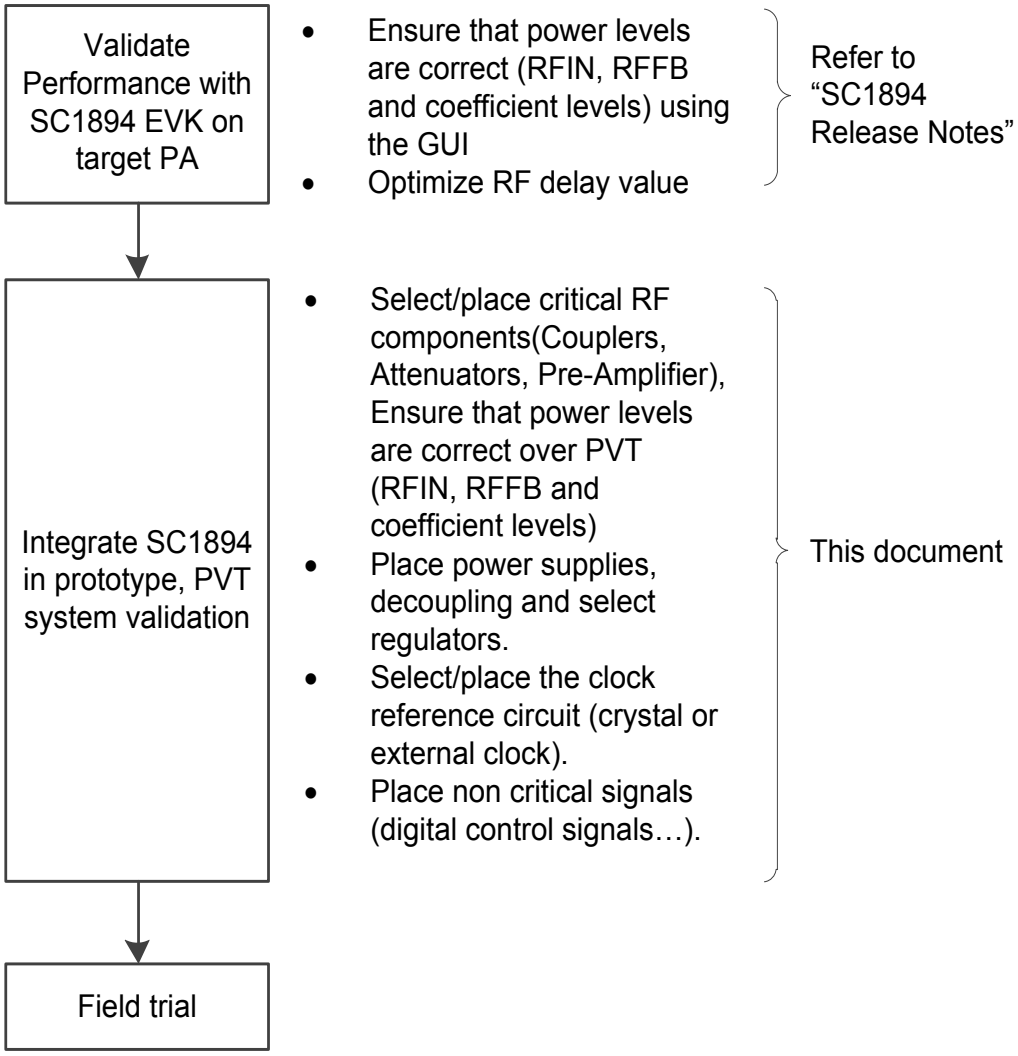


Figure 1. SC1894 integration flow.

1.2. Revision History

Revision	Date	Description
1.0	September 2012	Original document
1.1	October 2012	Added SPI Connector for Multi-RFPAL Operation Updated Crystal XO Specs Fixed External Clock Phase Noise Spec Added Checkered Pattern GND Layout for Delay Line Updated Frequency Range of EVK1500 Edited Multi-RFPAL Power-Supply Section
1.2	May 2013	Added URL for Link Budget Calculator Updated Input Voltage Range of all ADCs as 1.8V Clarified Analog Voltage Monitoring Functions on EVB (External Power and Temperature Detectors) Updated MGPOUT Section for Firmware 4.1 Kyocera DL246 Reliability Issues Updated STATO Pin description Specific Requirements for 1894 - 00, - 13 and - 23
1.3	August 2014	Updated for FW 4.1.03.08 Release to reflect merger of all bundles. Fixed errors in SC1894_DB200A and SC1894_DB500A schematic with RFOUT coupler incorrect connections (PCB was correct, but schematic was wrong). Updated schematic and layouts to use Maxim Integrated Logo. Power Consumption Updated for 4.1 firmware. 3ns Anaren and RN2 Delay Line Reference Corrected Interface Connector Pin-Out (DGPINO1, DGPINO0) Updated Pull-Up and Down Resistor Values
1.4	October 2014	Delay Line DL246 End Of Life (EOL). See Section 7.6, Footnote 1
1.5	December 2014	Changed ADC and DAC functions to “design support” status; these functions remain active but are not tested in production.
2.0	October 2016	Initial Release to web. General edits to remove requirement for NDA to access SC1894 collateral. Added recommendations for Anaren 3ns delay line. Kyocera delay line DL246 was replaced by DL246A from Richardson RFPD. Removed sections on features no longer supported. Updated spurious and noise performance section.

1.3. Acronyms

Acronyms	Description
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BALUN	Balanced to Unbalanced
CAL	FW mode: Calibration
CW	Continuous Wave
DAC	Digital-to-Analog Converter
EEPROM	Electrically Erasable, Programmable, Read-Only Memory
EM	Electromagnetic
ESR	Equivalent Series Resistance
EVB	Evaluation Board
EVK	Evaluation Kit (Includes EVB, Layout, GUI, BOM)
FSA	FW mode: Full Speed Adaptation
FW	Firmware
GPIO	General Purpose Input/Output
GUI	Graphic User Interface (Software to operate RFPAL)
LO	Local Oscillator
NTC	Negative Temperature Compensation
PMU	Power Measurement Unit (accurate power detector)
POR	Power-On-Reset
PVT	Process, Voltage and Temperature
RF	Radio Frequency
RFFB	RF Feedback
RFIN	RF Input
RFOUT	RF Output
RFPAL	RF PA Linearizer
SPI	Serial Peripheral Interface
SSN	SPI Slave Select Enable
XTAL	Crystal
WDT	Watch Dog Timer

2. References

[1] SC1894 Data Sheet
[2] Anaren 3ns RF Delay (XDL15-3-030S) Data Sheet
[3] Anaren 2ns RF Delay (XDL15-2-020S) Data Sheet
[4] Enpirion Regulator EP5358 Data Sheet
[5] Recommended reflow profile for Pb-Free Solder Paste
[6] SC1894 SPI Programming Guide
[7] SC1894 Firmware Release Notes
[8] DL246A RF Delay (Richardson RFPD) Data Sheet. Not recommended.

3. SC1894 Reference Designs

The SC1894 reference design contains all circuitry necessary for linearization and accurate power detection, including power-supply regulation from 5V DC. The PCB uses a single-side four-layer FR4 design, ideally suited for cost sensitive RF applications. The reference board block diagram is shown in **Figure 2** for SC1894. The pin configuratoin and photograph are shown in **Figure 3**.

Both RFIN and RFOUT couplers are connected to the SC1894 using a BALUN and differential matching network for best common-mode noise rejection. The RFIN signal is sampled with the Input directional coupler and converted to a differential signal by the BALUN. A matching network adapts the BALUN impedance to the SC1894 differential port's complex impedance. The SC1894 generates a correction function based on the RFIN signal and injects it through the RFOUT coupler (refer to the SC1894 data sheet for power range limits of RFIN and RFFB ports).

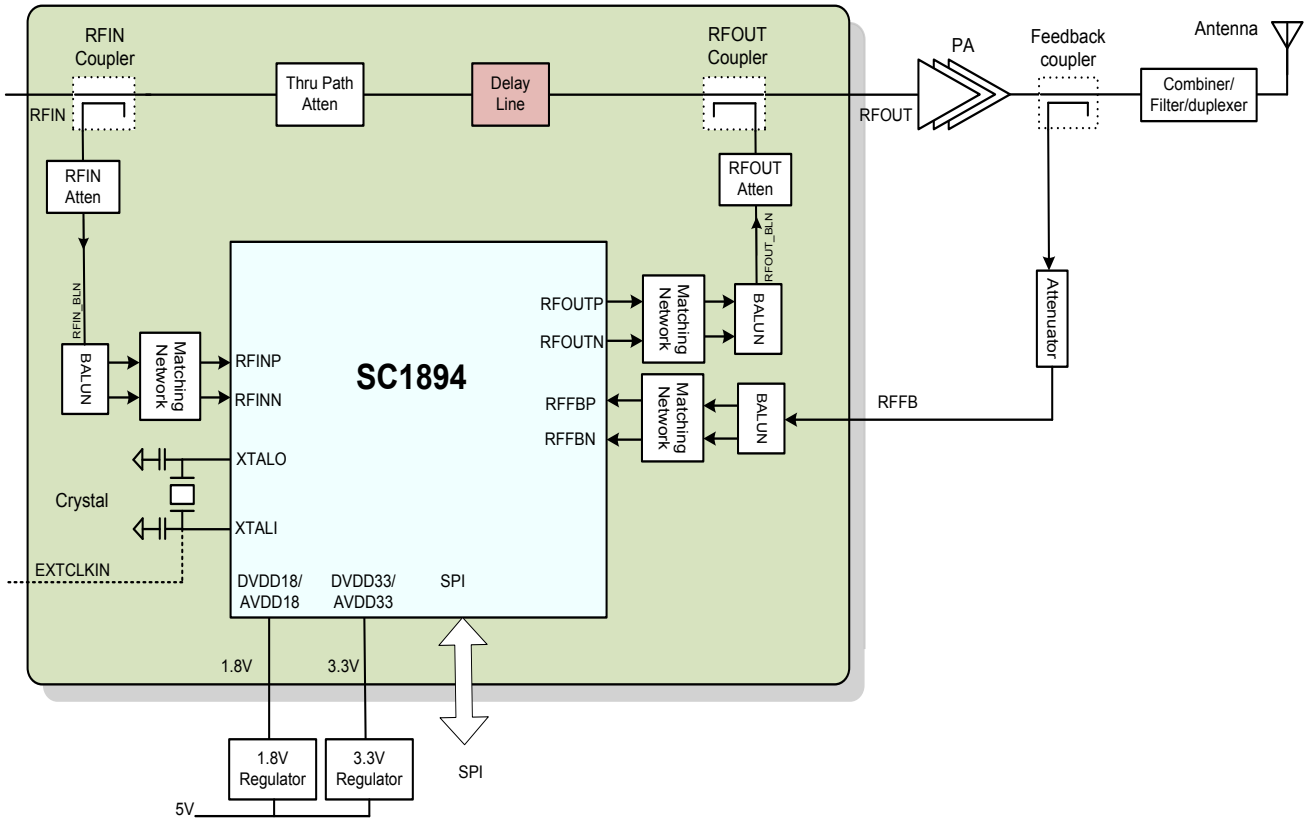


Figure 2. SC1894 reference design block diagram.

The linearizer uses the RFFB signal (coupled from PA output) to adaptively determine the nonlinear characteristics of the PA at any given average- and peak-power level, center frequency, and signal bandwidth. This feedback signal (RFFB) from the PA output is analyzed in the frequency domain to generate a spectrally resolved linearity metric used for the adaptation cost function. It is also used to measure accurate absolute power.

A clock input (EXTCLKIN) permits driving the SC1894 with an external clock, hence saving on the resonating element (crystal resonator) PCB area and cost (Section 9).

The SC1894 main supply/ground simplified circuits are described in Appendix 13.1.

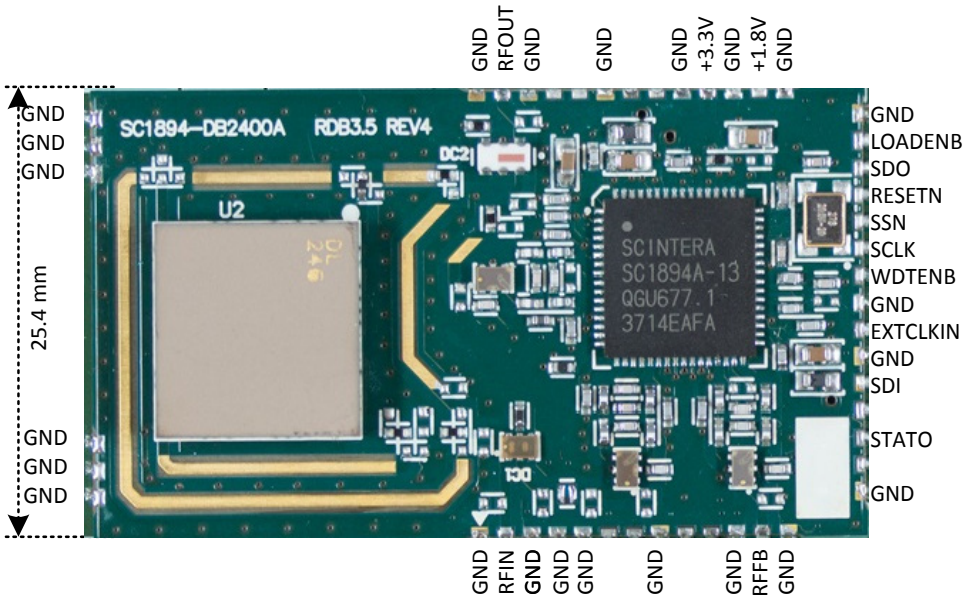


Figure 3. SC1894 reference board photograph and pin configuration.

IMPORTANT:

a. *Although not represented in Figure 3, it is highly recommended to use a connector to upgrade firmware with the GUI during the system integration and SPI interface bring up. This connector must have the following signals: SDI, SDO, SSN, SCLK, RESETN, WDTEN, GND, and LOADENB.*

b. *WDTEN (Watchdog Timer Enable) signal should be connected to the host to enable the timer during the firmware development phase.*

c. *The STATO signal is optional and is used for alarms in future FWs. It is recommended to connect it to the host for forward compatibility.*

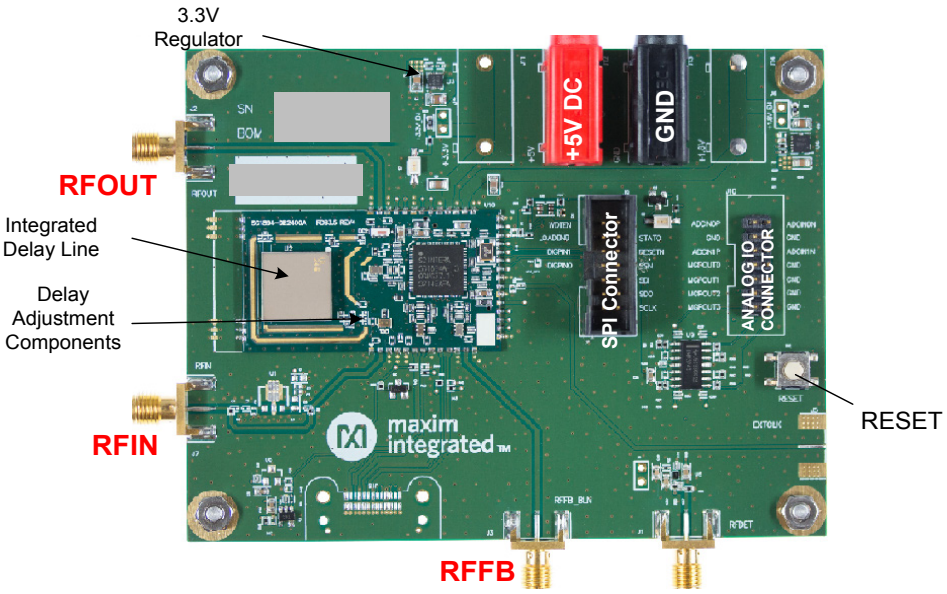


Figure 4. SC1894 reference design and motherboard.

SC1894 Reference Board is mounted on a larger board (motherboard) which includes DC and RF connectors and supply voltage regulators (**Figure 4**).

4. RF Design with RFPAL SC1894

This section provides help with the selection of RF components, physical placement and optimization of the power levels into the SC1894. It also helps to minimize spurs from entering the critical RF signal path as well as reducing coupling to other circuits.

4.1.RF Signal Path Overview

The following diagram depicts the RF signal path, typical average power levels and losses. The configuration illustrated in **Figure 5** utilizes directional couplers to sample the input signal (RFIN) and to inject the pre-distortion signal from SC1894 into the through path. Both Input and Output couplers should exhibit a minimum of 15dB directivity over the operating frequency band to avoid leaking of the predistorted signal back into RFIN.

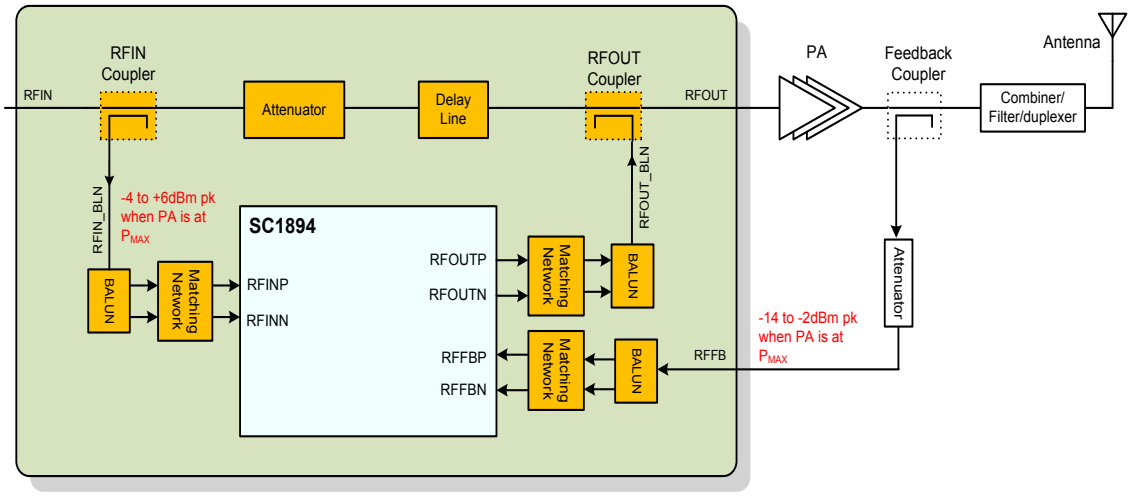


Figure 5. System block diagram.

4.2. RF Input (RFIN) Signal

This signal enters the SC1894 on pins 19 and 20 which are respectively labeled "RFINP" and "RFINN." The SC1894 generates a DC voltage at these pins hence the center tap of the BALUN secondary must be AC coupled. The signal return pins, 18 and 21, should be connected directly to the PCB ground area underneath the SC1894 (ground paddle, pin 65) for proper RF grounding. The RFIN matching network specification is provided in Section b.

We recommend placing the BALUN as close as possible to the SC1894 and designing the matching network with short symmetrical traces to avoid increasing capacitance and coupling to other circuits. High-parasitic capacitance due to long trace complicates the design of a broadband matching network (i.e., BW > 10% of RF). It is critical to layout a fully differential matching network to obtain good balance between the positive and negative inputs, improve common-mode signal rejection and coupling from other circuits. An example of fully differential matching network with low parasitics is illustrated in **Figure 6**.

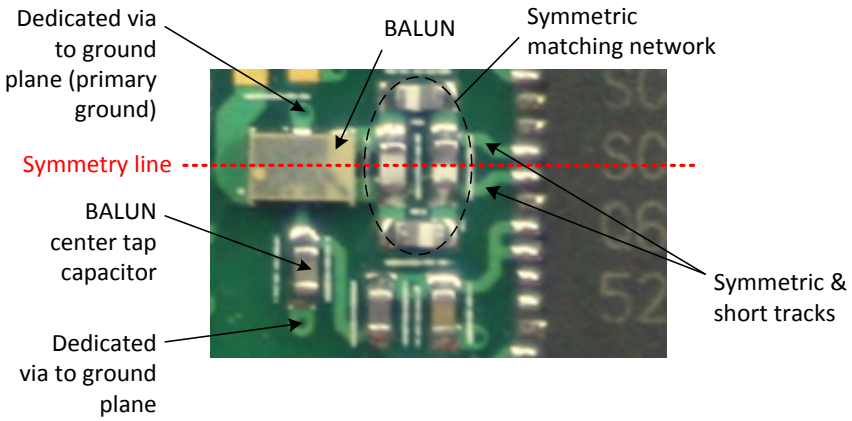


Figure 6. Balun + differential matching network.

The S-Parameter files of RF ports can be found in the Hardware Design Kit. Reference the application circuit schematics for details regarding the matching topology and component values (Section 2.2).

4.3. RF Input Path Temperature Dependent Attenuator Option

Due to temperature dependence of the power-amplifier gain RFIN coupled power might also change with temperature. RFIN power must be kept within acceptable limits for optimum predistortion performance. One way to minimize variation of RFIN level is to include a NTC (PTC) attenuator between the RFIN coupled port and the RFIN balun (**Figure 7**).

Layout provisions for a resistive pi-attenuators should be included in the design to fine tune the performance across the temperature range. For this purpose, SC1894 Evaluation Boards (EVBs) have an optional pi-attenuator on the RFIN trace. A link to the Budget Calculator Spreadsheet (Section 5.1) has also been provided to estimate the required attenuator at room and extreme temperatures.

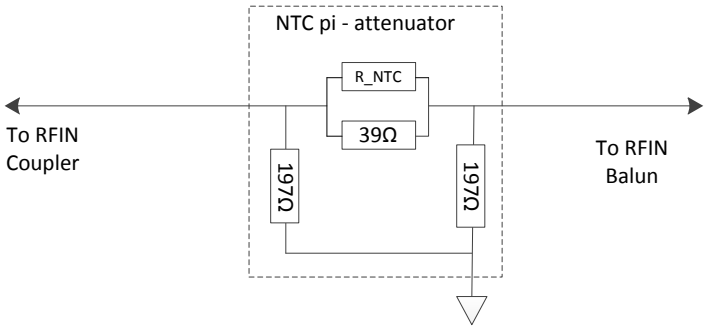


Figure 7. NTC attenuator in the RF input path.

4.4. RF Feedback (RFFB) Signal

The SC1894 uses the RFFB signal to monitor the PA output spectrum and to generate a metric to measure the PA linearity. This signal enters the SC1894 on pins 30 and 31, which are labeled "RFFBP" and "RFFBN," respectively. The SC1894 generates a DC voltage at these pins. Therefore, the center tap of the BALUN secondary must be AC coupled. The signal-return pins, 29 and 32, should be connected to the PCB ground area underneath the SC1894 ground pad (pin 65) for proper RF grounding. The specifications for the RFFB matching section can be found in Section 4.6. Identical recommendations apply to the RFFB matching network, as described in the RFIN section.

IMPORTANT:

a. *Spurious signals at the RFFB input can limit correction performance. Close-in (within 100MHz of the center frequency), the spurious/noise level due to external noisy circuits (i.e., not the SC1894) must be 10dB below the final correction. For example, if the ACLR requirement is -53dBc, the spurious level must be -63dBc.*

b. *It is critical to keep a flat gain response between the PA output and the RFFB IC input (< 1dB flatness over 3 times the signal bandwidth). Note that this requirement does not apply to the PA and the Group Delay of the RFFB path is not critical.*

c. *In some systems, if the spurious/noise level outside the correction bandwidth is large, performance can be increased by adding a band-pass filter at the RFFB input just before the BALUN. The band-pass filter bandwidth must be large enough to pass the PA nonlinearities and meet the < 1dB flatness over three times the signal bandwidth. For example, PAs with large 2^{nd} order harmonic (> -30dBc) can cause performance degradation. Low-cost handset SAW filters are good candidates for this filter.*

4.5. RF Output (RFOUT)

The SC1894 RFOUT correction signal is added to the through path using the RFOUT directional coupler to form the predistortion signal. This signal exits the SC1894 on pins 8 and 9, which are labeled "RFOUTP" and "RFOUTN," respectively. The signal return pins 7 and 10 should be connected to the PCB ground area underneath the SC1894 (ground paddle, pin 65) for proper RF grounding. The RFOUTP and RFOUTN pins are open-drain differential outputs. The drains are connected to the 1.8V power supply using the matching network and the BALUN secondary center tap. The specifications for the RFOUT matching section can be found in Section 4.6.

IMPORTANT: The RFOUT bandwidth is > 3x larger than the RFIN signal since it contains the RFIN signal and the predistortion signal.

2-port S-parameters of the SC1894 package pins are available for design in the Hardware Design Package. Refer to the application circuit schematic for details regarding matching topology and component values.

Note: There is a leakage path from RFOUT back to RFIN due to the finite directivity of the two directional couplers. This can adversely impact the signal purity of the "Reference" RFIN degrading linearization performance. Proper selection or design of the two directional couplers can be satisfactory as long as the directivity of each coupler is at least 15dB.

Matching network: It is recommended to place the BALUN as close as possible to the SC1894 and connecting the matching with very short symmetrical traces to avoid increasing capacitance and coupling to other circuits. High-parasitic capacitance due to long trace complicates the task of designing a broadband-matching network. It is critical to layout a fully differential matching network to obtain good balance between the positive and negative inputs, and to improve common-mode signal rejection and coupling from other circuits. An example of a fully differential matching network with low parasitics is illustrated in **Figure 8**.

IMPORTANT:

a. *The BALUN secondary center tap must be filtered to avoid supply noise leakage into the RFOUT port. We recommend using a ferrite bead in a π network configuration for optimum decoupling. It is especially important to filter out frequencies at the RFIN signal frequency.*

b. The RFOUT matching network must be DC coupled since the BALUN secondary provides the DC path to the power supply.

c. When selecting the ferrite bead, beware of the DC resistance since a 60mA current (max) flows across the BALUN center tap (coming from the SC1894). The DC voltage at pins 8 and 9 must meet the data sheet AVDD18 supply limits. The ferrite bead must meet the DC-current rating specification of 60mA.

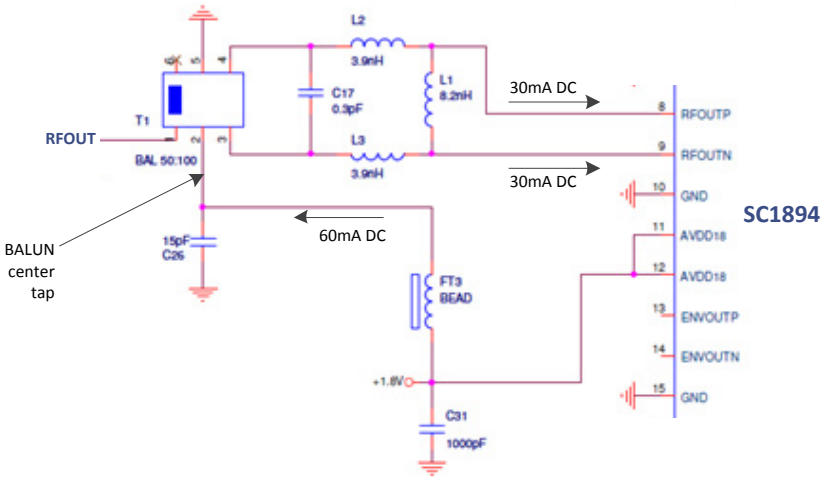


Figure 8. RFOUT BALUN, matching network and decoupling.

For improved filtering, the capacitor C26 (Figure 8) can be replaced by an inductor and capacitor in series to ground. The $L_{FILT}C_{FILT}$ combination should resonate at the center of the frequency band (f_{RF}). The values of L_{FILT} and C_{FILT} are given by:

$$f_{RF} = \frac{1}{2\pi.\sqrt{L_{FILT} \times C_{FILT}}}$$

IMPORTANT:

a. Do not share coupler 50Ω termination or BALUN ground vias with other circuitry. These vias should be connected directly to the ground plane with a very short trace to avoid coupling to other circuits.

b. Both the RFINP / RFINN and RFFBP / RFFBN differential ports are DC coupled inside the SC1894. Therefore, the BALUN center tap must be AC coupled.

4.6. Matching Network Performance Requirements

Although the hardware design guide provides values for RFIN, RFOUT, and RFFB ports, matching components, different substrate material, layer stack, and component choices require circuit tuning in order to optimize the return loss and obtain optimum power transfer. A single-stage matching network can achieve the flatness performance over the frequency range defined in Section b.

In case the operating frequency range needs to be increased beyond 15% of the RF center frequency, a 2-stage match should be used (at the cost of increased insertion loss).

The table below summarizes matching performance requirements for RF ports:

Table 1. RF Port BALUN/Matching Network Characteristics

Port	Return Loss (dB)	Return Loss BW [1] (MHz)	Insertion Loss (dB)	Group Delay Variation (ns)
RFIN	< -15	OBW	< -1.5	< 0.6 [2]
RFOUT	< -12	OBW + 6 x EBW	< -1.5	< 0.6 [2]
RFFB	< -15	OBW + 6 x EBW	< -1.5	NA

1. Example: OBW = Operating Bandwidth (i.e., 2100MHz to 2200MHz, or 100MHz). EBW = Envelop Bandwidth of the signal (i.e., for a 4-carrier WCDMA signal, 4x 5MHz, or ~20MHz). Total Required Return Loss Bandwidth: OBW + 6x EBW (i.e., 100MHz + 120MHz or 220MHz).
2. Over a 200MHz Bandwidth and the Group Delay variation must be less than or equal to 10° at 3GHz.

4.7. Power Measurement Unit (PMU) Recommendations

The SC1894 offers optional accurate power detection for the RFIN and RFFB signals. In case these applications are used, it is recommended to pay special attention to the temperature variations of the RF components to ensure that the temperature slope of RFIN and RFFB power levels do not vary across component batches. Minimizing variation of RFIN and RFFB levels with Temperature and Frequency is critical to achieve greater power-detector accuracy.

4.8. RF Delay Optimization

The RF delay is used to synchronize the SC1894 predistortion processing delay with the through-pass RF signal. In effect, the external (through-pass) delay must be close to the SC1894 memory polynomial average delay to fully take advantage of the integrated memory-effect compensation.

For most Doherty PAs and wideband class-AB PAs, the optimal delay is approximately 3ns to 4ns but we encourage experimentation with this value for each new PA design and after any PA tuning. For class-AB PAs amplifying more narrowband signals (BW ≤ 20MHz typically), the delay line can be replaced by 4dB attenuation with acceptable performance.

We recommend the following delay lines that are available from RN2 and Anaren:

- XDL15-3-030S by Anaren (3ns) [2]
- 2xXDL15-2-020S by Anaren (2ns) 2 [3]
- DL3 by RN2 (3ns)

SC1894 Evaluation Boards are using DL246A, which is no longer recommended. The delay value of the Reference Design Boards can be configured using 0Ω resistors around the delay line to 4ns (default configuration on), no delay, 2ns or 6ns.

5. RF Signal Level Optimization for RFPAL Circuits

For RFPAL to function at highest performance signal levels, the RFIN and RFFB ports must be within an optimum range at all operating conditions (PVT) when the PA operates at maximum power. This range is specified in SC1894 data sheet. To meet these requirements components determining the power levels (coupler, attenuators, matching networks) must be chosen based on a systematic link budget. The link-budget calculator provided is explained next.

5.1. Using the RFPAL Power Budget Spreadsheet

The "*RFPAL and PA Power Budget Calculator.xlsx*" spreadsheet is a tool provided with the hardware design guide to estimate required coupler and attenuator settings to meet the SC1894 power limits of RFIN and RFFB ports (**Figure 9**). It also helps the designer to size the correction power correctly. This tool encourages the system designer to consider temperature variations of each component since each parameter has to be entered for hot, cold, and nominal conditions. As the Input Power and component values are set for each temperature, the background for the associated cell changes if the RMS and/or peak-power level in RFIN and RFFB is not within the spec limits.

All instructions are located inside the spreadsheet. Follow the instructions step by step for an optimal design.

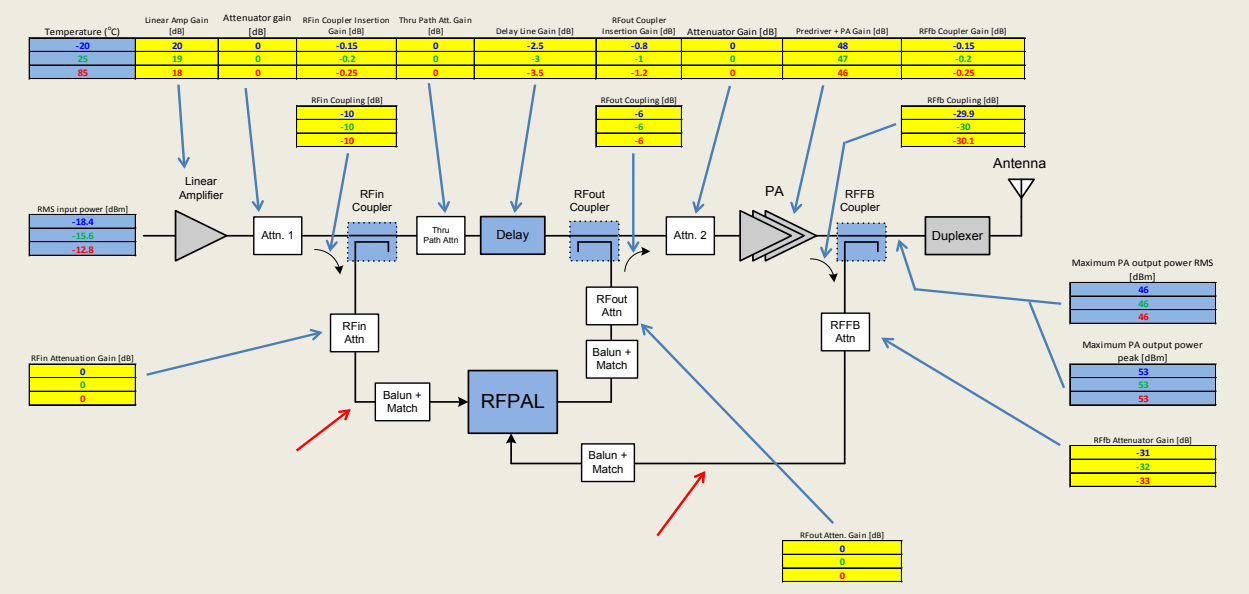


Figure 9. SC1894 power budget calculator panel.

5.2. RF Signal Level Optimization for RFPAL

- Initial calculation using spreadsheets like the RFPAL Link-Budget Calculator based on typical component values is only an estimation.
- It is strongly recommended that the prototype design should have enough input-power margin by using a high gain linear amplifier between transceiver IC output and RFIN-coupler input.
- Whether they are used or not, layout provisions for all resistive pi-attenuators should be included in all iterations of the design, even in the final product (and shorted with 0Ω SMT if not used). Experience has shown that, due to unforeseen part-to-part and temperature variations, which arise during the final qualification phase of the projects, resistive temperature-dependent attenuators had to be included to meet the link-budget requirement.

6. Spurious and Noise Performance

When designed according to the guidelines of this document, the SC1894 provides excellent correction performance with low spurious and noise levels. This section describes the SC1894's RFOUT spurious/noise content and how to improve it.

Depending on the FW state (CAL, TRACK/FSA), correction signal power and frequency band of operation, the frequency and power of the spurs vary. For most spurs, their level increases with correction power. For example, a PA with -25dBc uncorrected ACLR is more prone to spur/noise that a -30dBc uncorrected ACLR.

6.1. TRACK/FSA Mode

The spurs in TRACK/FSA mode are described in **Figure 10**. **Table 2** and **Table 3** list the frequency and power levels of these spurs for RFOUT correction power of minimum -20dBm.

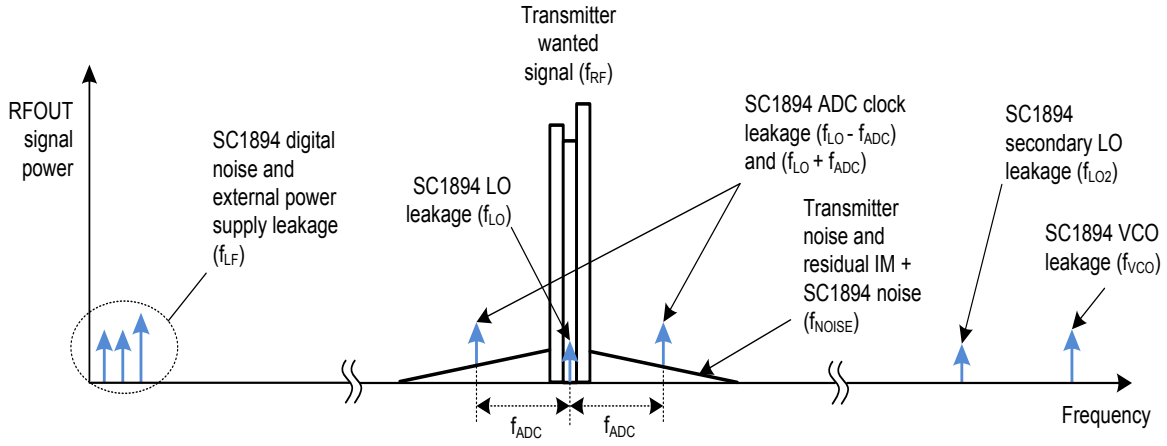


Figure 10. SC1894 spurious content (TRACK/FSA mode).

IMPORTANT: *For most systems, these spurs are NOT a problem since they are filtered out by the PA band pass action and the duplexer/filters.*

Table 2. Spur List (TRACK/FSA FW state) at RFOUT Port (except VCO spurs)

Spur type	Symbol	Frequency	Source(s)	Level [1]	Ways to reduce spurs/noise level
Low frequency spurs [2]	f_{LF}	< 1000MHz	Direct digital noise leakage/coupling from SC1894 internal circuitry/supplies to RFOUT	< -55dBm	• Decrease DVDD18 voltage (while meeting SC1894 data sheet limits). • Optimize 48, 55, 59 and 64 supply decoupling (see section 8.2). • Optimize RFOUT differential output balance and optimize BALUN center tap decoupling (see section 4.5). • Some of these spurs can be moved in frequency.
			Direct ADC clock leakage from SC1894 internal circuitry/supplies to RFOUT	< -55dBm	• Decrease AVDD18 voltage (must meet SC1894 data sheet limits). • Optimize supply decoupling network at pins 35, 36, 41 and 42 (see section 8.2). • Place ADC decoupling capacitors as close as possible to pins 33, 34, 37, 38, 39, 40, 43, 44 to reduce capacitive and EM coupling. • Optimize RFOUT differential output balance and optimize BALUN center tap decoupling (see section 4.5).
			Switching regulator noise leakage	< -55dBm	• Move switching regulator away from RFOUT output to reduce capacitive and electromagnetic (EM) coupling.
LO leakage (due to SC1894)	f_{LO}	Center of the RF signal ±0.5MHz	SC1894 LO generation circuit coupling to RFOUT	< -65dBm	• No fix, due to internal circuitry, typically not an issue.
ADC clock leakage	$f_{LO} - n*f_{ADC}$, $f_{LO} + n*f_{ADC}$	Center of the RF signal ±n*100MHz	SC1894 internal leakage from ADC to baseband correction path. The ADC clock frequency is between 90MHz and 108MHz depending on the LO frequency.	< -70dBm	• Decrease AVDD18 voltage (must meet SC1894 data sheet limits). • Optimize supply decoupling network at pins 35, 36, 41 and 42 (see section 8.2). • Place ADC decoupling capacitors as close as possible to pins 33, 34, 37, 38, 39, 40, 43, 44 to reduce capacitive and EM coupling. • Optimize RFOUT differential output balance and optimize BALUN center tap decoupling (see section 4.5).
Transmitter noise and residual IM	f_{NOISE}	Out of Band	SC1894 thermal noise and residual correction error		• If necessary, use filtering at the PA output.

1. Measured at RFOUT_BLN output for RFOUT Correction Power = -20dBm
2. Typically, low-frequency spurs are not critical; they are filtered out by the PA DC-blocking transfer function and other filtering elements at the PA output (diplexers, etc.). Nonetheless, it is important to check that the low-frequency spurs do not up-convert due to excessive second order distortion in the PA. To confirm this, it is recommended to apply a single CW tone at the RFIN input, and measure the PA output spectral content around the wanted signal frequency.

6.2. VCO Spurs in Track State

VCO spurs frequency (f_{VCO}) and level depends on the frequency of the operation. These spurs are measured when RFPAL is in TRACK state. VCO spurs also exist in CAL state as shown in the next section. These spurs can be reduced with a filter in the RFOUT_BLN path (**Figure 5**). However, one should be careful not to disturb the correction signal.

Table 3. VCO Spurs at RFOUT port

	Band	Operation Freq (f_{RF} in MHz)	f_{VCO}	Source	Level (dBm	How to Reduced VCO Spurs?
Internal VCO leakage (RFIN frequency dependent)	01	225 – 260	f_{RF} * 16	SC1894 Internal VCO coupling to RFOUT	< -35	Filter in the RFOUT_BLN path (Figure 5)
	02	260 – 520	f_{RF} * 8		< -70	
	03*	168 – 960				
	04	520 – 1040	f_{RF} * 4		< -35	
	05	1040 – 2080	f_{RF} * 2		< -35	
	06*	698 – 2700				
	07	1800 – 2700	f_{RF} * (4/3)		< -35	
	08	2700 – 3500	f_{RF} * (4/5)		< -35	
	09	3300 – 3800	f_{RF} * (2/3)		< -40	

*Band 03 and 06 are stitched bands and are combination of multiple bands. Their spur depends on the underlying band. To reduce the spur generation, it is recommended to limit the min and max frequency scanning range to the minimum required for the application.

Notice that for Band 01 and 02 VCO frequency is 16 and 8 times the operation frequency. Usually, for these bands harmonics of the correction signal, which is at the operation frequency, are closer to the operation band than the VCO spur.

6.3. CAL Mode Scanning Spurs

During the CAL Mode, SC1894 searches for input signal by scanning the LO frequency through the band defined by the min and max scanning frequency limits (see SPI command documentation for setting the f_{MIN} and f_{MAX} values). During this mode, the internal LO circuit (f_{LO}) scans the f_{MIN} to f_{MAX} frequency range and leaks small amounts of signal to RFOUT. In addition, other LO-generation circuit spurs are present at the RFOUT such as the secondary LO spur (f_{LO2}) and the VCO spur (f_{VCO}). The CAL mode spurs are described in **Figure 11** and **Table 4**.

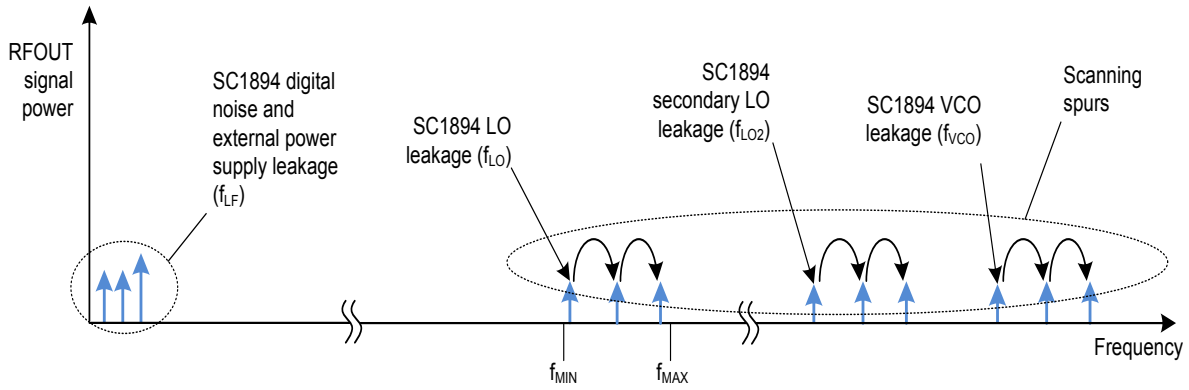


Figure 11. SC1894 spurious content (CAL mode).

IMPORTANT: *Restricting the f_{MIN} and f_{MAX} values to the band of interest is recommended to limit the frequency range of scanning spurs. For example, for the 2100MHz WCDMA band, f_{MIN} and f_{MAX} should be set to 2110MHz and 2170MHz, respectively.*

Table 4. Scanning Spurs List (CAL firmware state)

Spur type	Band	LO Frequency (MHz)	Source(s)	Level [1] (dBm)	Ways to reduce spurs/noise level
LO Leakage (f_{LO}) leakage (band dependent)	01	225 – 260	SC1894 LO generation circuit coupling to RFOUT	< -35	
	02	260 – 520		< -75	Typically, these spurs are not an issue since they are far out of band and filtered out by the PA duplexer/filter.
	03[1]	225 – 960			
	04	520 – 1040		< -75	
	05	1040 – 2080		< -35	
	06[2]	698 – 2700			
	07	1800 – 2700		< -50	
	08	2700 – 3500		< -35	
	09	3300 – 3800			
VCO leakage f_{VCO} (band dependent)	01	f_{MIN} * 16 to f_{MAX} * 16	SC1894 VCO coupling to RFOUT	< -35	
	02	f_{MIN} * 8 to f_{MAX} * 8		< -70	
	03[2]				
	04	f_{MIN} * 4 to f_{MAX} * 4		< -70	
	05	f_{MIN} * 2 to f_{MAX} * 2		< -35	
	06 [2]				
	07	f_{MIN} * (4/3) to f_{MAX} * (4/3)		< -35	
	08	f_{MIN} * (4/5) to f_{MAX} * (4/5)		< -35	
	09	f_{MIN} * (2/3) to f_{MAX} * (2/3)		< -40	
Secondary LO Leakage	All	All	SC1894 LO generation circuit coupling to RFOUT	< -70	

1. Measured at RFOUT_BLN output.
2. Band 03 and 06 are stitched bands and are a combination of multiple bands. Their spur depends on the underlying band. To reduce the spur generation, it is recommended to limit the min and max frequency-scanning range to the minimum required for the application.

6.4. High Speed ADC Voltage References (FLTCAP*)

The internal high speed ADC's bias lines are externally decoupled (FLTCAP0P, FLTCAP0N, FLTCAP1P, FLTCAP1N, FLTCAP2P, FLTCAP2N, FLTCAP3P, FLTCAP3N).

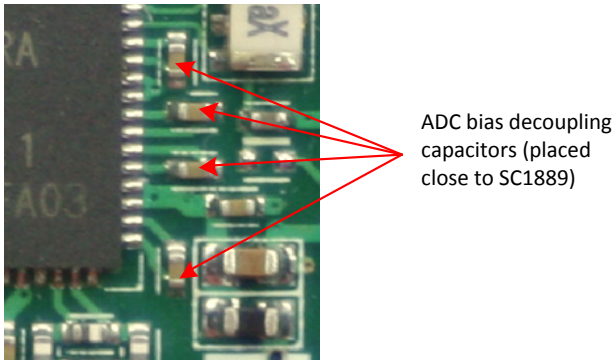


Figure 12. ADC decoupling capacitors.

IMPORTANT: *The ADC-bias decoupling capacitors must be close to the SC1894 since they filter out a noisy 100MHz switching signal. This prevents long lines from coupling noise and spurs to other circuits.*

7. PCB Layout Considerations for RFPAL

7.1. Floor Planning and Placement Priorities

Before laying out the board, it is important to create a good floor plan with optimum tradeoffs for best correction performance and lowest spurious emissions. The following guidelines are in priority order:

1. Priority 1: Select layer stack.
2. Priority 2: Design RF traces, select/place critical RF components and optimize power levels (RFIN, RFFB, coefficient levels). Place the RFPAL circuitry close to the input of the PA module to minimize trace lengths for RFIN and RFOUT and Thru (Delay) Path. See Section 5.
3. Priority 3: Place power supplies, decoupling and select regulators. See section 8.
4. Priority 4: Select/place the clock reference circuit. See section 9.
5. Priority 5: Place noncritical signals (digital control and analog signals, etc.). See section 0.

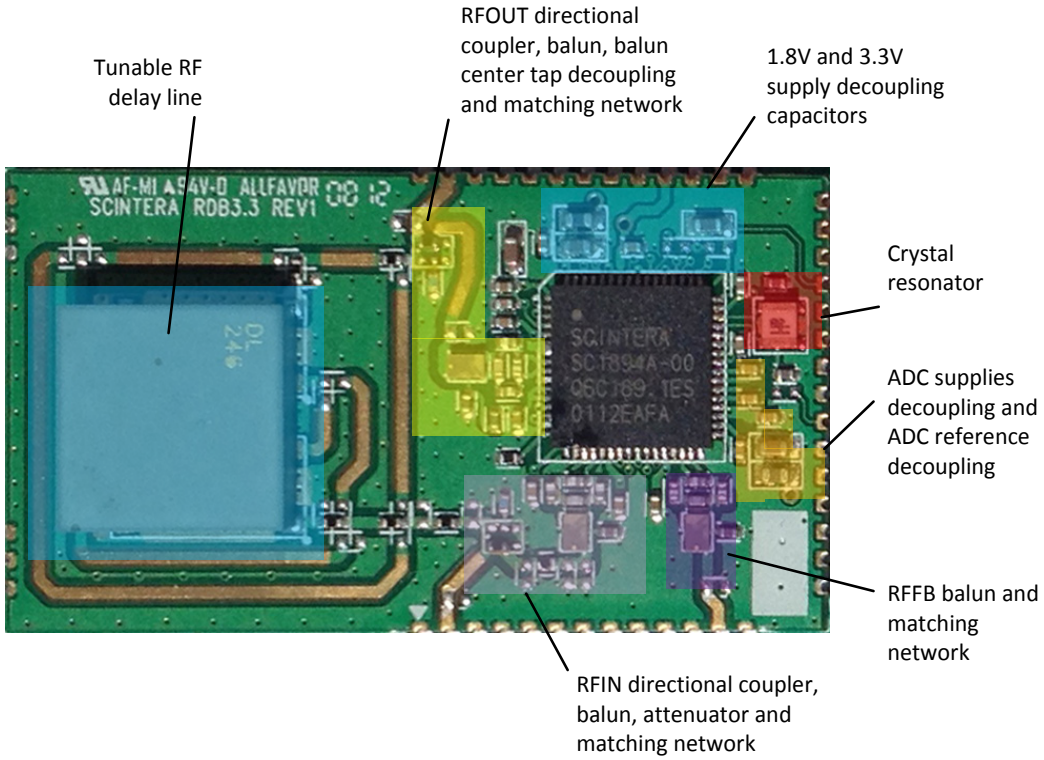


Figure 13. SC1894 reference board floor plan.

7.2. SMT Component Size Selection

To support compact designs, the SC1894 was designed with a package lead pitch of 0.5mm. Use of 0402 and 0201 components are ideal for matching networks since they permit very compact and low-parasitic implementations. It is also encouraged to use 0805 BALUNs and directional couplers for the same reasons.

7.3. Layer Stack

The SC1894 reference board is built on a four-layer, epoxy fiberglass, fabrication that is constructed with two cores each clad on both sides with 1oz copper. The layer stackup is shown in **Figure 14**:

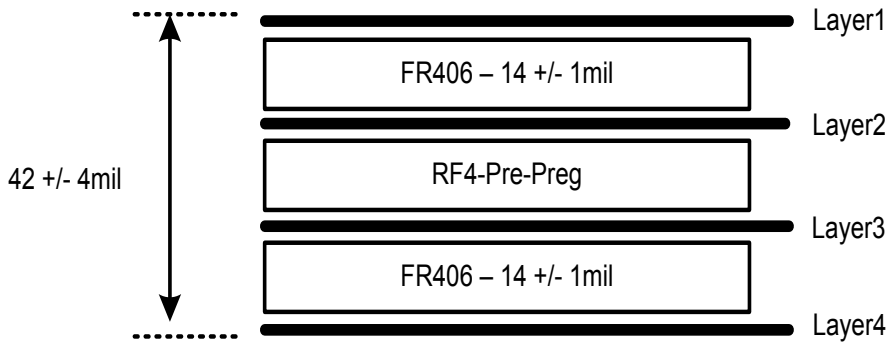


Figure 14. PCB fabrication layer stack.

IMPORTANT: *It is NOT recommended to use a two-layer PCB due to the numbert of connections and RF traces.*

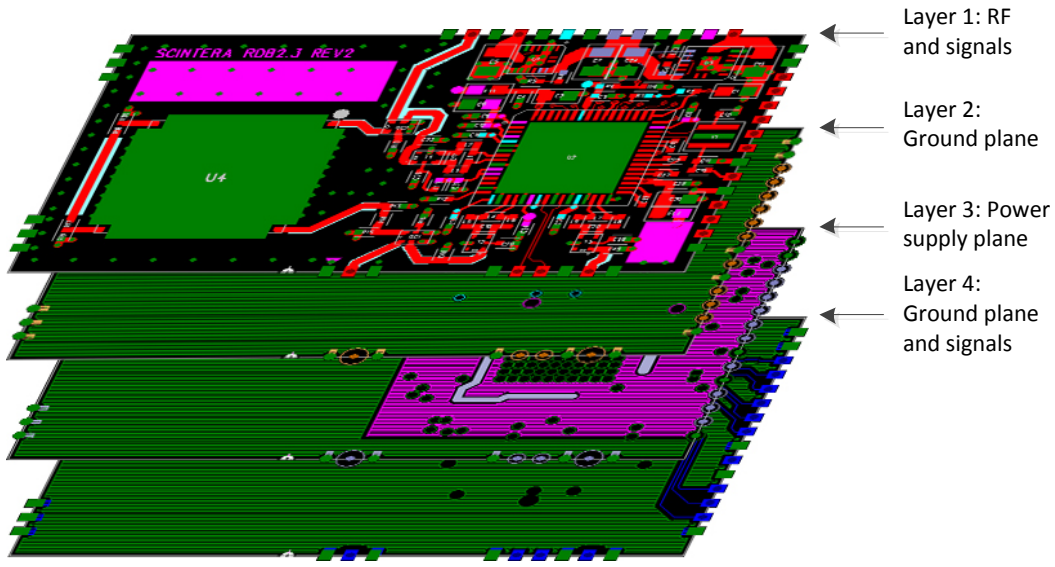


Figure 15. SC1894 reference board layers.

7.3.1. Layer 1: RF and Signals

As can be seen in the assembly drawing, the top layer contains the RF, interface, power-supply regulation and analog circuitry. All components are mounted on this layer, which is designed with an FR406 laminate that is 0.014in thick and has a nominal dielectric constant of 4.2. 50Ω-trace width needs to be modified for a different dielectric material.

This dielectric and material thickness are well-suited for RF design between 160MHz and 4200MHz since the 50Ω lines match the 0402 component-landing pad size, hence avoiding discontinuities. Also, the dielectric thickness is large enough to have sufficient trace width to meet 50Ω line impedance, including typical PCB fabrication tolerances.

When possible, surround RF traces and matching networks by ground vias to control the RF return. All RF traces must have a continuous ground plane underneath for impedance control and noise immunity.

IMPORTANT: *Care should be taken to ensure that no noisy return current paths are routed under or close to sensitive RF circuit blocks.*

Under the SC1894 ground paddle and the RF delay line, multiple vias ensure that the total parasitic inductance associated with the vias is minimized by several parallel connections. In addition, distributed vias ensure an even thermal distribution as described in section 7.4. Refer to the Altium layout and Gerber files.

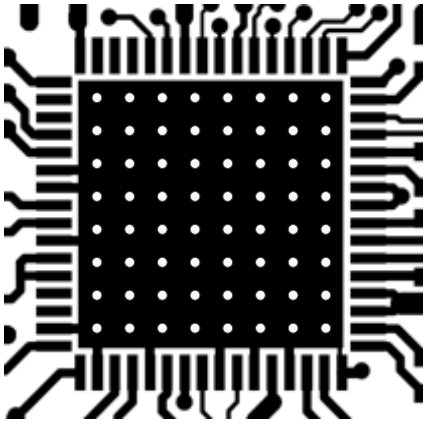


Figure 16. Via array under SC1894 ground paddle.

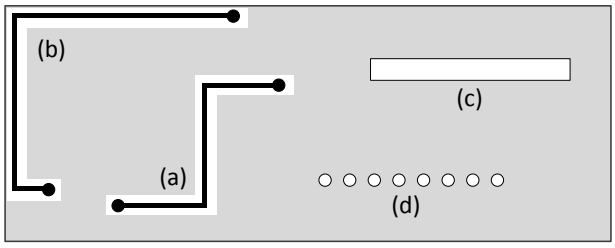
7.3.2. Layer 2: Ground Plane

The second layer is dedicated to the ground plane and fulfills the following functions:

- Provides a controlled impedance to RF signals.
- Provides noise immunity to RF signals.
- Provides a low-impedance return path to all supplies, RF, and digital and analog signals.
- Enhances the thermal spreading of the PCB.

Although this is not a hard rule, there is no ground separation between the DC supply, RF, and analog circuitry. This greatly simplifies the grounding and avoids unknown return paths due to complex grounding schemes. The following recommendation should be followed for the ground-plane design:

- Pay attention to the holes and cutouts in the ground planes. They break up the plane; therefore, cause increases in loop areas (see (a) and (b) in **Figure 17**).
- Avoid buried traces in the ground plane. If they must be used, put them in the signal or power supply plane.
- Breaking up the plane with a row of holes is much better than having a long slot (see (c) and (d) in Figure 17).
- Connect components directly to the ground plane and avoid sharing vias.



(a) Poor: trace cuts ground plane and prevents direct returns
(b) Better: Perimeter trace avoids cutting ground plane. Best solution is not signal trace in ground plane

(c) Poor: slot cuts ground plane and prevents direct returns
(d) Better: via string maintains ground plane continuity

Figure 17. Ground plane recommendations.

7.3.3. Layer 3: Power Supply Plane

Layer 3 is the power plane that distributes the 1.8V and 3.3V to the SC1894. Ground is placed under the RF-delay area. Priority is given to the 1.8V supply since it provides power to the RF blocks and it consumes more DC power than the 3.3V supply. Two dedicated 1.8V filtered supplies are used for the digital and ADC's power supplies as shown in **Figure 18**:

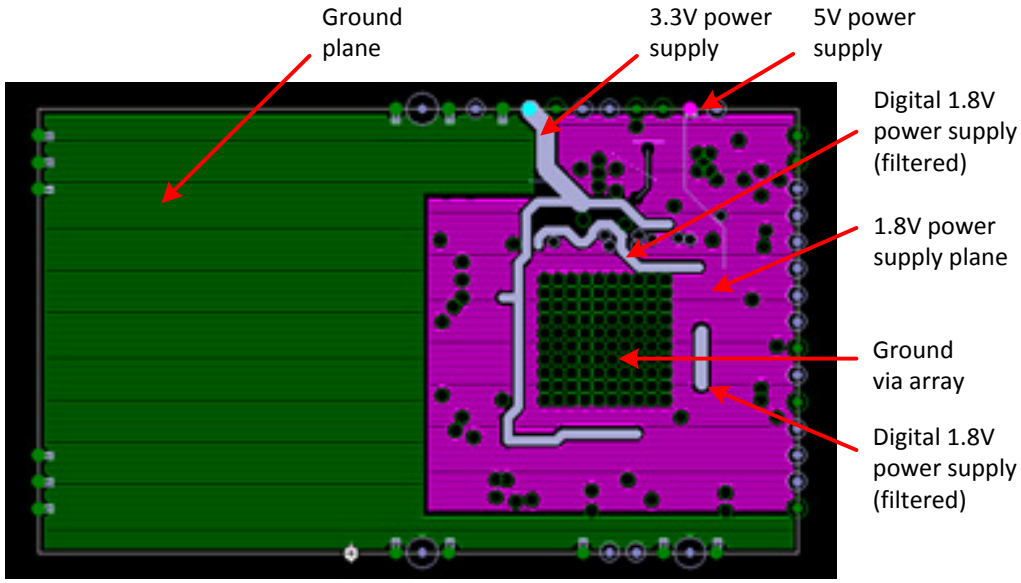


Figure 18. Layer 3, power supply distribution.

The dielectric between layer 2 and 3 is fabricated with an epoxy fiberglass material that is approximately 0.014in thick. The dielectric material is not critical as this layer is primarily used for DC-power distribution.

7.3.4. Layer 4: Ground Plane and signals

This layer is used to route noncritical low-frequency analog and digital signals. In addition to signal routing, a large portion of this layer is dedicated to grounding for thermal relief and low-impedance grounding, so this board can be soldered to a motherboard through a low-impedance connection.

SC1894 reference board can be soldered onto a PCB. In this case, it is important to place a solder mask over the signals to avoid shorts to the PCB. Refer to the Altium layout and Gerber files.

7.4. Thermal Relief Pad

The thermal relief pad under the SC1894 provides both thermal relief and a solid ground reference to the chip. This pad should be ideally connected to a component side ground connection which in turn is connected to the main ground plane layer by multiple vias. **Figure 16** illustrates the multiple via (or "well stitched") connection of the thermal relief pad to the main (inner) ground layer.

The SC1894 is guaranteed to work up to 100°C case temperature. Case temperature is the temperature at the ground paddle, as described in **Figure 19**:

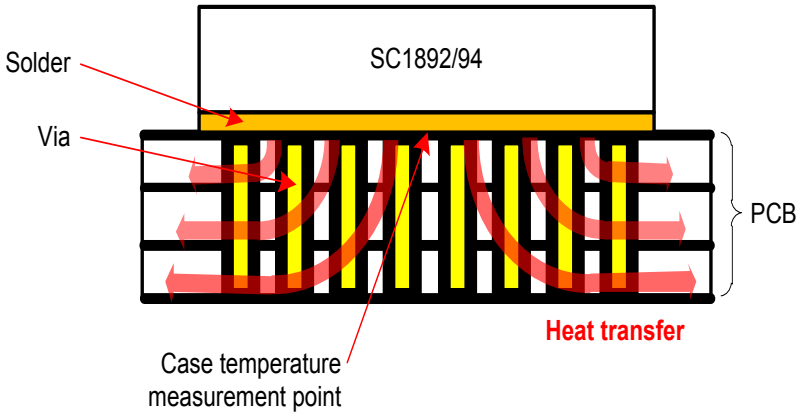


Figure 19. PCB fabrication layer stack.

7.5. PCB Parasitics

An area that is often overlooked during PCB layout is the electrical characteristics of the PCB material itself, component traces and vias. The electrical characteristics of the PCB used to physically mount and connect the circuit components in a high frequency RF product can have a significant impact on the performance of that product.

At RF it can be seen that a long signal trace has inductance associated with it, while a pad over an area of ground plane or power plane has an associated capacitance. As a result, we recommend using short traces for non-50Ω RF traces (from the BALUN to the RF match and to the IC inputs) to reduce capacitive loading and avoid coupling to other circuits.

An often overlooked PCB parasitic component is the via, used to connect one PCB layer to another. Typically for a 1.6mm thickness PCB material, a single via can add 1.2nH of inductance and 0.5pF of capacitance, depending upon the via dimensions and PCB dielectric material.

7.6. Delay Line Solutions

We recommend the following delay lines that are now widely available:

1. XDL15-3-030S (3ns delay line) by Anaren

2. XDL15-2-020S (2.2ns delay line) by Anaren. For 20MHz and Doherty linearization, two of these components should be used for optimal performance.

3. DL3 (3ns) and DL4 (4ns) by RN2

The SC1894 evaluation boards were designed to provide delay "programmability" to address all PA configurations; thus, they use the Kyocera DL246A. Kyocera delay line DL246 was replaced by DL246A from Richardson RFPD [1]. The higher reliability and more-cost effective Anaren delay parts became available at a much later time and do not exhibit the solder pad failure mechanism of the DL246 or DL246A.

If Richardson RFPD's DL246A is the only option, then the layout with checkered pattern soldermask must be used in order to address the reliability problem. Notice that the top layer ground is a continuous shape while the soldermask (purple) is a checkered pattern alternating with via holes (gray). See **Figure 20**.

An example schematic and layout with two Anaren Delay Line (XDL15-2-020S) for SC1894 – EVK1900 has been included in the Hardware Design Kit (Section 2.2). Similar schematic and layout can be adapted for frequencies between 300MHz and 2700MHz and one XDL15-3-030S (3ns delay line) by Anaren.

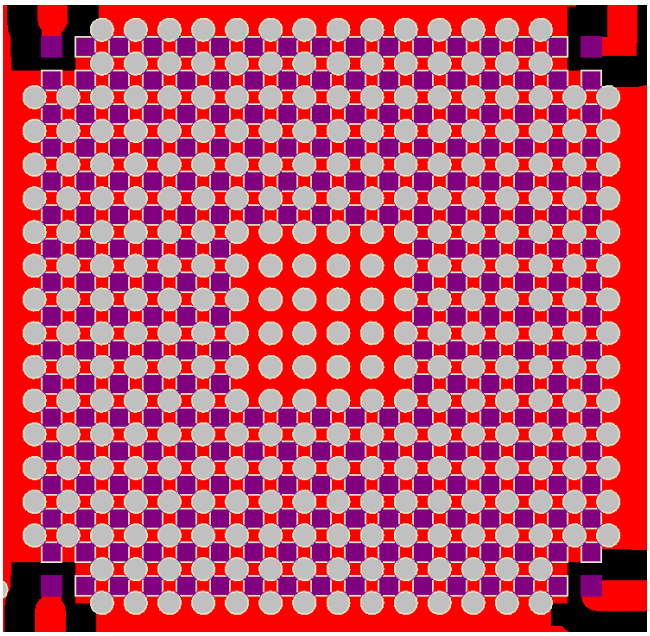


Figure 20. Checkered pattern for DL246A delay line (red: top layer, purple: solder mask, grey: via holes).

[1] Please contact Richardson RFPD for more information.

8. Power Supplies

The SC1894 has been designed to support linear regulators as well as switching regulators. It is recommended to use switching regulators for better efficiency and reduce overall system power consumption.

This section describes how to:

- Properly size the regulators and supply feeds.
- Design adequate supply noise/ripple.
- Decouple the supply lines.
- Sequence the power supplies.

8.1. Regulator Selection

The supply regulator must support the SC1894 peak current load as well as provide low ripple and noise as described in section 8.4. The maximum SC1894 peak current is provided in the SC1894 data sheet [1].

Power-supply trace widths must be large enough to minimize resistive losses. Special care must be taken with pins: 35, 36, 41, 42, 48, 55, and 64, which draw higher current than others. Section 13.3 provides typical pin currents when using firmware 4.1

Star connection is recommended for best current distribution and noise filtering for the following supply groups:

- 35, 36, 41, 42—see section 8.2 for decoupling recommendations.
- 48, 55, 59, 64—see section 8.2 for decoupling recommendations.

IMPORTANT: *Pins 35, 36, 41 and 42 have significant digital switching activity and must NOT be shared with other power supplies. The same comment applies to pins 48, 55, 59 and 64.*

8.2. Supply Decoupling

Minimize current loops on PCB layouts by decoupling as close to the port being decoupled to ground as possible. Try and avoid capacitive coupling by ensuring that each circuit block or port has its own decoupling capacitor. Ensure that each decoupling capacitor has its own via connection to ground. As a rule of thumb, components should not share vias.

It is recommended that all associated supply decoupling capacitors be mounted as close as possible to SC1894 power supply pins for the following reasons:

- Provide efficient supply decoupling and reduce trace inductance.
- Reduce the risk of polluting other circuits due to capacitive or electromagnetic coupling.

In addition to the decoupling capacitors, ferrite beads on selected supply lines are required. The ferrite beads are used to isolate digital noise generated by the SC1894. It is important to select a ferrite bead that does not introduce a large voltage drop to respective SC1894 supply pins. See the application circuit Bill of Materials for recommended ferrite bead part numbers. Recommendations:

1. Each of the power supply pins 4, 5, 17, 22, 47 and 58 should have a 1000pF decoupling capacitor connected to the ground plane. Close placement of these 1000pF decoupling capacitors to the corresponding pins is recommended.
2. Pin 11 and 12 can share a 1000pF decoupling capacitor connected to the ground plane.
3. Pin 23 and 28 can share a 1000pF decoupling capacitor connected to the ground plane.
4. One ferrite bead (MURATA BLM18AG121SN1D, 120Ω 500MA 0603), 1000pF decoupling capacitor and a 2.2µF capacitor are required going into DVDD18 pins 48, 55, 59 and 64.
5. One ferrite bead (MURATA BLM18AG121SN1D, 120Ω 500MA 0603), 1000pF decoupling capacitor and a 2.2µF capacitor are required going into AVDD18 pins 35, 36, 41 and 42.
6. One ferrite bead (MURATA BLM18AG471SN1D, 470Ω 500MA 0603) is required on pin 2 of the RFOUT BALUN with a capacitor to ground. An alternate ferrite bead (BLMBD471SN1) can be used.

8.3. Supply Power On and Turn Off Timing Sequence

In the SC1894 reference design, a delay between the 1.8V and 3.3V supplies has been designed. This delay is required to ensure that the 3.3V IO supply is settled before the 1.8V is powered on (see **Figure 22** and **Figure 23**). As a result, the 1.8V digital core is reset (with an internal Power-On Circuit when all the digital IOs are quiet and the EEPROM supply is stable. Refer to **Figure 21** and **Table 5** for the timing requirements. There is no requirement on the power-off sequence.

Table 5. Power Sequencing Requirements

PARAMETER	SYMBOL	Value	UNITS
3.3V Ramping Time (10% to 90%)	$T_{3.3}$	> 10	µs
1.8V Ramping Time (10% to 90%)	$T_{1.8}$	> 10	µs
Delay between 3.3v and 1.8V	T_{DELAY}	> 100	µs

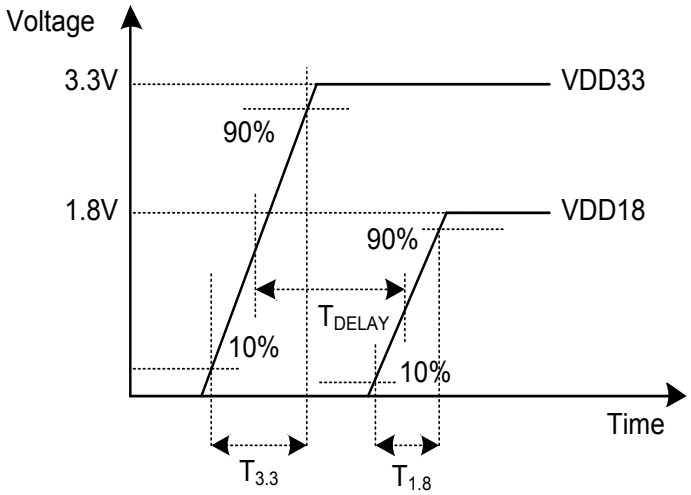


Figure 21. 1.8V and 3.3V power-on timing sequence.

IMPORTANT: *The 1.8V and 3.3V power supplies must be powered sequentially if no external reset is applied. Refer to Figure 21 and Table 5 for the timing requirements.*

It is possible to avoid power supply sequencing. In that case, the RESETN signal is held low at least 100µs after the last supply voltage stabilizes to 90% of its final value. The RESETN pulse must be held low for at least 1µs.

8.4. Power Supply Requirements

Table 6. Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VDD33_v	AVDD33 or DVDD33 Supply Voltage at IC pin	3.1 + 0.5 x VDD33_ripple_pkpk	3.3	3.5 – 0.5 x VDD33_ripple_pkpk	V
VDD18_v	AVDD18 or DVDD18 Supply Voltage at IC pin	1.7 + 0.5 x VDD18_ripple_pkpk	1.8	1.9 – 0.5 x VDD18_ripple_pkpk	V
VDD33_ipk	3.3V Supply Peak Current (across PVT), when using the supply decoupling used in the SC1894 Reference Boards	-	-	150	mA
VDD18_ipk	1.8V Supply Peak Current (across PVT), when using the supply decoupling used in the SC1894 Reference Boards	-	-	1000	mA
VDD33_ripple_pkpk	Peak-to-peak 3.3V Supply Ripple from 10kHz to 5MHz	-	-	30	mV (pk-pk)
VDD18_ripple_pkpk	Peak-to-peak 1.8V Supply Ripple from 10kHz to 5MHz	-	-	30	mV (pk-pk)

If step-down voltage conversion is needed, it is acceptable to use a switching regulator operating at approximately 4MHz. While this requires special attention in the design of the power-supply filters, this is a tractable problem given the 4MHz switching frequency and these regulators offer attractive efficiencies of 70% to 95% depending upon the regulator and the load. The Enpirion regulators shown in **Figure 22** and **Figure 23** are each capable of providing 1A of current at their respective voltages.

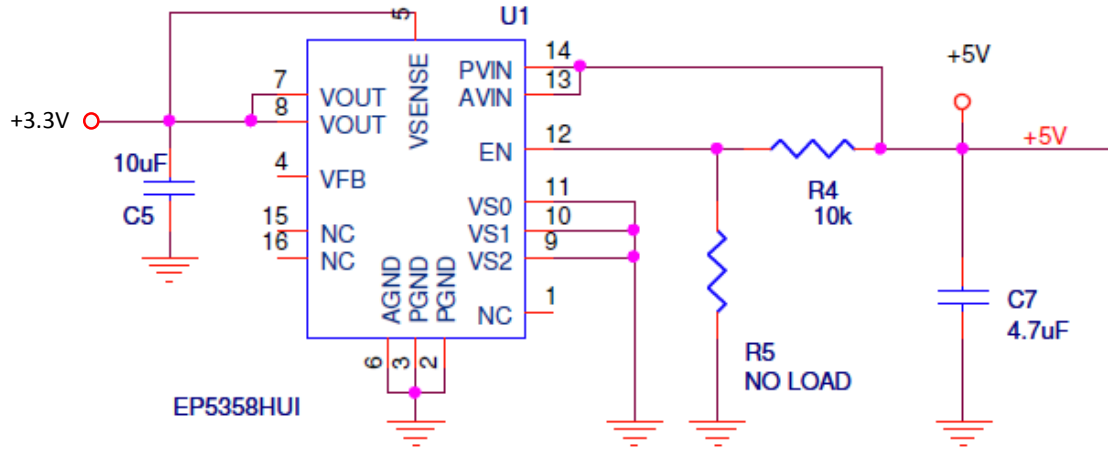


Figure 22. 5V to 3.3V switching regulator.

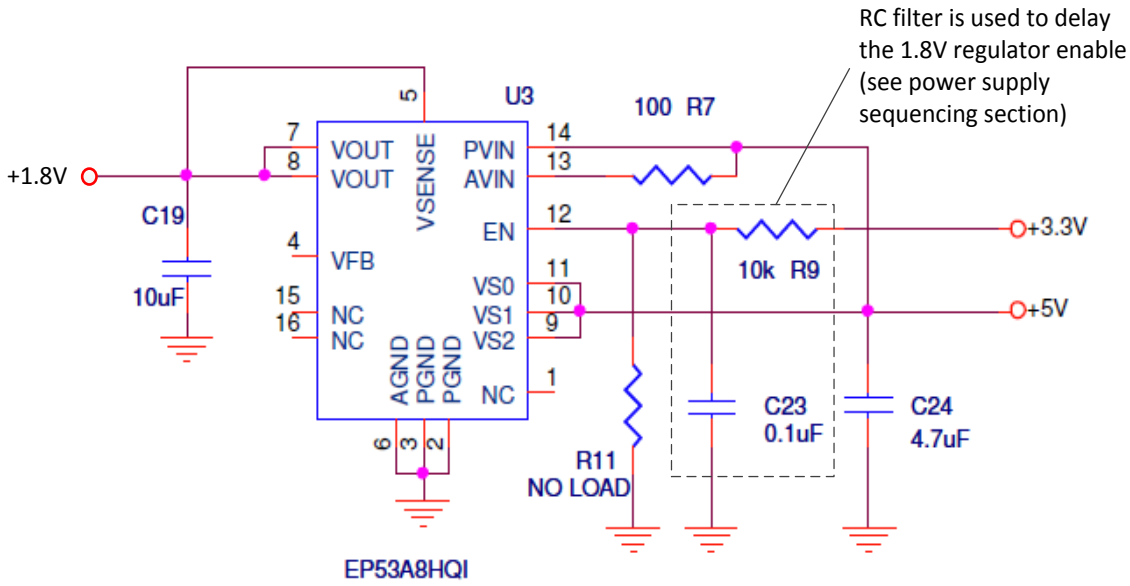


Figure 23. 5V to 1.8V switching regulator.[2]

Minimize current loops on PCB layouts by decoupling as close to the port being decoupled to ground as possible. Try and avoid capacitive coupling by ensuring that each circuit block or port has its own decoupling capacitor. Ensure that each decoupling capacitor has its own via connection to ground. As a rule of thumb, components should not share vias.

[2] The 1.8V regulator enable pin (pin 12) is connected to a filtered (R9, C23) 3.3V supply to ensure that the delay between the 1.8V and 3.3V supplies met the requirements defined in **Table 7** and Figure 21.

8.5. SC1894 Power Consumption

*IMPORTANT: The power supplies current provided in this section as typical only. See **Table 6** for the regulator requirements.*

Table 7. Typical Power Consumption for SC1894—23 with FW 4.1 (25°C ambient)

	1.8V Current (mA)		3.3V Current (mA)		Total Power (mW)	
Condition	**RMS**	**Peak**	**RMS**	**Peak**	**RMS**	**Peak**
Average Current/PWRduring INIT/CAL mode	592	776	81	108	1332.9	1753.2
FSA/Track Duty Cycled Feedback OFF	565	840	71	110	1251.3	1875
FSA/Track Duty Cycled Feedback ON	320	840	33	110	684.9	1875

Table 8. Typical Power Consumption for SC1894—23 with FW 4.1 (-40°C ambient)

	1.9V Current (mA)		3.5V Current (mA)		Total Power (mW)	
Condition	**RMS**	**Peak**	**RMS**	**Peak**	**RMS**	**Peak**
Average Current/PWRduring INIT/CAL mode	615	808	80	96	1448.5	1871.2
FSA/Track Duty Cycled Feedback OFF	581	824	70	98	1348.9	1908.6
FSA/Track Duty Cycled Feedback ON	327	832	32	96	733.3	1916.8

9. Reference Clock

Either a crystal resonator or external clock is required to generate an accurate reference. If a crystal oscillator is used, its frequency must be 20MHz. If an external clock is used, the system accepts various reference frequencies (MHz): 10, 13, 15.36, 19.2, 20, 26 and 30.72.

IMPORTANT: *FW 4.0 only supports 20MHz external clock. Additional clock frequencies are supported in FW 4.1.*

9.1.20MHz Resonant Element (using the SC1894 oscillator)

The resonator element frequency must be 20MHz with the following characteristics:

- Tolerance < 250ppm
- Drift < 100ppm over temperature range and aging

When a crystal resonator is used, it should be connected across pins 45 "XTALI" and 46 "XTALO" with capacitors to ground. See the SC1894 reference circuit schematic for details.

To guarantee startup of oscillation, a crystal with ESR < 50Ω and load capacitance to ground at < 12pF is required.

IMPORTANT: *Although the SC1894 is rated for -40°C to +100°C case temperature, many crystals are not routinely rated for an operating temperature range of -40°C to +100°C.*

9.2. 10MHz to 30.72MHz External Clock (slave mode)

In slave mode, the system accepts various reference frequencies (MHz): 10, 13, 15.36, 19.2, 20, 26 and 30.72. The external source must meet the following requirements:

- Tolerance < 250ppm
- Drift < 100ppm over temperature range and aging

IMPORTANT: *Selecting an external reference clock frequency other than 20MHz requires programming the SC1894 EEPROM through the SPI bus. See SC1894 SPI Programming Guide [6].*

For an external clock (sine and square waves are supported), the clock signal must be AC coupled (DC is set by the SC1894) to the "XTALI" pin. The amplitude must be between $0.5V_{PK-PK}$ and $1.5V_{PK-PK}$ at the pin and phase noise must be better than -130dBc/Hz at 100kHz offset.

If only 3.3V logic levels are available in the system, an appropriate level shifter must be utilized. We recommend an AC-coupled voltage-divider as shown in **Figure 24**. R1 and R2 values need to be adjusted based on the clock source voltage level as described below:

$$\mathrm{Vpkpk(XTALI)} = \frac{\mathrm{R2}}{\mathrm{R1} + \mathrm{R2}} . \mathrm{Vpkpk(EXTCLK)}$$

Example: if the clock buffer has a $3.3V_{PK-PK}$ output (EXTCLK), then if R1 = 1kΩ, R2 = 560Ω, V_{PK-PK}(XTALI) ~ $1.2V_{PK-PK}$. C1 = 47pF. The clock buffer must have a low-output impedance (or high-current drive) so that Z_{OUT} < (R1 + R2) / 10.

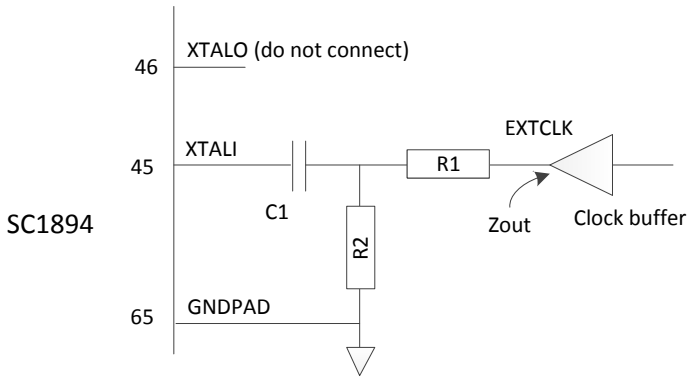


Figure 24. External clock diagram.

IMPORTANT:

a. *Pin 46 (XTALO) must not be connected when an external clock is utilized.*

b. *Ensure that the clock at XTALI has clean edges (no ringing or spurious transitions)*

c. *In case a square wave is used, the duty cycle must be between 45% and 55%*

10. Analog and Digital Input / Output

10.1. Analog Signals

10.1.1. Bandgap Voltage (BGRES)

The SC1894 uses an internal bandgap circuit to generate a bias reference that feeds all the internal circuits. The external band gap resistor must be placed very close to pin 16 and connect directly to the ground paddle (do not share ground with other circuits). This minimizes coupling from other circuits. The bandgap voltage is provided in the SC1894 data sheet [1].

The bandgap resistor must be 12.4kΩ, 1% tolerance and temperature stable to 100ppm/°C.

This bandgap voltage at pin 16 can be reused to bias other circuits in the system. In that case, the bandgap voltage must be isolated from the other circuits as follows:

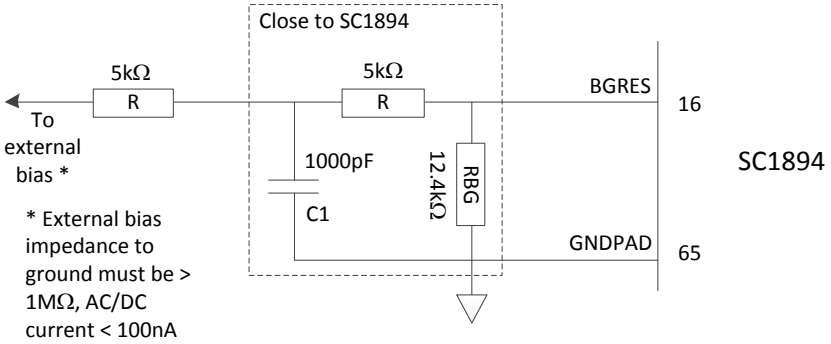


Figure 25. External bias circuit using the SC1894 bandgap voltage.

10.2. Digital Signals

An SC1894 IBIS model is available in the HDK to simulate the digital signals integrity. See sections 2.2.

10.2.1. RESETN

It is required that RESETN, pin 49, be connected to a host processor through a GPIO connection or use a 1µF capacitor connected between pin 49 and ground. The RESETN pin is internally pulled up to DVDD33 through an integrated resistor (**Table 10**). The RESETN (active low) signal must be kept low for at least 100µs after the last supply is ramped to at least 90% of its final level or it can be pulsed (from high-to-low and kept there for at least 1µs and then back to high). When this signal is low, the SC1894 is in reset mode. When the signal goes high, the SC1894 begins to boot up and completes this process in approximately 1s to 3s (depending on firmware version). After the boot-up process, SC1894 starts adapting toward optimal linearization.

Implementing a GPIO connection to pin 49, RESETN, allows the host processor to remotely reset SC1894 if a reinitialization is required.

10.2.2. WDTEN (Enable Watch Dog Timer)

The SC1894 has an internal watchdog timer to reboot the system in case the FW crashes. It is recommended to connect this pin to the host for future use. Otherwise, it should be left floating since this pin has an internal pullup resistor.

10.2.3. STATO (Status Output)

Pin 57 provides status output from SC1894. The STATO pin is a +3.3V, open-drain output with an internal pullup resistor (Table 10).

10.2.4. DGPIN1 (Transmit Enable Input)

DGPIN1, also known as transmit enable input pin 56, (sometimes abbreviated TXEN), is a +3.3V digital logic signal with an internal pullup resistor (Table 10).

10.2.5. Internal Pullup/Pulldown Information

Table 9. Internal Pullup/Pulldown Information

PIN	NAME	IO	PULL Direction
49	RESETN	Input	Pullup
50	WDTEN	Input	Pullup
51	SCLK	Input	Pulldown
52	SSN	Input	Pullup
53	SDI	Input	Pulldown
54	SDO	Output	None
56	DGPIN1	Input	Pullup
57	STATO	Output	Pullup
60	LOADENB	Input	Pulldown
61	RESERVED0	Input	Pulldown
62	RESERVED1	Input	Pulldown
63	DGPIN0	Input	Pulldown

Table 10. Internal Pullup/Pulldown Values

PARAMETER	TYP	UNITS
Internal Pullup	14	kΩ
Internal Pulldown	8.5	kΩ

10.2.6. SPI Interface

The SPI bus is comprised of four pins labeled: SCLK, SSN, SDI, and SDO. The SC1894 operates as a slave on this interface, can operate from 50kHz up to 4MHz, and can share the bus with other slave devices (including multiple SC1894s) using distinct slave select signals from the master control (SSN). The SPI bus operates in Mode 0 (CPOL = 0 and CPHA = 0), which means that data is sampled on the rising edge and data is generated on the falling edge of SCLK. The signals use 3.3V digital logic levels and support the following functionality:

- SCLK is an input that should receive a clock signal from the bus master during SPI transactions. The clock should have a 50% duty cycle and can operate from 50kHz up to 4MHz. Internally to the SC1894, the pin is connected to a 50kΩ resistor to ground.
- SSN (Slave Select) is an active-low input that functions as an active-low slave select allowing the host to act as the bus master to enable communications to the SC1894. Internally to the SC1894, the pin is pulled up with an internal resistor (Table 10) to DVDD33.
- SDI is an input that functions to receive addresses, messages/commands, and data values from the host controller. This signal should be wired to the MOSI (master out/slave in) signal from the bus master. Internally to the SC1894, the pin is connected to a 50kΩ resistor to ground.
- SDO is a three-state output when not in transaction. This signal should be wired to the host MISO signal (master in/slave out) signal. This pin does not have an internal pullup or pulldown, and must be externally pulled-up by 10kΩ to DVDD33. This pin is capable of driving 12mA. Listed below is the equation for determining the maximum load capacitance for the SDO pin:
    - C_{MAX} (shunt to ground) = 3.75e-4/f_{SPI} (in Farad), where f_{SPI} is the frequency of the SPI clock (SCLK) in Hz.
        - For example: for f_{SPI} = 4MHz, the maximum load capacitance (C_{MAX}) to ground is 94pF. The SDO pin capacitance is 2.8pF and must be taken into account when calculating C_{MAX}.
        - For values greater than C_{MAX}, a buffer such as the NC7WZ16P6X would be required.

10.2.7. LOADENB

In conjunction with the aforementioned SPI interface signals, pin 60 must be utilized when updating SC1894 firmware. Input to the pin utilizes 3.3V logic and contains an internal pull down resistor (Table 10). If the board or system containing SC1894 has an administrative Host Processor, it is recommended that this LOADENB pin be connected to a GPIO from the host controller. While this signal is "low," the SC1894 is in normal operation. When the LOADENB signal is HIGH, the SC1894 is placed in a mode where the SPI Bus is directly connected to the internal EEPROM. It is recommended that in this mode, the SC1894 be placed in a special continuous reset mode (explained previously). Throughout programming, LOADENB must be a logic level HIGH and at the completion of the programming process the level must transition to a LOW logic level. After the programming has been completed, a hard reset should be initiated by commanding the RESETN input LOW for at least 1us then toggled HIGH through the GPIO connection.

10.2.8. Digital Interface Connector

To upload new firmware and debug the operation of SC1894 PA linearizer, a digital connector with 14 pins shown in **Figure 27** is suggested to be included in the final product. Out of these 14 pins, DGPIO0, DGPIO1 and STATO are not used by RFPAL Firmware. WDTEN is recommended for host software development. The other pins are critical for Firmware upload.

IMPORTANT: ESD protection measures must be included around this connector to avoid any damage to digital pins of the IC.

11. Multi-SC1894 Applications

The SC1894 is well-suited for multiple channel applications such as MIMO or beam forming. A multi-SC1894 application schematic is available.

11.1. SPI interface

The SDI, SDO and SCLK signals can be shared amongst several SC1894 (**Figure 26**). One SSN per SC1894 is needed to communicate with a single linearizer. Special care must be taken when connecting long PCB traces at the SDO output since the capacitance (C_{LOAD}) increases. Refer to section 10.2.6 to calculate the maximum speed at which the SDO pins can be read (including the parasitic load capacitance C_{LOAD}).

The GUI can support only one RFPAL. Therefore, for multi-RFPAL applications it is suggested to include layout provisions for a series 0Ω resistors in the SDO line of each RFPAL as shown in Figure 26 and connect this component only for the SC1894 being tested to avoid any conflict with the inactive SC1894 while working with the GUI.

Also suggested is to include layout provisions for a separate connector for each RFPAL. This 14 pin connector should have pin-out as in **Figure 27** to match the SC1894 evaluation board connectors.

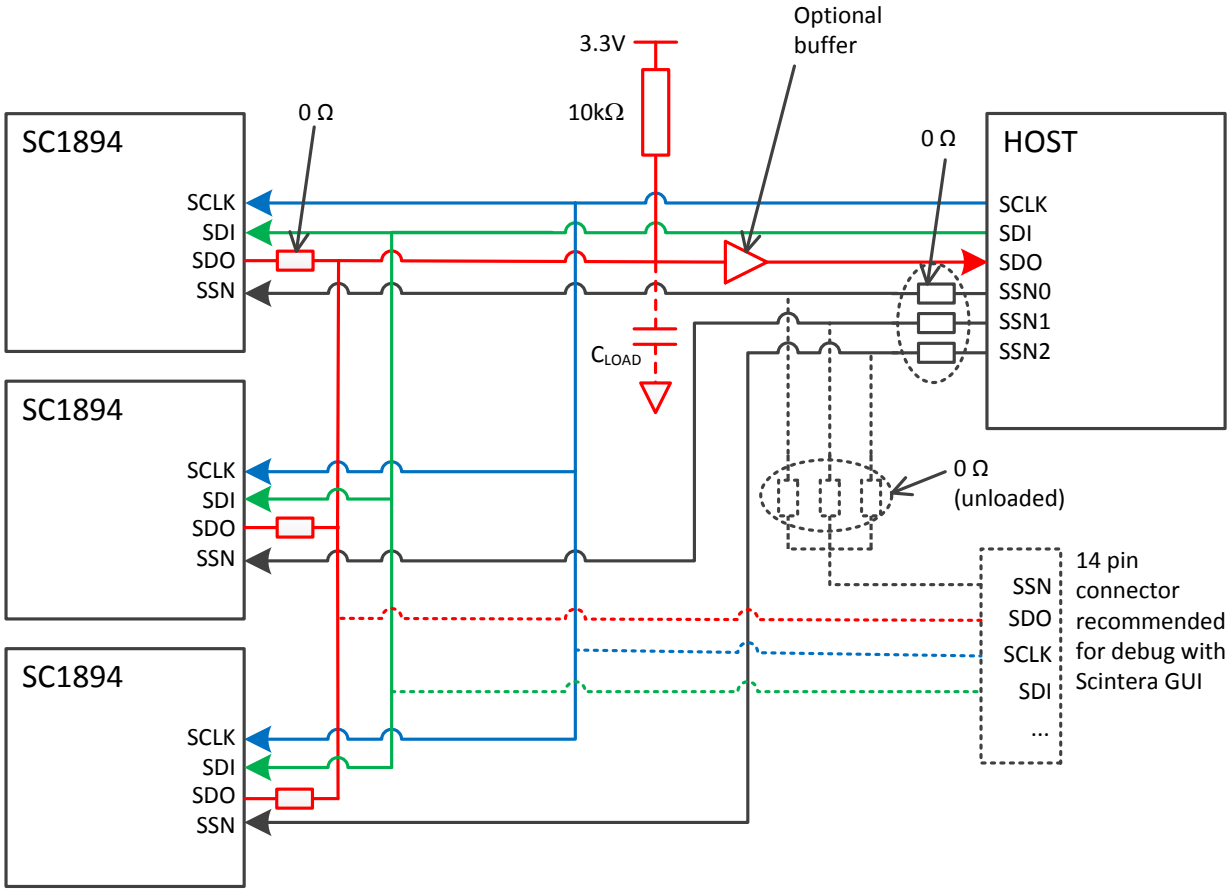


Figure 26. Host SPI connection for multiple SC1894 applications.

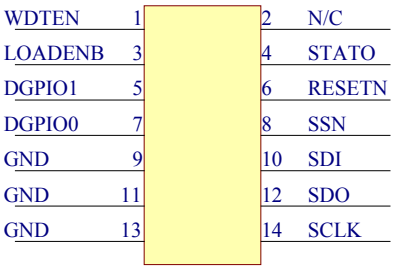


Figure 27. Interface connector for firmware upload and development.

IMPORTANT:

a. *The SC1894 SDO-pin capacitance is 2.8pF and must be part of the C_{LOAD} calculation. See section 10.2.6 for the maximum load capacitance calculation.*

b. *If an SDO buffer is needed, the buffer must be placed after the point (a) as described in Figure 26.*

c. *Refer to the multi-SC1894 SPI protocol in the SPI Programming Guide [6]*

d. *If this additional connector cannot be included because of layout restrictions at least test-point pins should be included for debugging if necessary.*

e. *DGPIO0 can be connected to GND*

11.2. Miscellaneous Digital Pins for Multi-SC1894 Applications

- **STATO**: If STATO pin is used for ALARM INDICATOR (Section 10.2.3) each STATO pins from SC1894 must be routed separately to the host connector.
- **LOADENB (pin 60)**: LOADENB pins can be connected into a single pin of the host interface.
- **RESETN (pin 49)**: When RESETN pins are connected together into a single pin of a host interface, all SC1894s are reset when these pins are pulled to 0V.
- **WDTEN (pin 50):** WDTEN pin can be connected into a single pin of a host interface.
- **DGPIN1 (TXEB):** TXENB (pin 56) pins can be left disconnected if not used or connected to the host-interface pin separately.

11.3. Reference Clock for Multi-SC1894 Application

A single external clock can be used for multi-SC1894 applications as in **Figure 28**.

Refer to section 9.2 for component values.

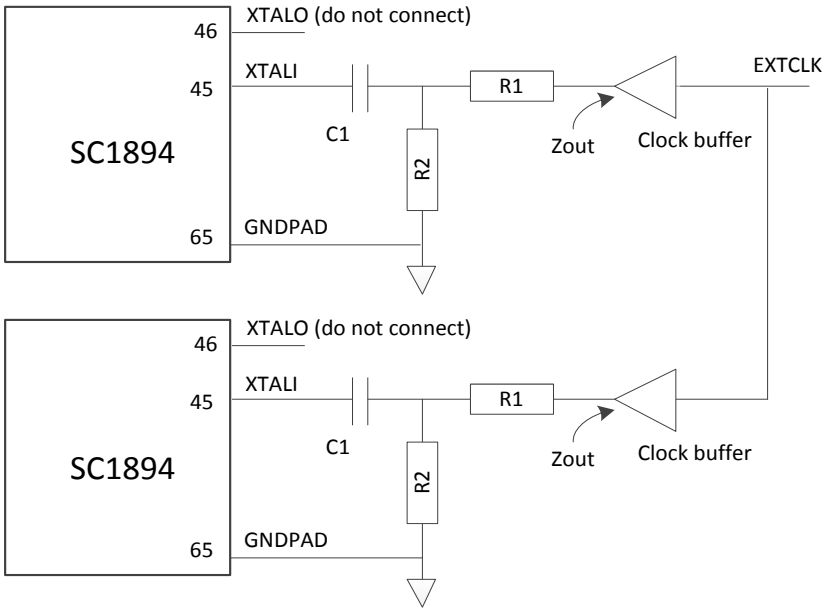


Figure 28. External clock diagram for multiple SC1894 applications.

11.4. Power Supplies for Multi-SC1894 Applications

3.3V and 1.8V regulators can be shared between multiple SC1894s as long as the total current requirement is satisfied. **Table 11** lists switching regulators available from one of the vendors to supply multiple RFPALs. Alternatively, linear regulators can be used as well.

Table 11. Enpirion regulator part numbers

Regulator Part Number	Maximum Current Load (A)	3.3V Supply	1.8V Supply
EP5358	0.6	OK for 4x3.3V supplies	Not OK
EP5388	0.8	OK for 4x3.3V supplies	Not OK
EP53A8	1.0	OK for 5x3.3V supplies	OK for 1x1.8V supply
EN5311	1.0	OK for 5x3.3V supplies	OK for 1x1.8V supply
EP53F8	1.5	OK for 10x3.3V supplies	OK for 1x1.8V supply
EN5322	2.0	NA	OK for 2x1.8V supplies
EN5339	3.0	NA	OK for 3x1.8V supplies
EN6337	3.0	NA	OK for 3x1.8V supplies
EN6347	4.0	NA	OK for 4x1.8V supplies
EN2340	4.0	NA	OK for 4x1.8V supplies

12. Troubleshooting

If your system is not working correctly, reference the troubleshooting tips outlined in **Table 12**.

Table 12. Troubleshooting tips

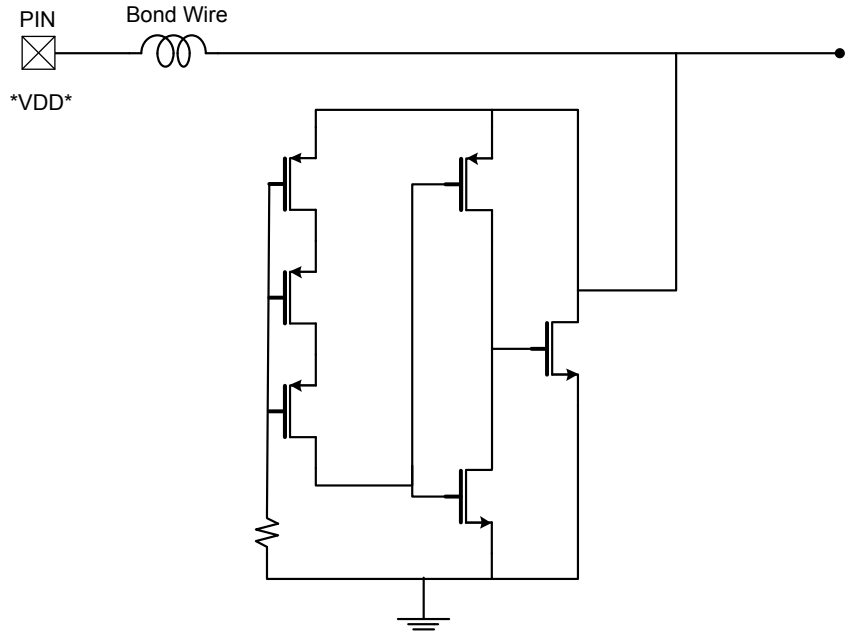
#	Symptom	Recommendations
1	No Correction	Verify 1.8V and 3.3V are present at each of the supply pins and meet the data sheet limits and the ripple/noise requirements as described in section 3.
2	No correction, but 3.3V and 1.8V supplies are present at the IC pins.	Verify that the bandgap resistor (12.4kΩ) is installed properly and that the DC voltage on pin 16 is 1.24V ±0.074V. A low-capacitance scope probe (< 10pF) must be used to perform this measurement. Verify that the supply currents are similar to those listed in **Table 13** and that the pin voltages correspond to **Table 14**.
3	No correction, but 3.3V and 1.8V supplies are present at the IC pins.	Verify the crystal is properly installed. A 1.2 ±0.3V_{PK-PK}, sinusoid should be observed on pin 45. A low-capacitance scope probe (< 10pF) must be used to perform this measurement. If the software is not running and 1.8V and 3.3V current consumption is approximately 10mA for each supply. If using the same regulators as SC1894 reference board, the 5V current is approximately 22 ±5mA.
4	No correction. Crystal/resonator is working properly. SC1894 remains in the CAL state (FW state can be determined through the GUI or based on current consumption). See section 8.5 for 1.8V and 3.3V typical current consumptions.	Verify that the couplers, RFIN BALUN and that the RFIN matching components are installed and properly soldered to the PCB. Verify that the RFFB BALUN and RFFB matching components are installed and properly soldered to the PCB.
5	RFIN-power level displayed from GUI is much lower than expected.	Verify that the input power to the coupler is within the recommended operating range (see Figure 5 and SC1894 data sheet).Verify that the couplers, RFIN BALUN and that the RFIN matching components are installed and properly soldered to the PCB.
6	RFFB-power level displayed on GUI is much lower than expected.	Verify input-power level to the RFFB BALUN is correct. Check that RFFB BALUN and that the RFFB matching components are installed and properly soldered to the PCB (see Figure 5 and SC1894 data sheet).
7	RFIN- and RFFB-power level are correct, but there is no correction.	Verify that all the RFOUT components are installed and properly soldered to the PCB.
8	If the board is correcting, but the GUI is not working.	Verify that all SPI signals are present. Measure the SCLK, SSN, SDI, SDO and compare with information/diagrams described in section 0. Verify that GUI version is compatible with the Firmware.
9	If the board is correcting, but spurs are present.	See sections 4.5 and 6.
10	No correction or worse correction performance at low and or high temperatures.	Verify that RFIN and RFFB levels are within the recommended limits across the temperature range as specified in the SC1894 data sheet; Verify that the crystal oscillator (pin 45 and 46) is still running with 1.2V_{pp} across the temperature range.
11	Correction is varying across the frequency.	Verify that RFIN and RFFB levels are within the recommended limits across the frequency range as specified in the SC1894 data sheet.
12	Firmware can't be uploaded.	Verify that the crystal oscillator is running.
13	RFPAL registers cannot be accessed by the host.	Verify that the crystal oscillator is running.

13. Appendix

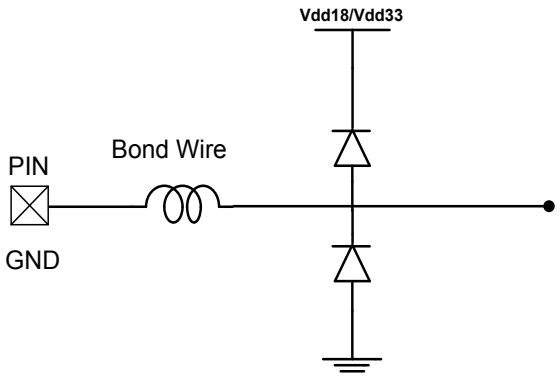
13.1. GND / VDD Pins

This section describes the SC1894 internal ground and supply circuits.

13.1.1. *VDD*



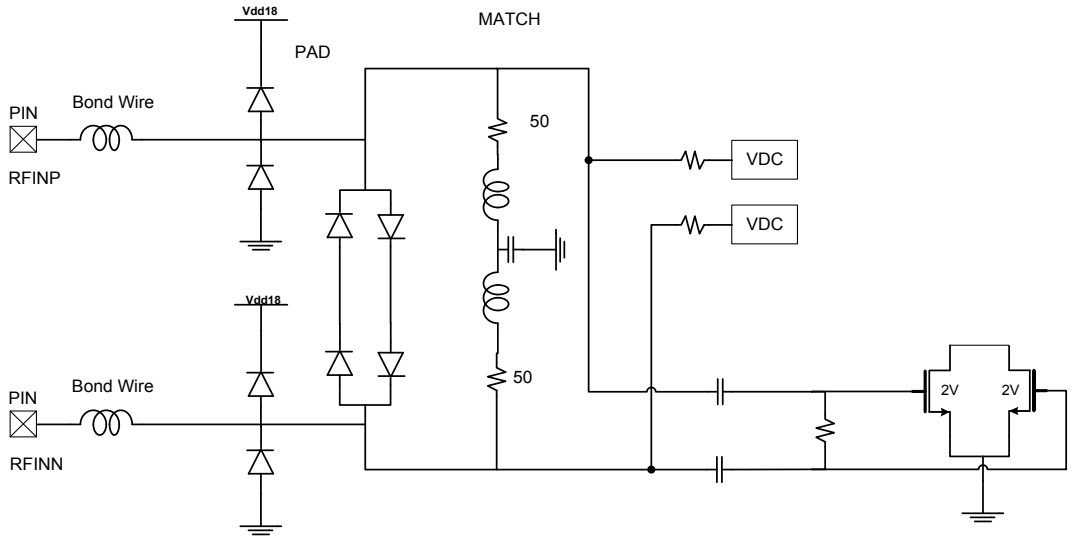
13.1.2. GND



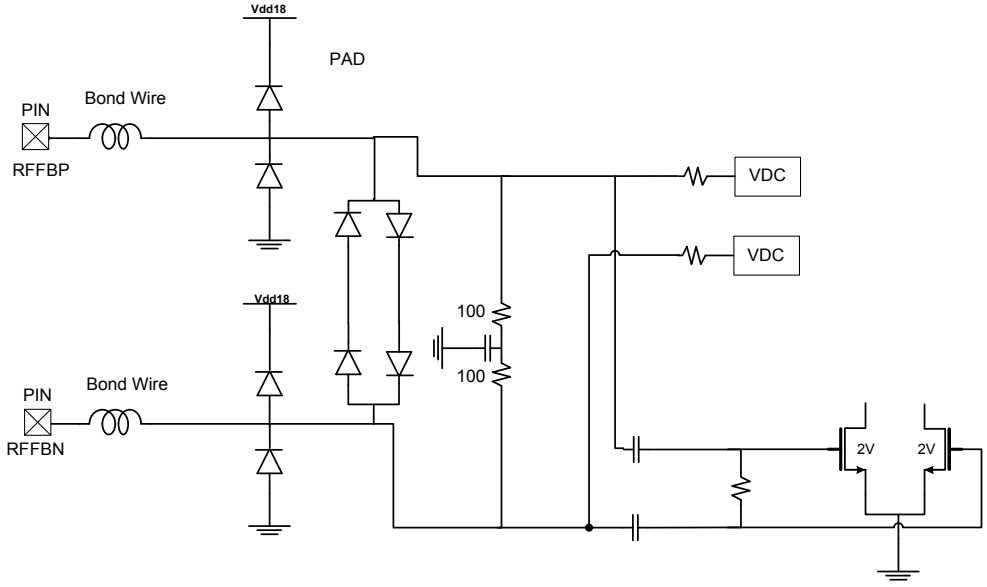
13.2. IO Circuits

This section describes the SC1894 internal input/output circuits.

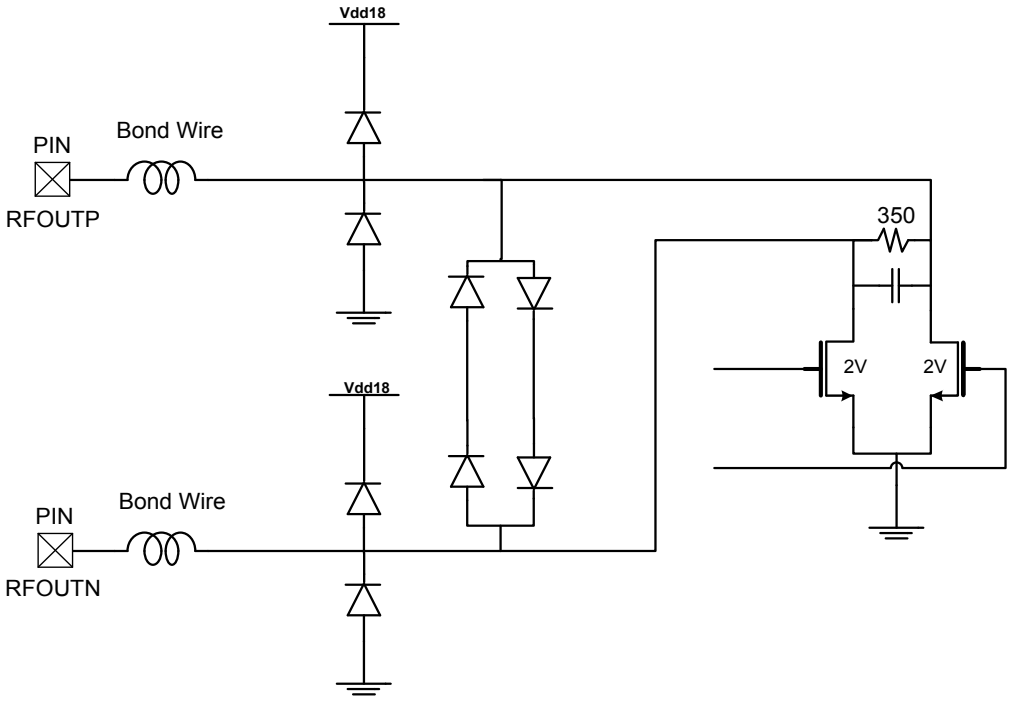
13.2.1. RFINP/RFINN



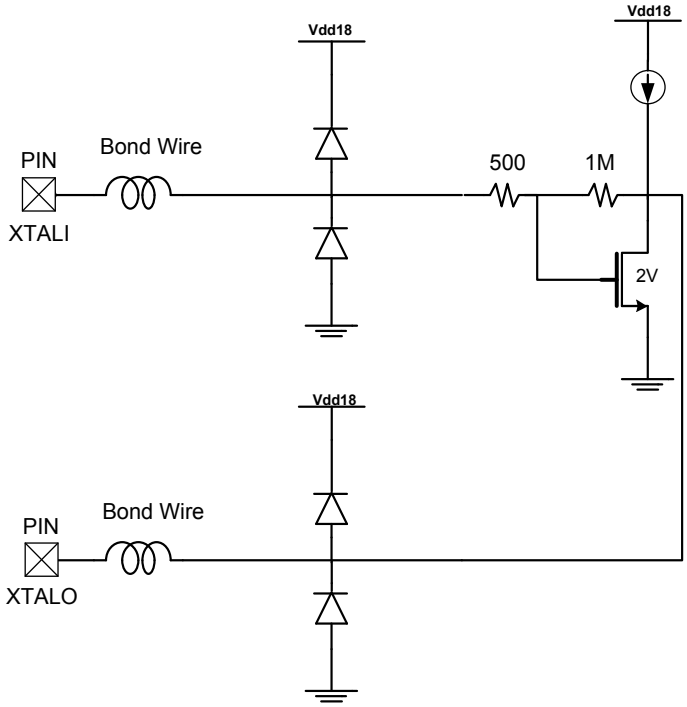
13.2.2. RFFBP/RFFBN



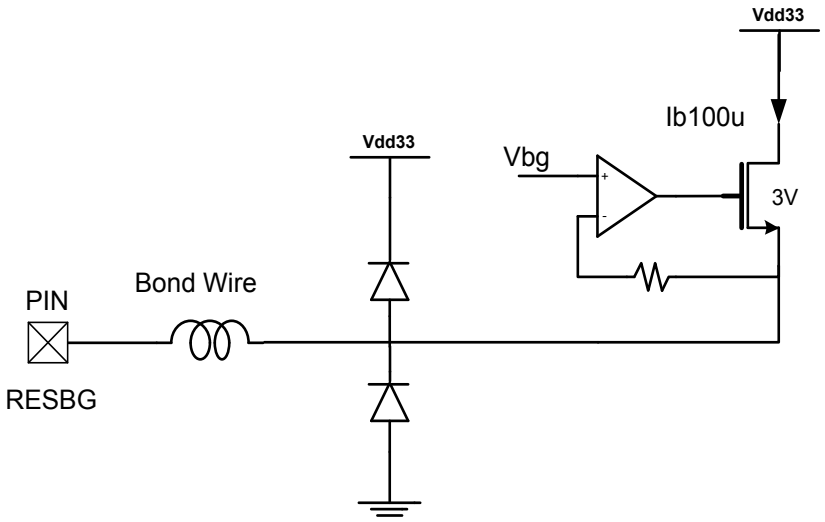
13.2.3. RFOUTP/RFOUTN



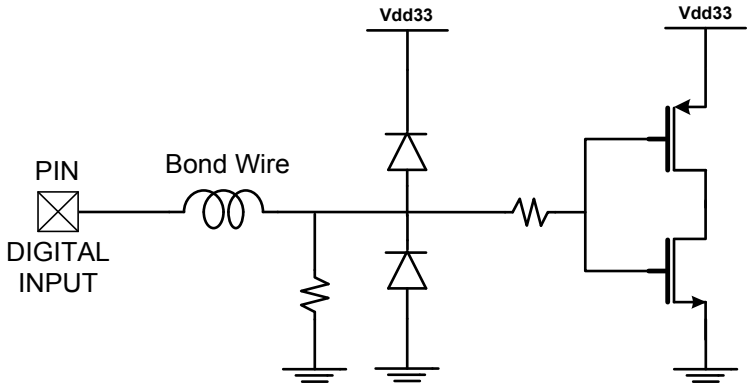
13.2.4. XTALI / XTALO



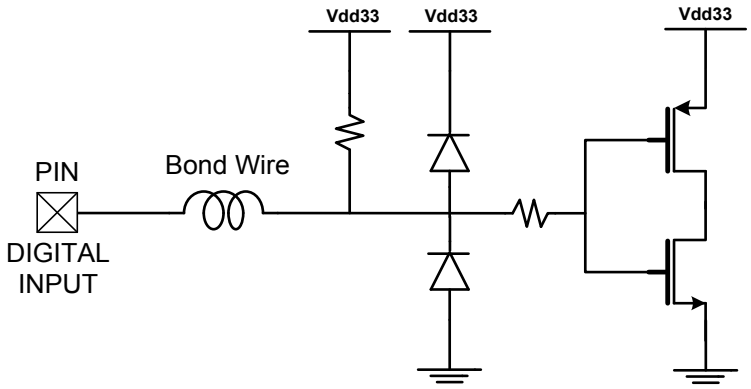
13.2.5. BGRES



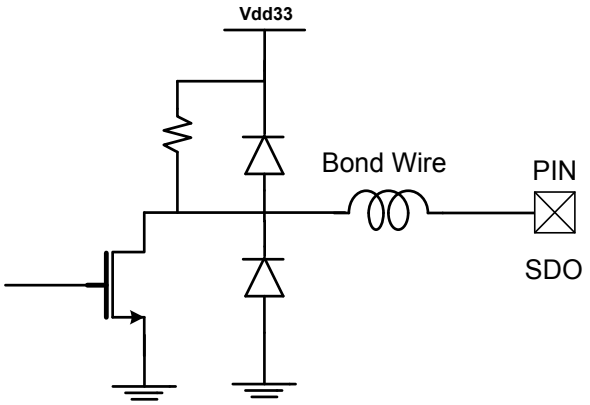
13.2.6. Digital Input with pulldown resistor (SCLK, SDI, LOADENB)



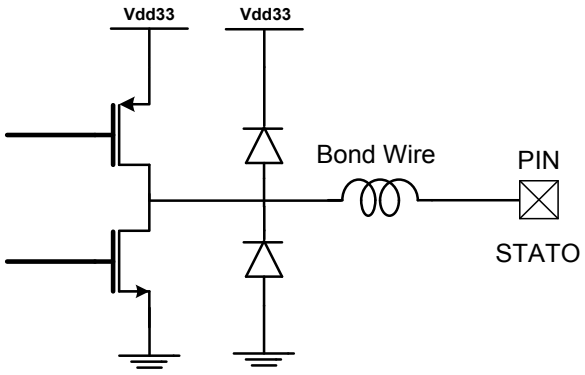
13.2.7. Digital Input with pull up resistor (RESETN, WDTEN, SSN, TXENB)



13.2.8. STATO



13.2.9. SDO



13.3. SC1894 Supply-Pin Current Consumption

Table 13. Approximated SC1894 Supply-Pin Current Consumption, Duty-Cycled Feedback OFF, FW 4.1

Pin #	Pin name	TRACK Mode [1] Current (mA)	Comment
1	DVDD18	6	Quiet digital supply
4	AVDD18	60	Noisy analog supply (RF and digital switching)
5	AVDD33	20	Noisy analog supply (RF)
11	AVDD18	50	Quiet analog supply
12	AVDD18	50	Noisy analog supply (RF)
17	AVDD33	3	Quiet analog supply
22	AVDD18	25	Noisy analog supply (RF)
23	AVDD33	1	Quiet analog supply
28	AVDD33	25	Noisy analog supply (RF)
35	AVDD18	50	Noisy ADC supply (100MHz switching activity) + harmonics of 100MHz
36	AVDD18	50	
41	AVDD18	5	
42	AVDD18	5	
47	AVDD18	1	Crystal oscillator power supply, switching at the reference frequency. Noisy supply.
48,55,59,64 [2]	DVDD18	220	Noisy digital supply pins (20-100MHz switching activity) + harmonics of 100MHz
58	DVDD33	2	Quiet digital pin (EEPROM supply and digital IO supply)

1. Typical current with a 4-carrier WCDMA signal.
2. Pins 48, 55, 59 and 64 are connected to a supply trace. Current consumption reflects the sum of all four pins.

Table 14. SC1894 Approximate Pin Voltages

Pin number	Pin name	Voltage	Unit	Comment
1	DVDD18	1.8	V	
2	MPGOUT0	0	V	Not Supported
3	MPGOUT1	0	V	Not Supported
4	AVDD18	1.8	V	
5	AVDD33	3.3	V	
6	GND	0	V	
7	GND	0	V	
8	RFOUTP	1.8	V	
9	RFOUTN	1.8	V	
10	GND	0	V	
11	AVDD18	1.8	V	
12	AVDD18	1.8	V	
13	MPGOUT2	0	V	Not Supported
14	MPGOUT3	0	V	Not Supported
15	GND	0	V	
16	BGRES	1.24	V	
17	AVDD33	3.3	V	
18	GND	0	V	
19	RFINP	~0.8	V	
20	RFINN	~0.8	V	
21	GND	0	V	
22	AVDD18	1.8	V	
23	AVDD33	3.3	V	
24	ADCIN0P	input		Not Supported
25	ADCIN0N	input		Not Supported
26	ADCIN1P	input		Not Supported
27	ADCIN1N	input		Not Supported
28	AVDD33	3.3	V	
29	GND	0	V	
30	RFFBP	~0.8	V	
31	RFFBN	~0.8	V	
32	GND	0	V	
33	FLTCAP0P	1.25	V	
34	FLTCAP0N	0.45	V	
35	AVDD18	1.8	V	
36	AVDD18	1.8	V	
37	FLTCAP1P	1.25	V	
38	FLTCAP1N	0.45	V	
39	FLTCAP2P	1.25	V	
40	FLTCAP2N	0.45	V	

Pin number	Pin name	Voltage	Unit	Comment
41	AVDD18	1.8	V	
42	AVDD18	1.8	V	
43	FLTCAP3P	1.25	V	
44	FLTCAP3N	0.45	V	
45	XTALI	~1	V	
46	XTALO	~1	V	
47	AVDD18	1.8	V	
48	DVDD18	1.8	V	
49	RESETN	3.3	V	
50	WDTEN	3.3	V	
51	SCLK	0	V	
52	SSN	3.3	V	
53	SDI	input		
54	SDO	3.3	V	
55	DVDD18	1.8	V	
56	DGPIN1 (TXENB)	input		
57	STATO	0	V	
58	DVDD33	3.3	V	
59	DVDD18	1.8	V	
60	LOADENB	0	V	
61	RESERVED0	0	V	
62	RESERVED1	0	V	
63	DGPIN0	input		
64	DVDD18	1.8	V	
65	GNDPAD	0	V	

13.4. Manufacturing Related Information

All manufacturing related information, solder reflow profile, package footprint and material data sheet can be found in the SC1894 data sheet.