

HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

Typical Applications

The HMC3716LPE is ideal for:

- Point-to-Point Radios
- Satellite Communication Systems
- Military Applications
- Sonet Clock Generation

Features

- Ultra Low SSB Phase Noise Floor:
-153dBc/Hz @ 10kHz offset @ 100MHz
- Integrated Output Resistors
- Improved Input Sensitivity
- Lock Detect and Invert Functionality
- 24-Pin 4 x 4mm SMT Package

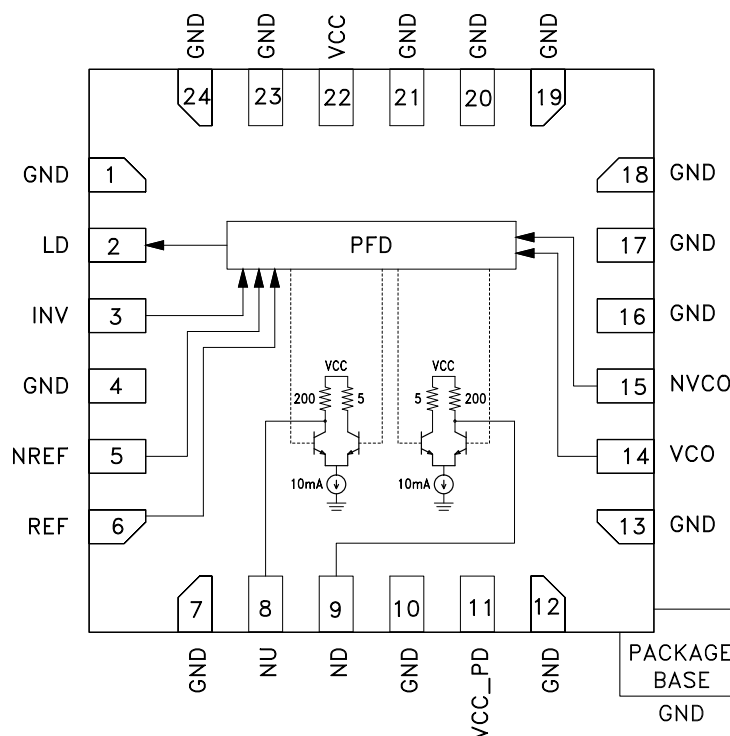
General Description

The HMC3716LP4E is a digital phase frequency detector which operates from 10 to 1300MHz. It is intended for use in low phase noise synthesizer applications.

The combination of high frequency of operation along with its ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast switching and very low phase noise. When used in conjunction with a differential loop amplifier, the HMC3716LP4E generates output voltages that can be used to phase lock a VCO to a reference oscillator.

The device is packaged in a 24-pin, 4 x 4mm leadless QFN surface mount package with an exposed ground paddle for improved RF and thermal performance.

Functional Diagram



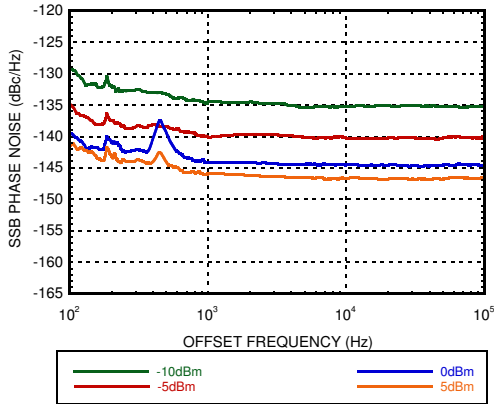
**HBT DIGITAL PHASE FREQUENCY DETECTOR
10 - 1300MHz**
Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|--|------------|------|------------|------------------|
| REF / VCO Input Frequency | Min must be Square Wave Max can be Sine or Square Wave | 10 | 100 | 1300 | MHz |
| Input Power Range | | -10 | 5 | +5 | dBm |
| Output Voltage Swing (NU / ND) | Driving High-Z Load / Op-Amp | | 2 | | V _{p-p} |
| PFD Gain | Gain = $V_{pp} / 2\pi$ Rad | | 0.32 | | V / Rad |
| SSB Phase Noise [1] | @ 10kHz Offset with 100 MHz REF / VCO @ +5 dBm | | -153 | | dBc/Hz |
| Logic Input Voltage (INV) | CMOS / TTL Logic Low CMOS / TTL Logic High | 0.0 1.8 | | 1.1 5.0 | V |
| Lock Detect Output Voltage | Filtering & 1k Ω Pull-Up Required CMOS / TTL Logic Low = Unlocked MOS / TTL Logic High = Locked | 0.0 2.7 | | 0.5 5.0 | V |
| Lock Detect Sink Current | | | 5 | | mA |
| Supply Voltage (V _{CC}) | | 4.75 | 5.00 | 5.25 | V |
| Supply Current (I _{CC}) | V _{CC} = 5.0V | | 115 | | mA |
| Temperature Range | | -40 | | +85 | $^\circ\text{C}$ |

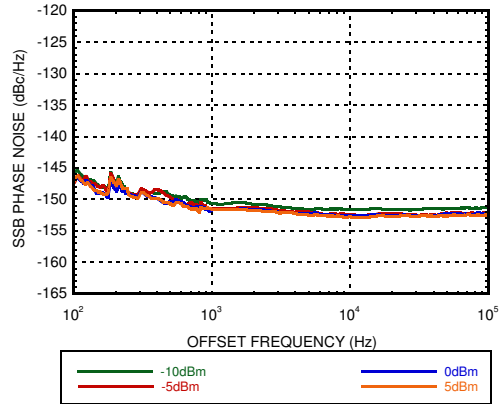
[1] Square wave input achieves best phase noise at lower REF/VCO frequencies (see comparison plots on preceding page)

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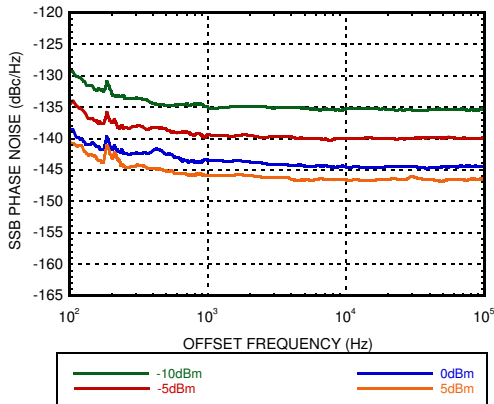
**Phase Noise Floor, Vcc = 4.75V
REF = 100MHz Sine Wave**



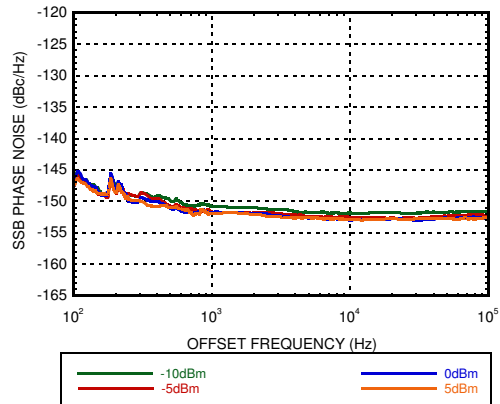
**Phase Noise Floor, Vcc = 4.75V
REF = 100MHz Square Wave**



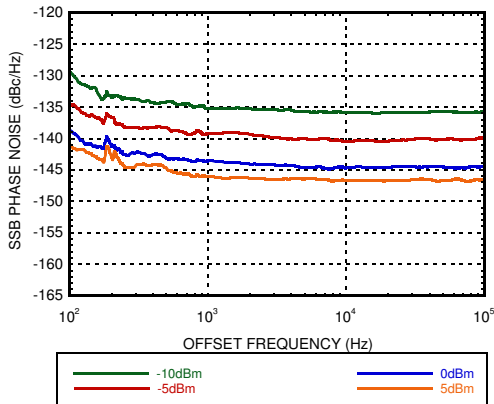
**Phase Noise Floor, Vcc = 5.00V
REF = 100MHz Sine Wave**



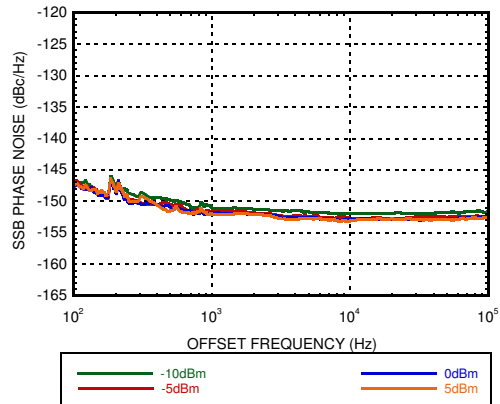
**Phase Noise Floor, Vcc = 5.00V
REF = 100MHz Square Wave**



**Phase Noise Floor, Vcc = 5.25V
REF = 100MHz Sine Wave**

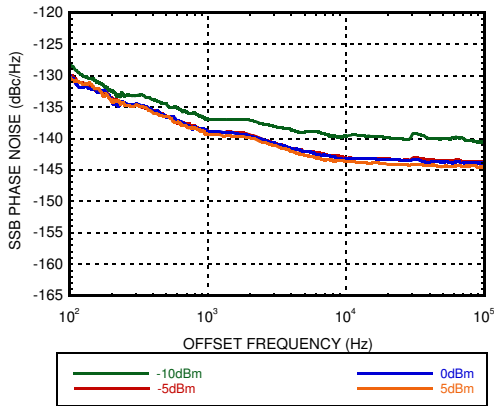


**Phase Noise Floor, Vcc = 5.25V
REF = 100MHz Square Wave**

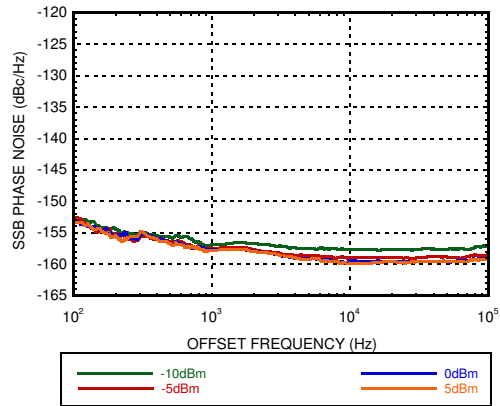


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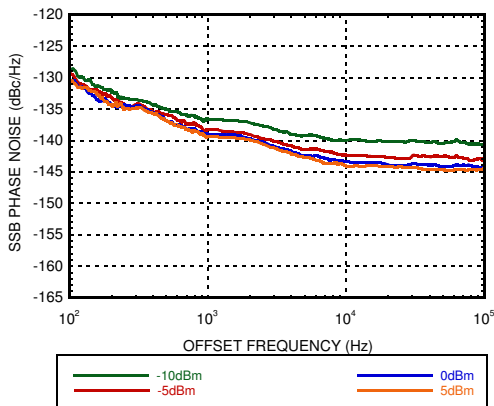
**Phase Noise Floor, Vcc = 4.75V
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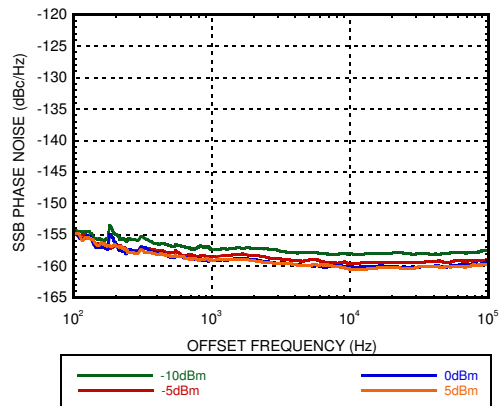
**Phase Noise Floor, Vcc = 4.75V
REF = 10MHz Square Wave**



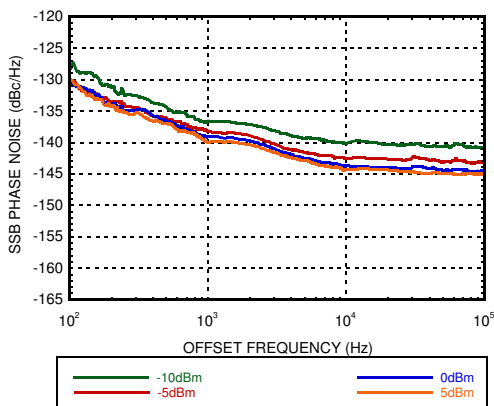
**Phase Noise Floor, Vcc = 5.00V
REF = 1000MHz Sine Wave**



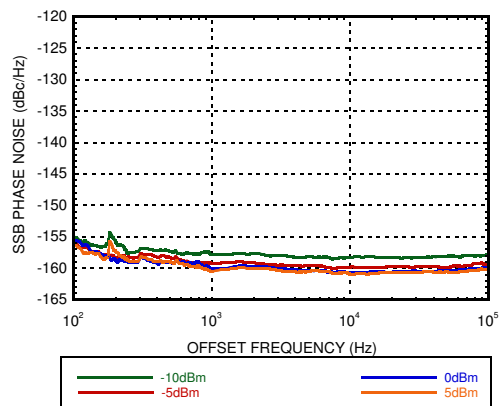
**Phase Noise Floor, Vcc = 5.00V
REF = 10MHz Square Wave**



**Phase Noise Floor, Vcc = 5.25V
REF = 1000MHz Sine Wave**

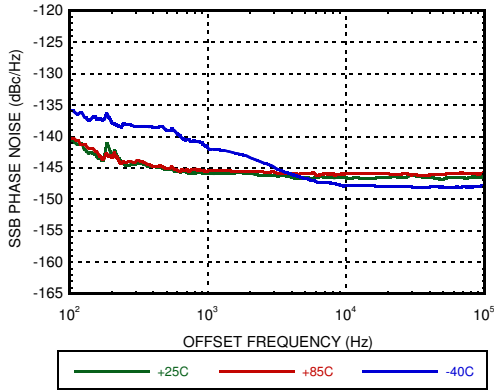


**Phase Noise Floor, Vcc = 5.25V
REF = 10MHz Square Wave**

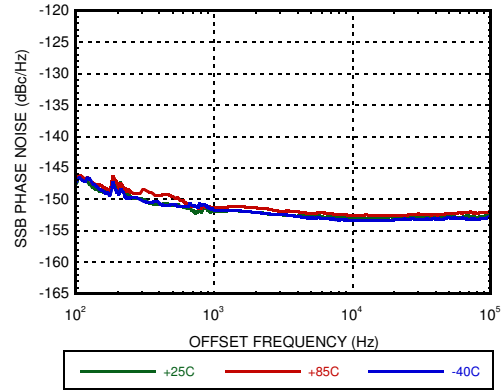


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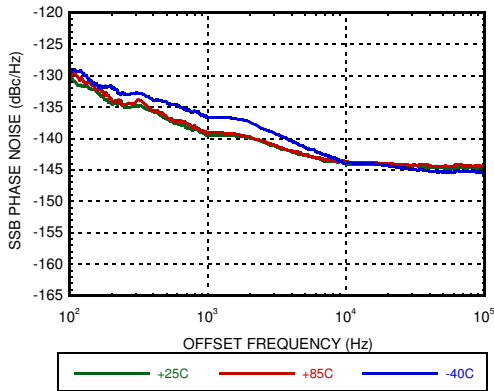
**Phase Noise Floor, Vcc = 5.00V
REF = 100MHz Sine Wave**



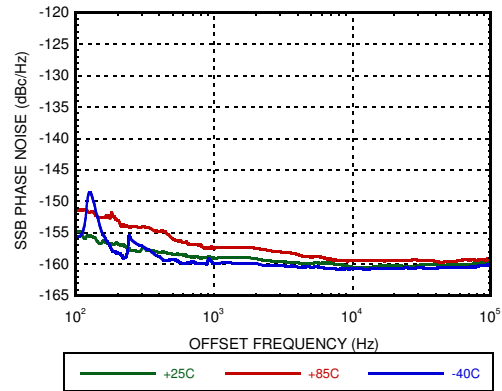
**Phase Noise Floor, Vcc = 5.00V
REF = 100MHz Square Wave**



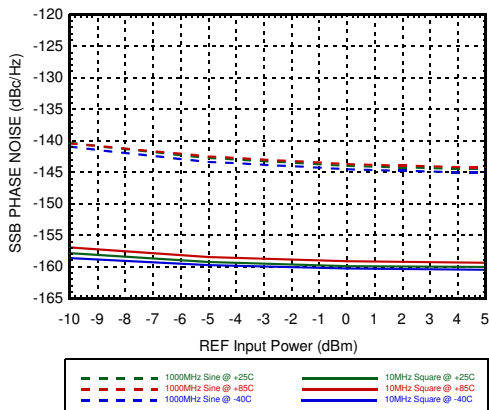
**Phase Noise Floor, Vcc = 5.00V
REF = 1000MHz Sine Wave**



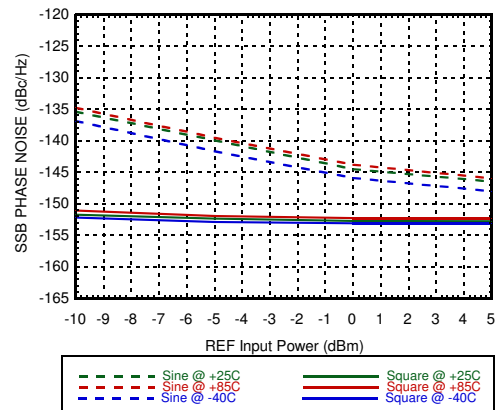
**Phase Noise Floor, Vcc = 5.00V
REF = 10MHz Square Wave**



**Phase Noise Floor, Vcc = 5.00V
REF = 10 & 1000MHz, ≥10kHz offset**

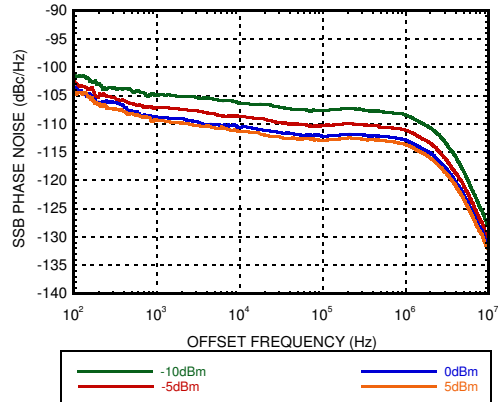


**Phase Noise Floor, Vcc = 5.00V
REF = 100MHz, ≥10kHz offset**

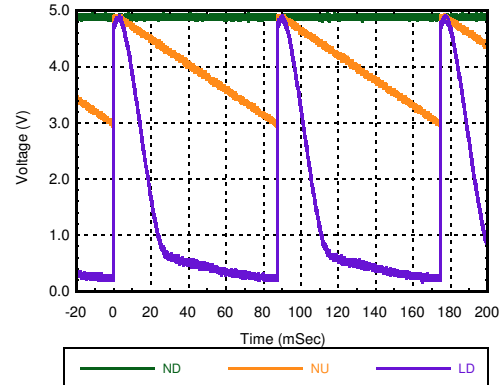


HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

**Typical PLL Performance, $V_{CC} = 5.00V$
REF = 100MHz Square Wave
VCO = 10GHz, $N = 100$, $T = +25C$**



**PFD Outputs ND, NU, LD, $V_{CC} = 5.00V$
Forced PFD Difference $\approx 11Hz$
High-Z Scope, $BW = 20MHz$, $T = +25C$**



Typical Supply Current vs. V_{CC}

| V_{CC} (Vdc) | I_{CC} (mA) |
|----------------|---------------|
| 4.75 | 107 |
| 5.00 | 115 |
| 5.25 | 123 |

Typical ND & NU Voltages, $V_{CC} = +5V$

| Symbol | Characteristics | +25C | | | Units |
|----------|---------------------|------|------|------|-------|
| | | Min. | Typ. | Max. | |
| V_{OH} | Output High Voltage | 4.9 | 5.0 | 5.1 | V |
| V_{OL} | Output Low Voltage | 2.9 | 3 | 3.1 | V |

Reliability Information

| | |
|--|---------------|
| Junction Temperature To Maintain 1 Million Hour MTTF | 135 °C |
| Nominal Junction Temperature ($T = +85$ °C) | 99.3 °C |
| Thermal Resistance (junction to ground paddle) | 24.9°C/W |
| Operating Temperature | -40 to +85 °C |

Absolute Maximum Ratings

| | |
|-----------------------------|----------------------------|
| RF Input ($V_{CC} = +5V$) | +13 dBm |
| Supply Voltage (V_{CC}) | +5.5V |
| Logic Inputs (INV) | -0.5 to (0.5V + V_{CC}) |
| PFD Outputs (ND, NU) | 2.5 to (0.5V + V_{CC}) |
| Storage Temperature | -65 to +150 °C |
| ESD Sensitivity (HBM) | Class 1B |
| ESD Sensitivity (CDM) | Class C2 |



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Notes:

- All data shown is typical and actual performance may vary depending upon implementation.
- Phase Noise data taken utilizing 2-unit PLL cancellation method with $VCO \geq 2400MHz$ and healthy power level.
- Only one PFD output will be active with a forced frequency difference, depending upon which input frequency is higher.
- Without oscilloscope bandwidth limiting, there will be narrow pulses on NU, ND, & LD, at the input frequencies. These pulses may create spectral content, which is normally suppressed with the loop filter and lock detect filter.

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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|----------|--|---------------------|
| 1, 4, 7, 10, 12, 13, 16 - 21, 23, 24, Paddle | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC ground. | |
| 2 | LD | Lock Detect Output Open collector pulsed output. Requires external 1kΩ Pullup to Vcc and filtering. Average "LOW" = UNLOCKED Average "HIGH" = LOCKED | |
| 3 | INV | PFD INVERT Function to swap REF & VCO CMOS / TTL compatible Logic "LOW" = NORMAL Logic "HIGH" = INVERT | |
| 11 | Vcc_PD | Supply Voltage, +5.00V | |
| 22 | Vcc | | |
| 8 | NU | Up Output Do not load output below 2.5V or damage can occur. | |
| 9 | ND | Down Output Do not load output below 2.5V or damage can occur. | |
| 5 | NREF | Differential REF Inputs Pins are DC coupled, External DC blocks required | |
| 6 | REF | | |
| 14 | VCO | Differential VCO Inputs Pins are DC coupled, External DC blocks required | |
| 15 | NVCO | | |

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PFD Functionality

The phase frequency detector functionality of the HMC3716LP4E is such that it compares the rising edge the two input signals (REF / VCO). This information is then used to pulse the ND and NU outputs depending upon which input signal is greater in frequency.

Under normal operation the ND pin will be active when VCO frequency is greater than the REF frequency; NU would remain constant. Conversely, when the VCO frequency is lower than the REF frequency, then NU would be active and ND would remain constant. Here, the term “active” means that the output will on average, vary between 3 - 5V, and the term “remain constant” means that the output will remain at approximately 5V.

INVERT Functionality

The INV pin effectively swaps the REF and VCO input signals, such that the NU and ND pin responses are swapped. This has the advantage of easily correcting a layout issue if the loop filter op-amp inputs were swapped.

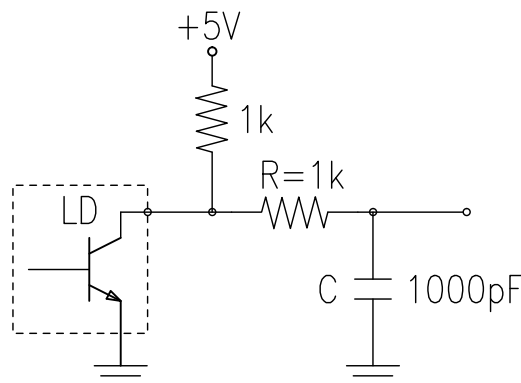
A logic “LOW” on this pin will configure the device for normal operation, and a logic “HIGH” cause the input signals to swap. The evaluation board has a 10kΩ resistor pull up resistor to 5V. A jumper must be installed connecting the INV pin to ground for normal operation.

Lock Detect Functionality

The LD pin is an open collector pulsed output transistor. It requires an external 1k pull up resistor to Vcc (5V), as well as a simple RC filter.

Since the pin will produce very narrow pulses at each zero crossing of the REF and VCO input signals, filtering is necessary to create an average voltage which can be used to drive an LED or system input logic. When the device is “LOCKED”, that transistor will effectively be “OFF”, and the filtered output voltage will be “HIGH”.

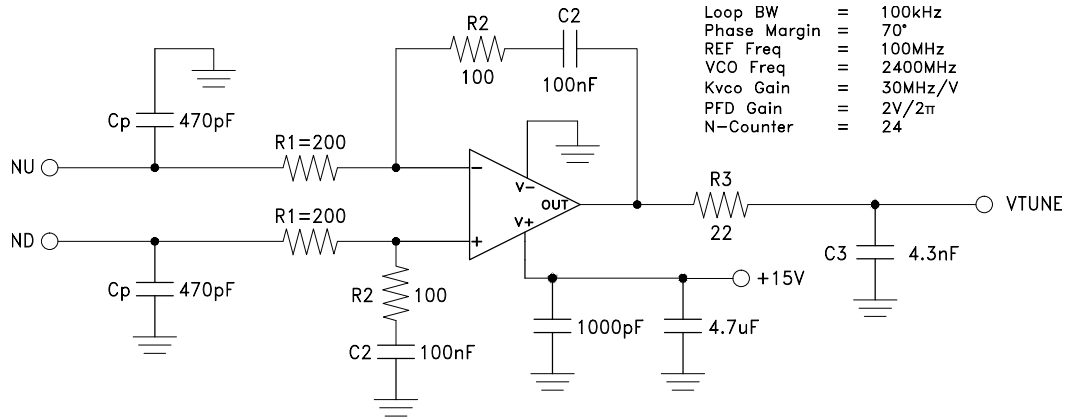
Below is an example of an RC filter for the lock detect pin. The value of resistor “R” should be greater than 100Ω to limit any surge current from flowing when the output transistor is “ON”. The value of capacitor “C” should be selected such that the filter cutoff is much less than the REF frequency, but not excessively large (slow) that it will inhibit detection of lock status.



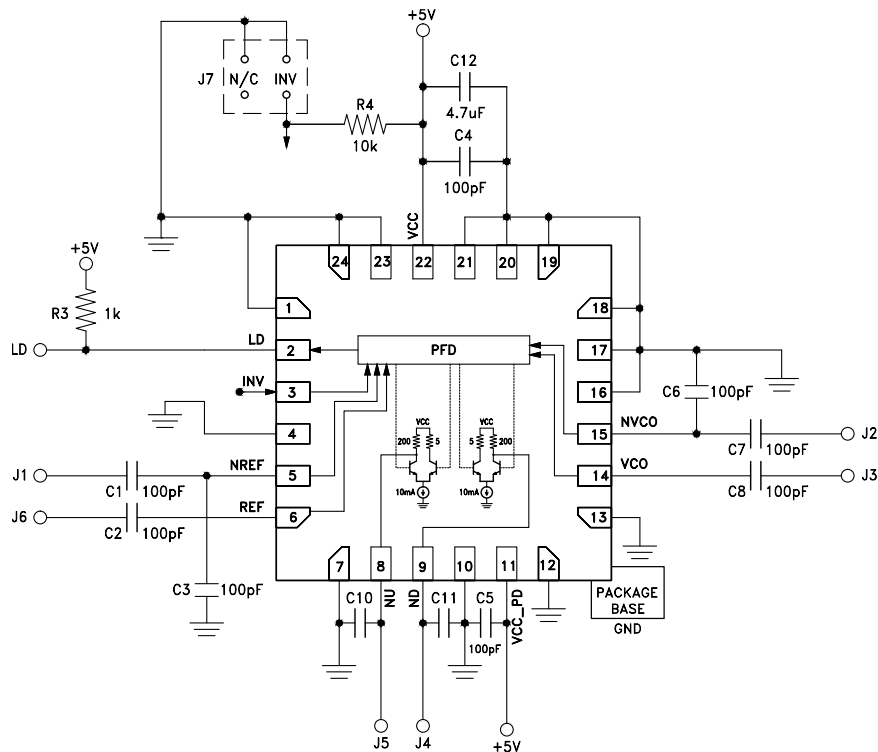
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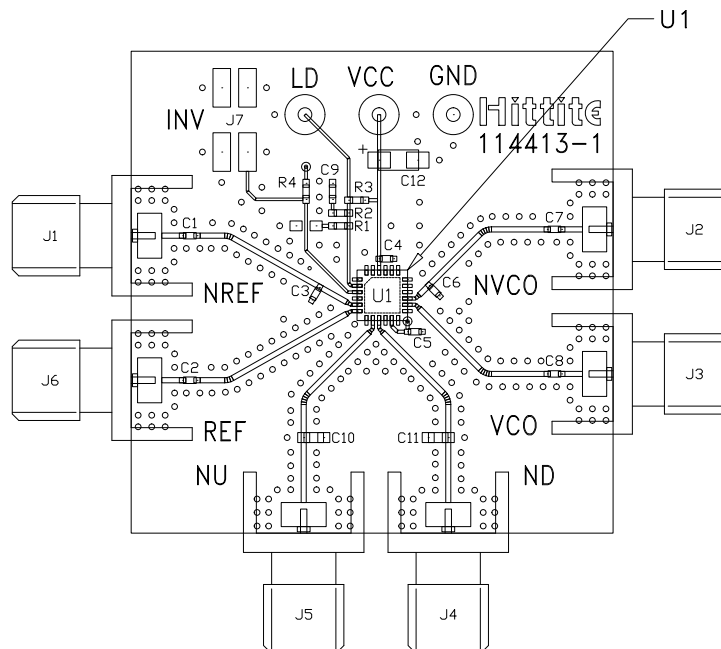
Typical Loop Filter

A differential op-amp loop filter is required in order to integrate the ND and NU pulses into a usable tune voltage to drive the oscillator in a PLL. The loop filter synthesis can be performed using a variety of simulation tools. Below is an example of a third-order filter produced with the listed PLL parameters for loop bandwidth, etc.



Evaluation PCB Circuit



**HBT DIGITAL PHASE FREQUENCY DETECTOR
10 - 1300MHz**
Evaluation PCB


The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50Ω impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes.

List of Materials for Evaluation PCB EV1HMC3716LP4 [1]

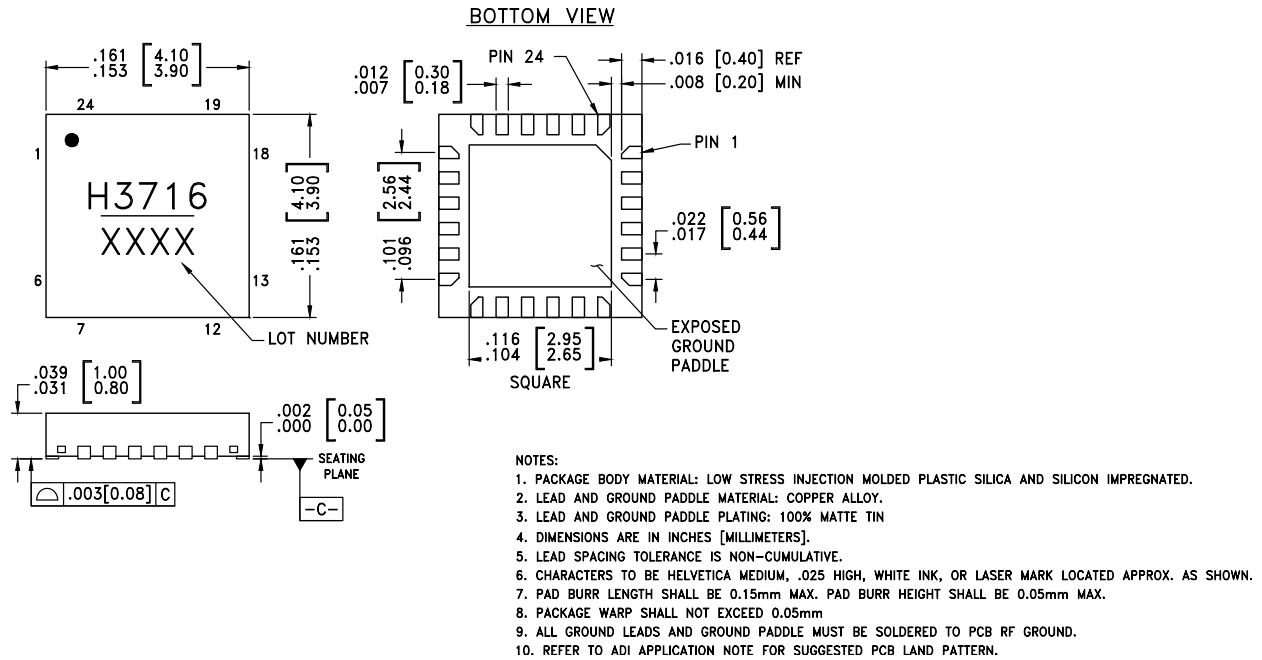
| Item | Description |
|------------------|--|
| PCB [2] | 114413 Eval Board |
| U1 | HMC3716LP4E, PFD w/ Lock Detect and Invert functions |
| J1 - J6 | PCB Mount SMA RF Connector |
| J7 | 2mm, 4-pin DC Header (cut to fit) |
| Qty 1 | 2mm Shunt/Jumper |
| C1 - C8 | 100pF Ceramic Capacitor, 5%, 50V, 0402 |
| C12 | 4.7μF, Tantalum Capacitor, 16V, 20%, 3216 |
| R3 | 1kΩ Resistor, 5%, 1/10W, 0402 |
| R4 | 10kΩ Resistor, 5%, 1/10W, 0402 |
| R1, R2, C9 - C11 | Do Not Install |

[1] Reference this part number when ordering complete PCB

[2] Circuit Board Material: Rogers 4350

HBT DIGITAL PHASE FREQUENCY DETECTOR
10 - 1300MHz

Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC3716LP4E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[1] | H3716 XXXX |

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX