Nuvoton
N-Channel FET Synchronous Buck Regulator Controller
W83320G

W83320G

Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	N.A.	N.A.	0.50	N.A.	All version before 0.5 are for internal use only.
2	N.A.	N.A.	0.51	N.A.	Add Pb-free part no :W83320G
3	9,10.	Oct./05	0.52	N.A.	To modify the application circuit.
4.	N.A	Oct./06	1.0	1.0	1.Remove non Pb-free part no:W83320S 2. All versions before 1.0 are preliminary versions.
5.	10	Apr./08	1.1	1.1	Add Absolute Maximum Rating

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LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

The W83320G is a high-speed, N-Channel synchronous buck regulator controller optimized for wide reference input range. The W83320G employs adjustable frequency ranging from 100 KHz to 400 KHz voltage-mode PWM control architecture. The regulator is biased from a 5V rail and the power for the high-side MOSFET can be supplied by a separate 12V rail or supplied from the internal charge pump.

A Current limit protection is implemented by monitoring the voltage drop across the switch ON resistance of the low-side MOSFET. This method can eliminate the requirement of extra current sensing resistor and avoids false trigger of OC protection when V_{IN} varies efficiently. The adaptive non-overlapping MOSFET gate drivers help avoid potential shoot-through problems while maintaining high efficiency. All these together with Power-good flag, enable and soft start features make power sequencing easy.

2. FEATURES

- 1.8V to 5V power stage input voltage
- Providing +/-1.5% reference voltage
- Power Good flag
- Current limit without sense resistor
- Soft start
- Switching frequency from 100 kHz to 400 kHz
- Tiny plastic SOP-14 package

3. APPLICATIONS

- DDR SDRAM and AGP core power for Desktop PC
- Set-Top Boxes/ Home Gateways
- Core Logic Regulators
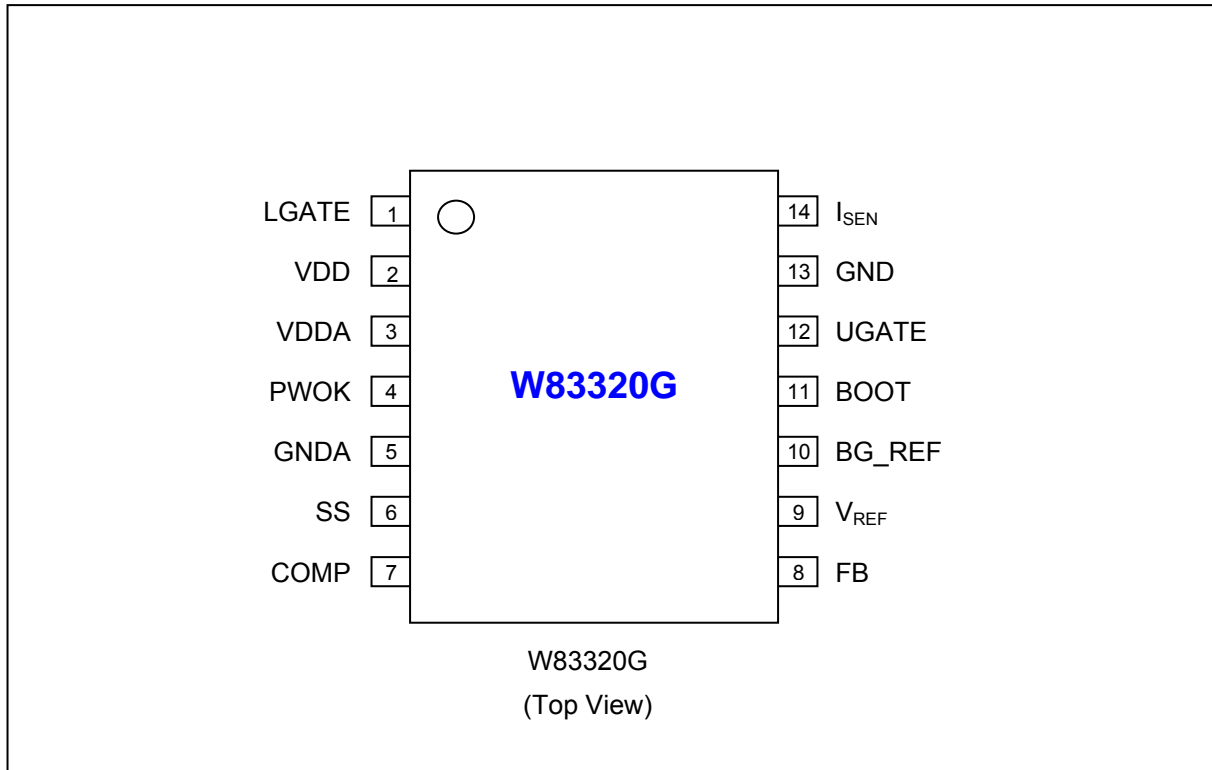- High-Efficiency Buck Regulation

4. PIN-OUT

Figure1. W83320G Pin-out

5. PIN DESCRIPTION

| PIN	NAME	FUNCTION
1	LGATE	Low-Side N-Channel MOSFET Gate Drive Pin. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET turned off.
2	VDD	+5V supply rail for the lower gate driver and control logic circuit.
3	VDDA	VDDA: +5V supply rail for the chip.
4	PWROK	Power OK. Open drain output. This pin will be opened in following conditions: 1. No over-current detected; 2. V_{REF_IN} >0.6V; 3. FB > 75% of V_{REF_IN}; 4. SS >3V.
5	GNDA	Ground for analog circuit. Connect it to system ground.
6	SS	Soft Start Pin. A capacitor should be attached in this pin to ground for soft start output clamping. This capacitor, along with an internal 12uA current source, set the output clamp ramp up speed.
7	COMP	Internal Error Amplifier Output Pin. This pin is available for compensation of the control loop.
8	FB	Inverting Input of the Error Amplifier. This pin is available for compensation of the control loop.
9	V_{REF}	Non-inverting Input of the Error Amplifier. Voltage on this pin provides reference input to the PWM control loop. When the V_{REF_IN} voltage is less than 0.27V, the PWM is shut-down and the UGATE and LGAET are driven low. Due to its wide input range (0 ~ 3.6V), the V_{REF_IN} voltage can be raised slowly to perform the input clamp function. Besides, a special function is implemented in this IC to inform the reference provider of over current alarm. Each time as the OC occurs, V_{REF_IN} will be short to GND (through 170 ohms) for about 5~10uS. The reference provider can be aware of the OC condition by detecting this pulse.
10	BG_REF	Internal Band gap Reference Voltage Output.
11	BOOT	Supply rail for the high-side MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage or a separate 12V supply can be used.
12	UGATE	High-Side N-Channel MOSFET Gate Drive Pin. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the high-side MOSFET has turned off.
13	GND	Ground for signal level circuit. Connect it to system ground.
14	I_{SEN}	Current limit threshold setting. Connect a resistor (R_{OCSET}) between this pin and the drain of the low-side MOSFET. An internal 72uA current source will flow through R_{ISEN} and cause a fixed voltage drop on it while the low-side MOSFET is turned on. In the mean while, the W83320G compares the voltage drop with the voltage across the low-side MOSFET and determines whether the current limit has been reached. The equation for over-current limit is: $I_{LIM} = (72uA * R_{ISEN})/R_{DSON}$

6. INTERNAL BLOCK DIAGRAM
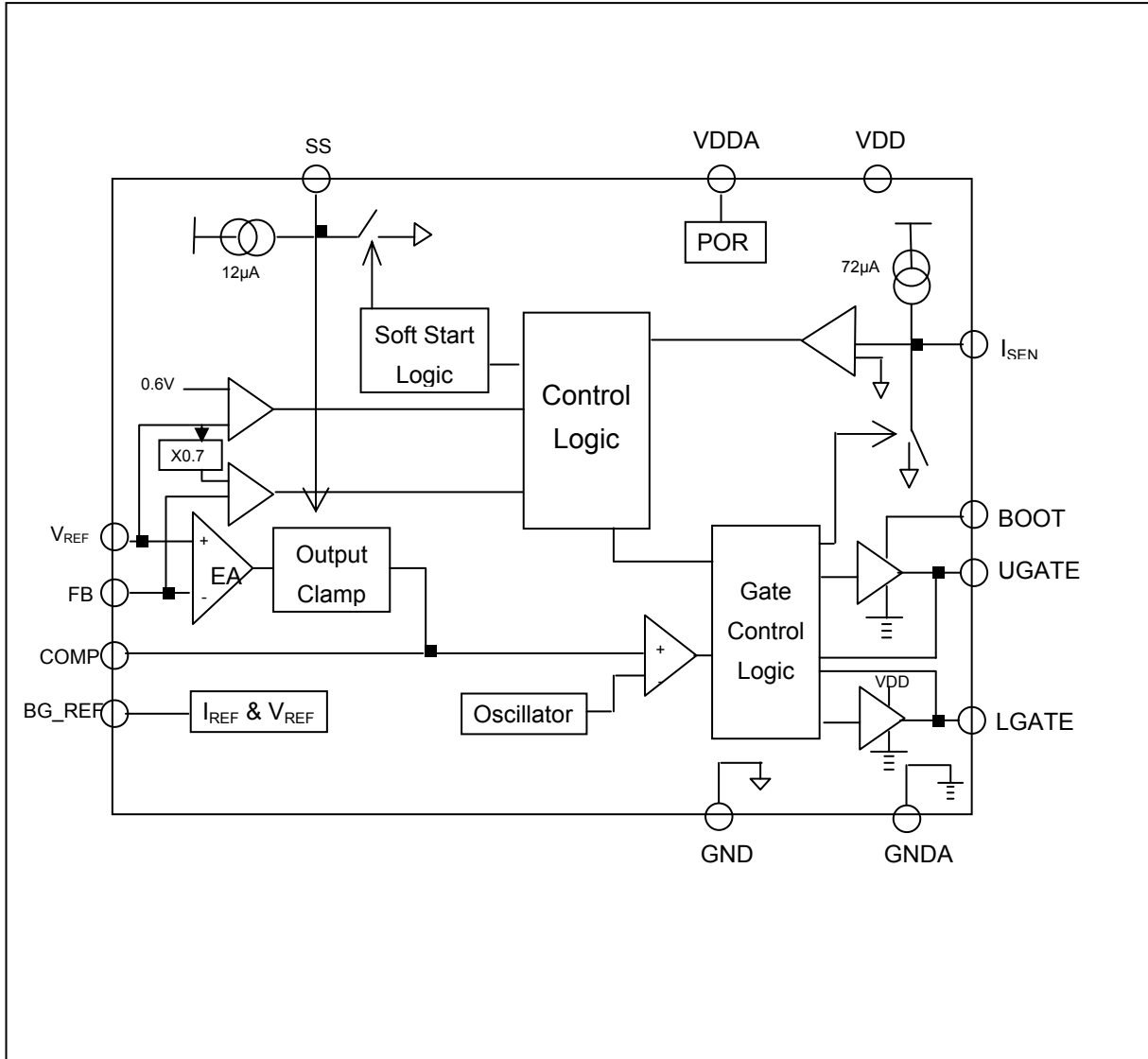
Figure2. W83320G Block Diagram

Soft-Start

When V_{DDA} and V_{DD} ramp over 4.3V and the voltage at pin V_{REF} ramps over 0.27V; the soft start capacitor begins to charge through an internal 12uA ($I_{REF}/2$) current source. The error amplifier (and the PWM duty) is both output clamped by the voltage on soft-start pin V_{SS} and input clamped by the voltage on V_{REF}. There are two ways to soft start the power that's following the rising of the slower one between V_{SS} or V_{REF}; during soft-start, PWOK is forced to low and the internal Over-Current Protection is triggered to work. 0.4V to 1.9V of V_{SS} is roughly mapping to 0 to 100% pulse-width. Smaller than 0.27V on V_{REF} will disable the PWM controller and discharge C_{SS}.

MOSFET Gate Drivers

The power for the high-side driver is flowing through the BOOT pin. This voltage can be supplied by a separate, higher voltage source, or supplied from a local charge pump structure or combination of the two.

Since the voltage of the low-side MOSFET gate and the high-side MOSFET gate are being monitored to determine the state of the MOSFET, it should be taken carefully to add external components between the gate drivers and their respective MOSFET gates. Doing so may interfere with the shoot-through protection.

Current Limit

Current limit is implemented by sensing the voltage across the low-side MOSFET while it is ON. This method enhances the converter's efficiency and reduces total cost by eliminating a current sensing resistor.

While low-side MOSFET is turned on, a constant current of 72uA (I_{REF} X 3) is forced through R_{OCSET} which is an external resistor connected between phase and I_{SEN}, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the chip enters current limit mode. In the current limit mode both the high-side and low-side MOSFETS are turned off and the soft start capacitor C_{SS} will be discharged immediately. The V_{REF} is shorted to GND for 5~10uS to indicate the over current condition. After a 5mS delay, a soft-start cycle is initiated. If the cause of the over-current is still present after the delay interval, the current limit would be triggered again. The shut down - delay - soft start cycle will be repeated indefinitely until the over-current event been removed.

Input Tracking

When the V_{REF} voltage is less than 0.3V, the PWM is shut-down and the UGATE and LGATE are driven low. Due to its wide input range (0 ~ 3.6V), this chip is suitable for reference input tracking application. But note that the chip will be shut-down when V_{REF} <0.27V, a proper setting of C_{SS} is needed to clamp the output at initiation of start up and avoid output voltage step-up (and so a large inrush current).

I_{REF} and PWM Clock

The Internal reference current (I_{REF}) is determined by the resistor between pin BG_REF pin and GND (R_{SET}) according to the following equation:
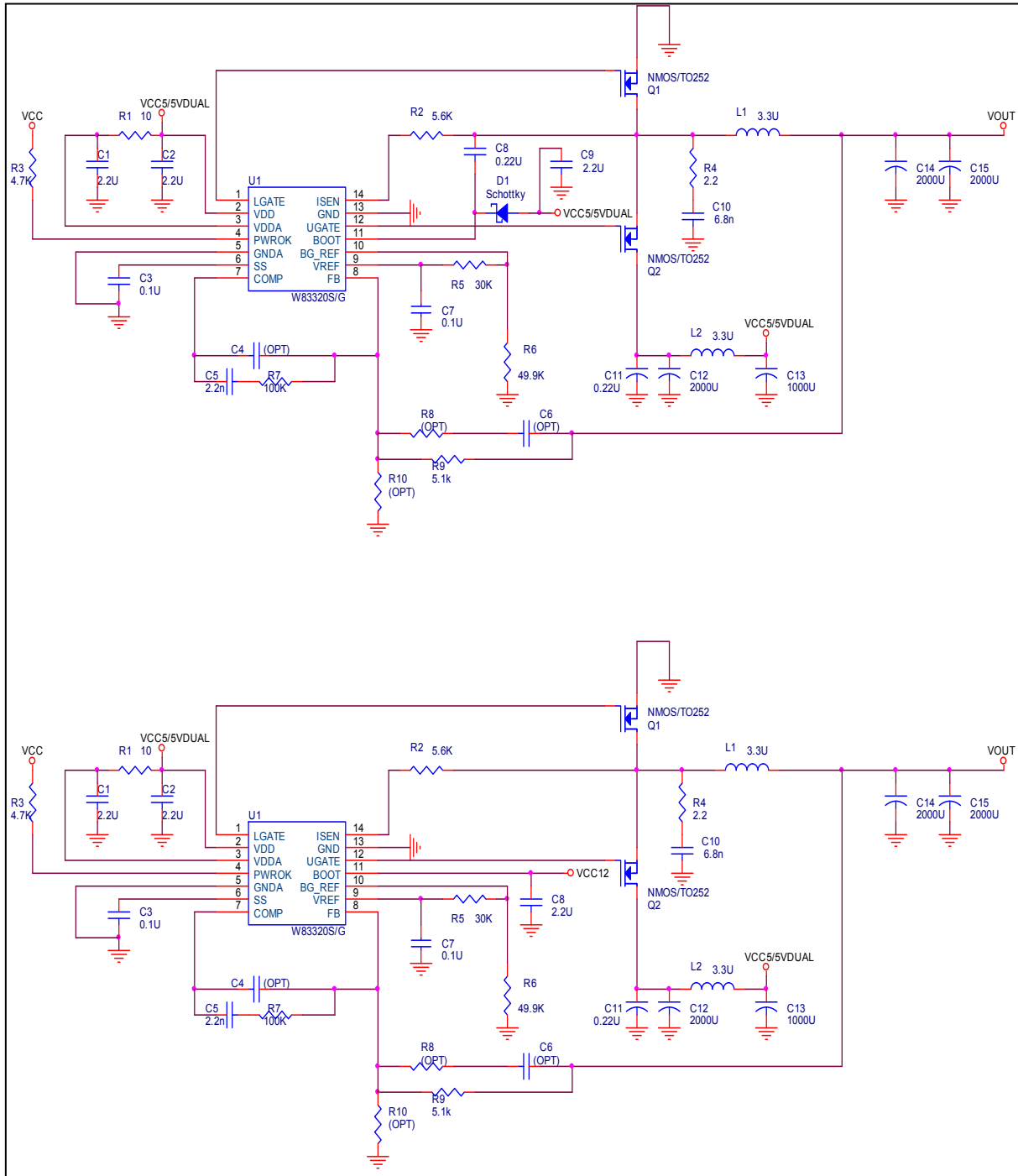
$$I_{REF} = 1.19V/ R_{SET}$$

The nominal 200 kHz PWM clock can be adjusted ranging form 100 kHz to 400 kHz by changing I_{REF} according to the following equation:
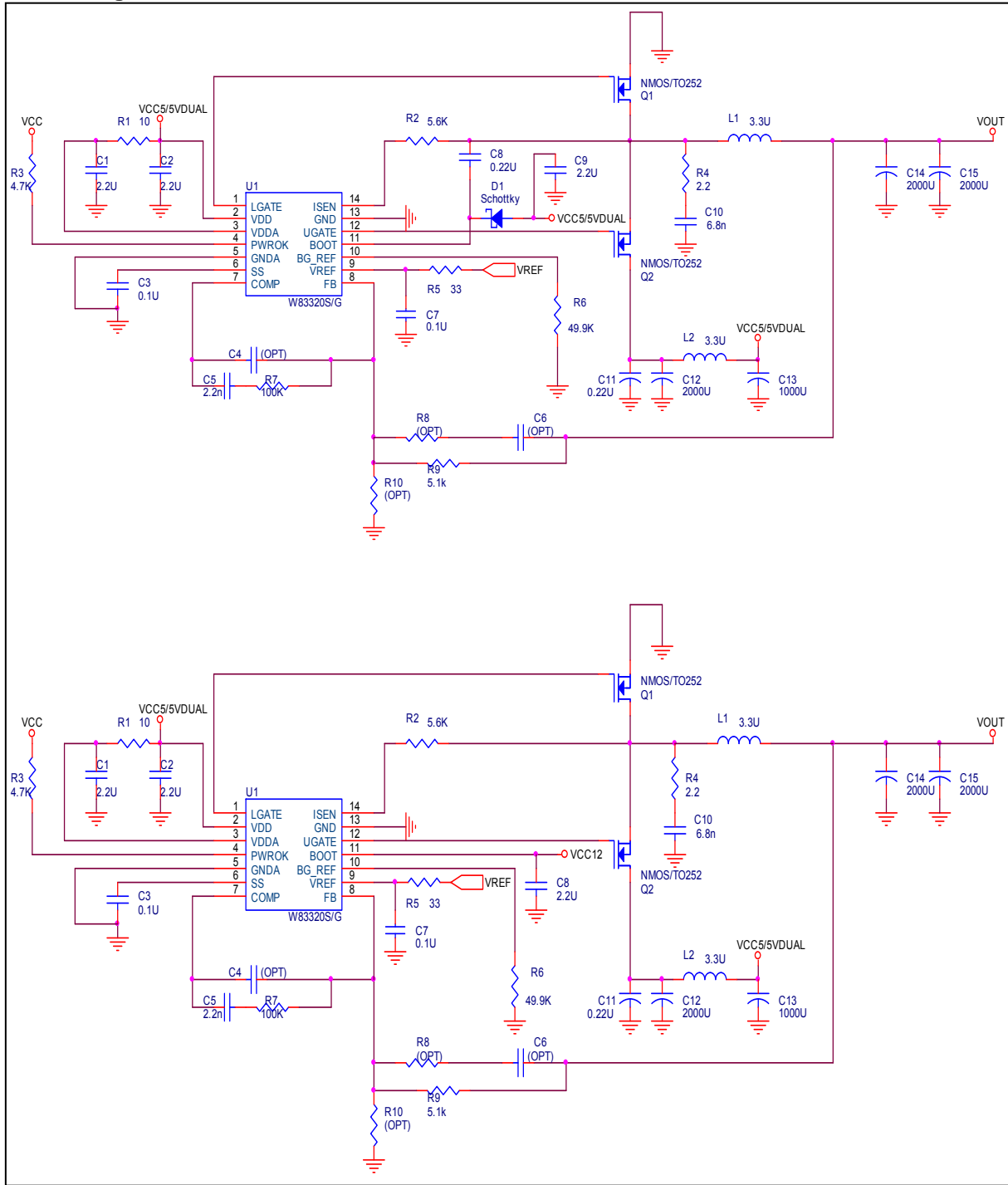
$$Freq = 200\ KHz * I_{REF} / 24uA;$$

7. APPLICATION CIRCUIT

● **Standalone mode with internal 1.19V V$_{REF}$**

### ● Tracking mode with external V_{REF}

8. ABSOLUTE MAXIMUM RATINGS

- Supply Voltage VDD/VDDA --- 6V
- BOOT & UGATE to GND --- 15V
- Package Thermal Resistance SOP-14, θ_{JA} ----------------------------------- 128°C/W
- Ambient Temperature Range --- 0°C~+70°C
- Junction Temperature Range --- -40°C~+125°C
- Storage Temperature Range --- -65°C~+150°C
- Electrostatic discharge protection (ESD) Human Body Mode ----------------------- $\pm$2KV

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9. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V$_{CC}$ SUPPLY CURRENT						
Nominal Supply	I$_{CC}$	EN=V$_{CC}$; UGATE and LGATE Open	-	3	-	mA
POWER-ON RESET						
Rising V$_{DD}$ Threshold			-	4.3	-	V
Falling V$_{DD}$ Threshold			-	3.7	-	V
V$_{REF}$ Enable			-	0.27	-	V
OSCILLATOR						
Free Running Frequency		R$_{SET}$=49.6K	160	200	240	kHz
Ramp Amplitude	ΔV$_{OSC}$	R$_{SET}$=49.6K	-	1.5	-	V$_{P-P}$
REFERENCE						
Reference Voltage Tolerance	V$_{REF}$		-1.5	-	1.5	%
Reference Voltage			-	1.19	-	V
ERROR AMPLIFIER						
DC Gain			-	80	-	dB
Gain-Bandwidth			-	5	-	MHz
Slew Rate			-	4	-	V/$_{μS}$
GATE DRIVERS						
High-side Gate Source	I$_{HGATE-SRC}$	V$_{BOOT}$=12V,V$_{UGATE}$=6V	250	-	-	mA
High-side Gate Sink	I$_{HGATE-SNK}$	V$_{BOOT}$=12V,V$_{UGATE}$=6V	600	-	-	mA
Low-side Gate Source	I$_{LGATE-SRC}$	V$_{CC}$=5V, V$_{LGATE}$=2.5V	250	-	-	mA
Low-side Gate Sink	I$_{LGATE-SNK}$	V$_{CC}$=5V, V$_{LGATE}$=2.5V	300	-	-	mA
PROTECTION						
I$_{SEN}$ Current Source	I$_{SEN}$		64	72	80	μA
Soft-Start Current	I$_{SS}$		10	12	14	μA

10. TYPICAL PERFORMANCE CHARACTERISTICS

- Power start up with condition: no loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.

Ch1: V_{CC}
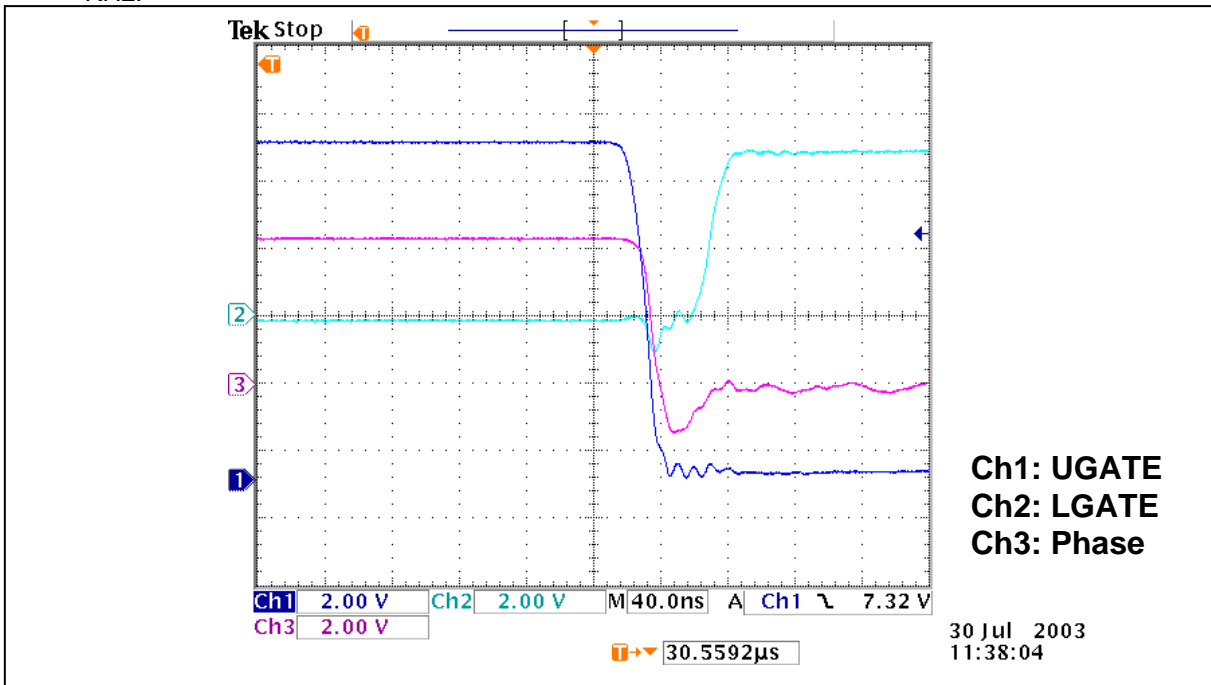Ch2: V_{REF}
Ch3: V_{OUT}
Ch4: PWROK
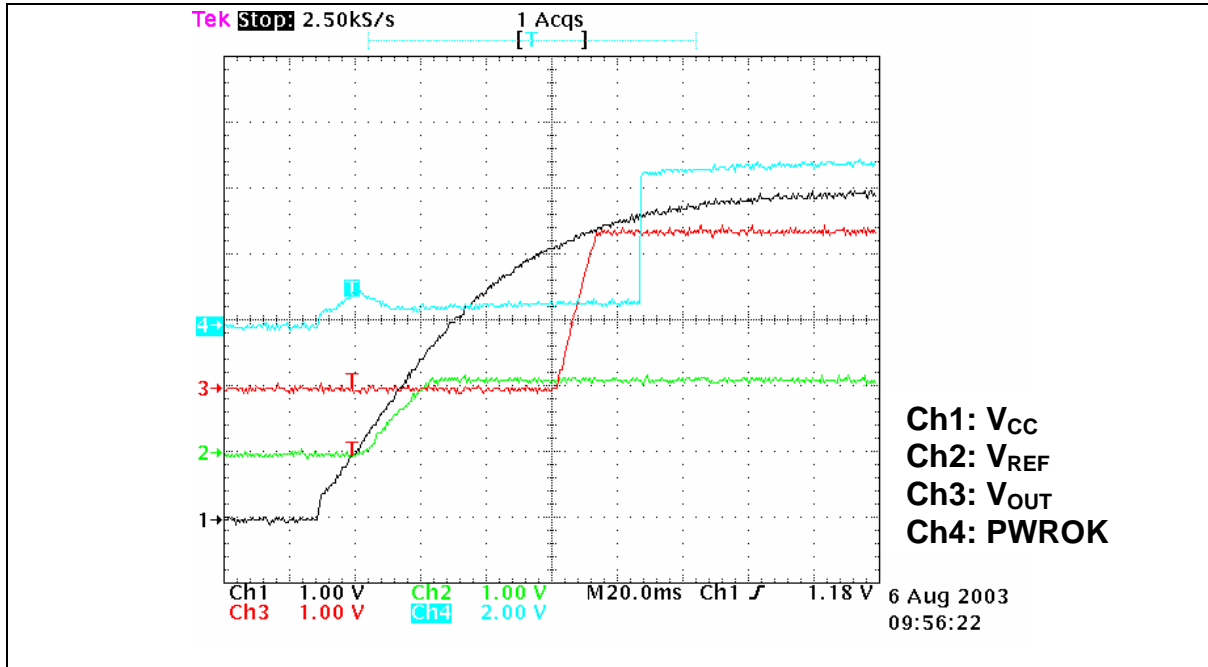
- Power shut down with condition: no loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.
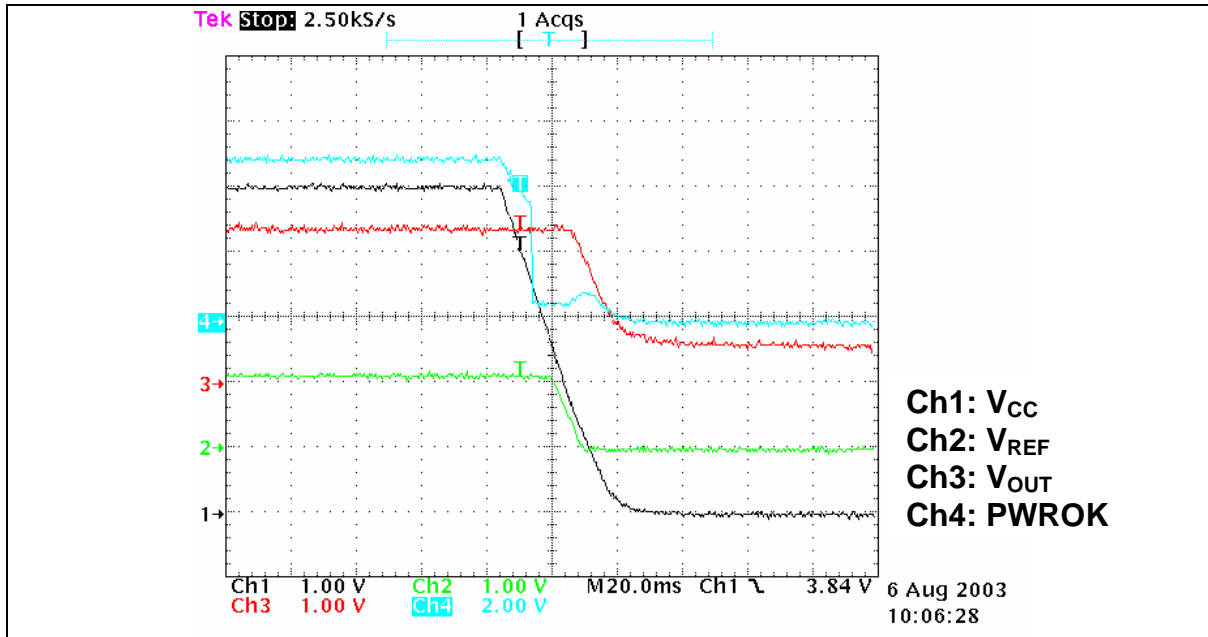
Ch1: V_{CC}
Ch2: V_{REF}
Ch3: V_{OUT}
Ch4: PWROK

- High gate switch off with condition: no loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.

Ch1: UGATE
Ch2: LGATE
Ch3: Phase
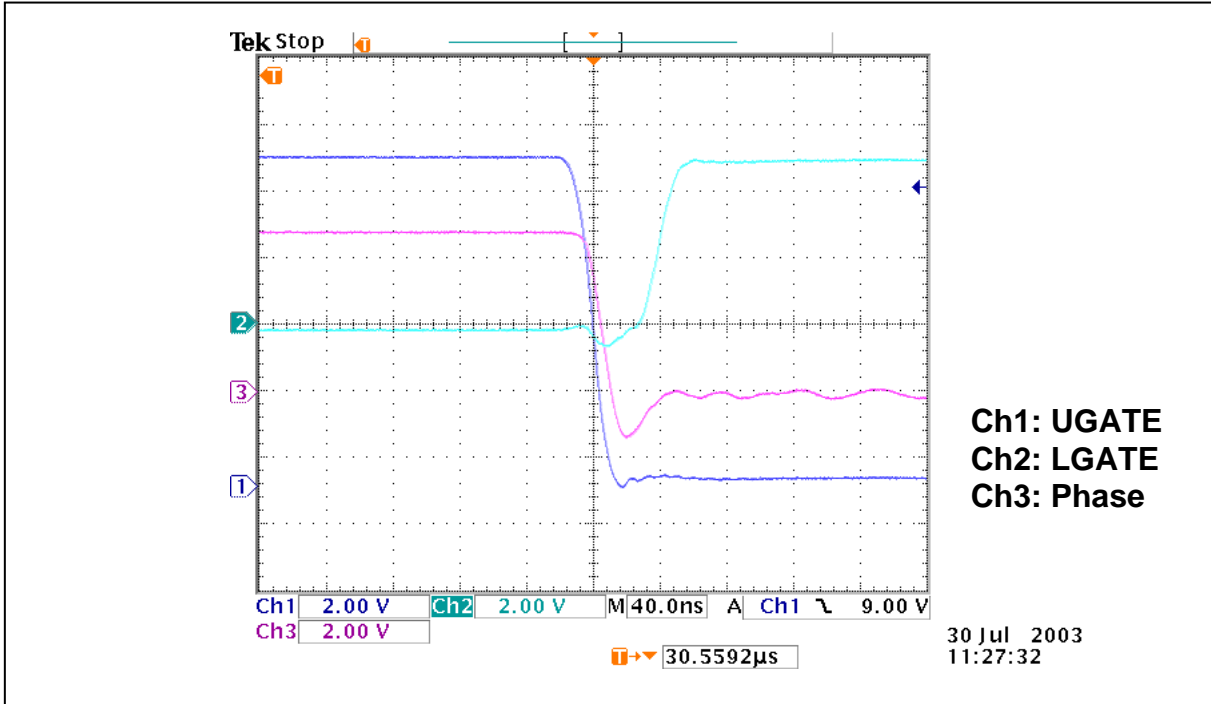
- High gate switch off with condition: 2Amp loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.

Ch1: UGATE
Ch2: LGATE
Ch3: Phase

- High gate switch on with condition: no loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.

Ch1: UGATE
Ch2: LGATE
Ch3: Phase

- High gate switch on with condition: no loading; C_{SS}=0.1uF; VCC=5V; VOUT=2.5V; f = 200 KHz.

Ch1: UGATE
Ch2: LGATE
Ch3: Phase
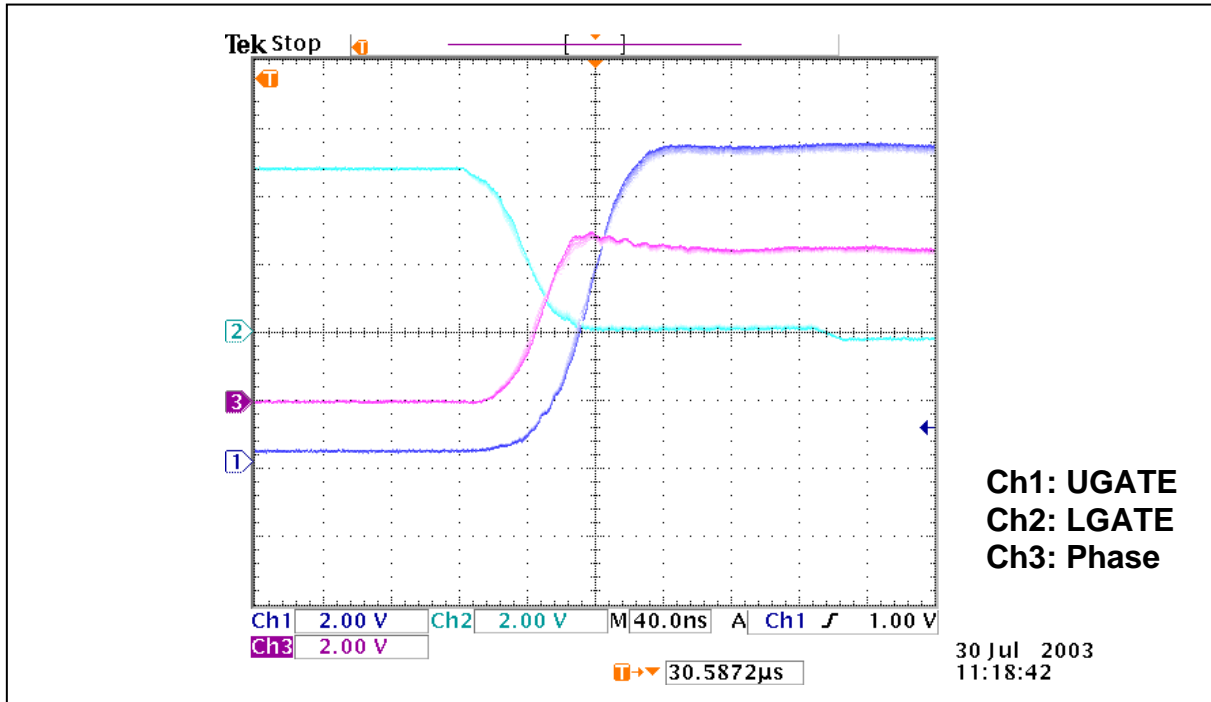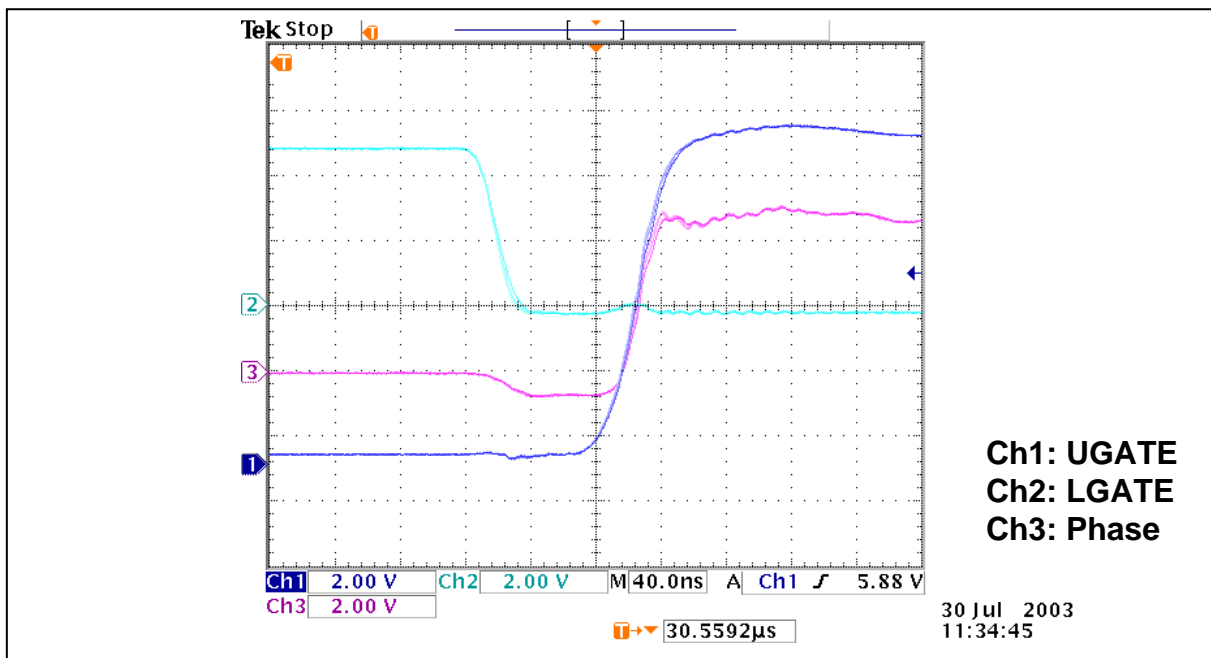
- Load transient response with condition: 0.5Amp to 5.5Amp; C_{SS}=0.1uF; VIN=5V; VOUT=2.5V; f = 200 KHz.

Ch1: I$_{OUT}$
Ch4: V$_{OUT}$
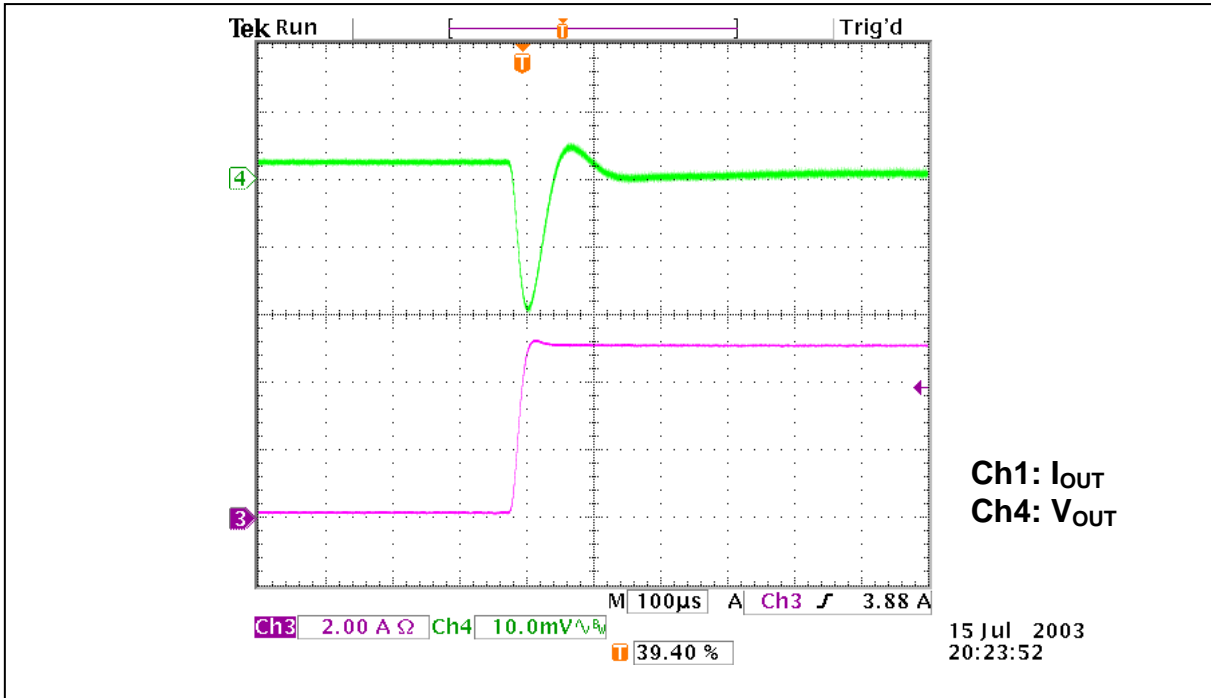
- Load transient response with condition: 5.5Amp to 0.5Amp; C_{SS}=0.1uF; VIN=5V; VOUT=2.5V; f = 200 KHz.

Ch1: V$_{OUT}$
Ch4: I$_{OUT}$

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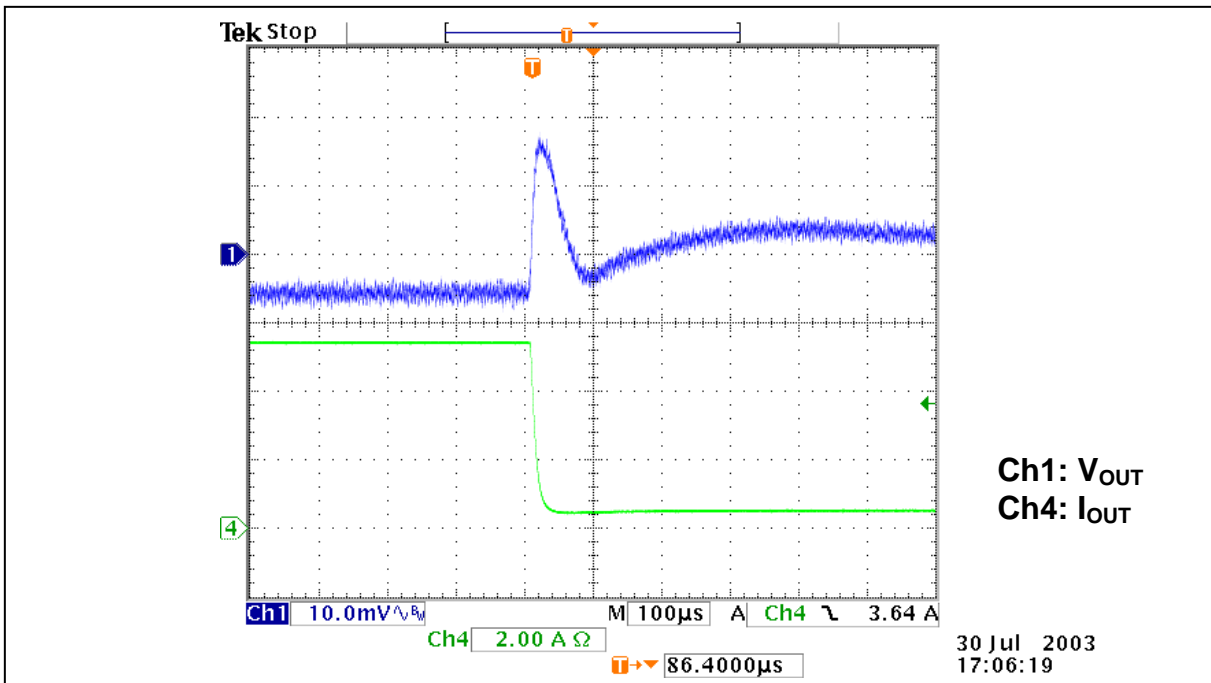
- Output load transient response with condition: IOUT=2Amp; C_{SS}=0.1uF; VIN=5V; VOUT=2.5V; f = 200 KHz.

Ch1: V$_{OUT}$
Ch4: I$_{OUT}$
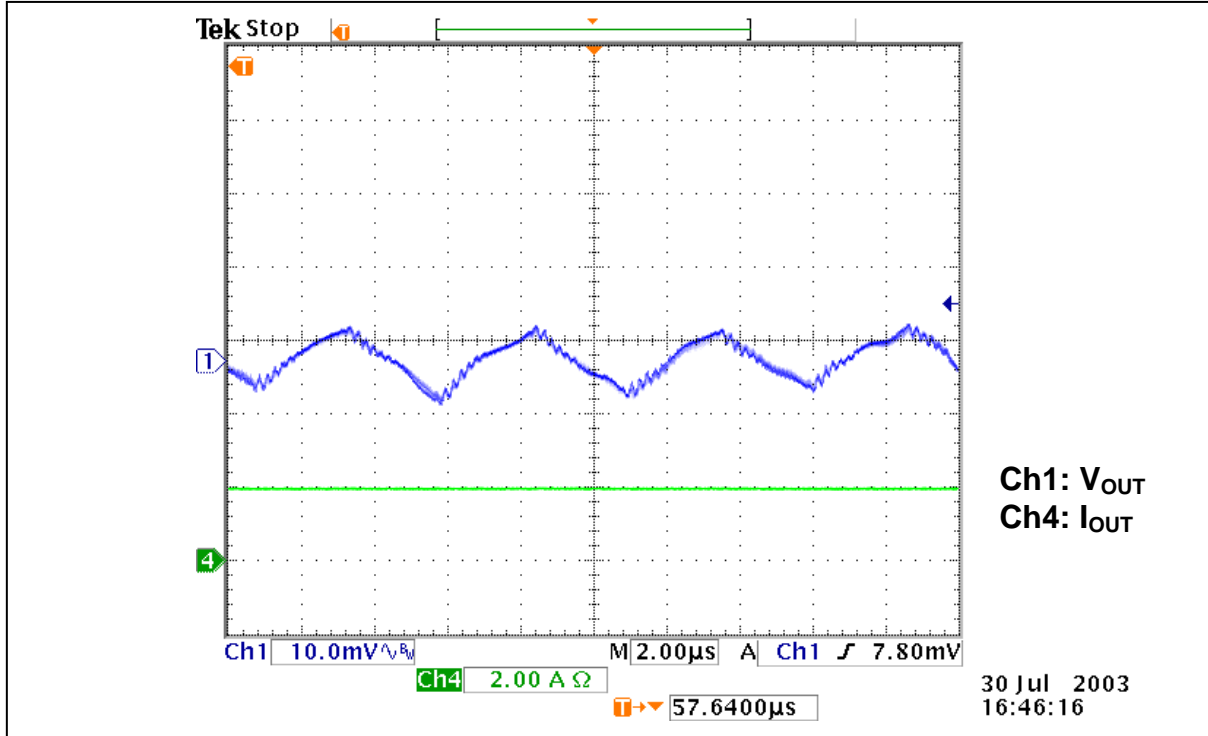
- Regulation efficiency with various loading
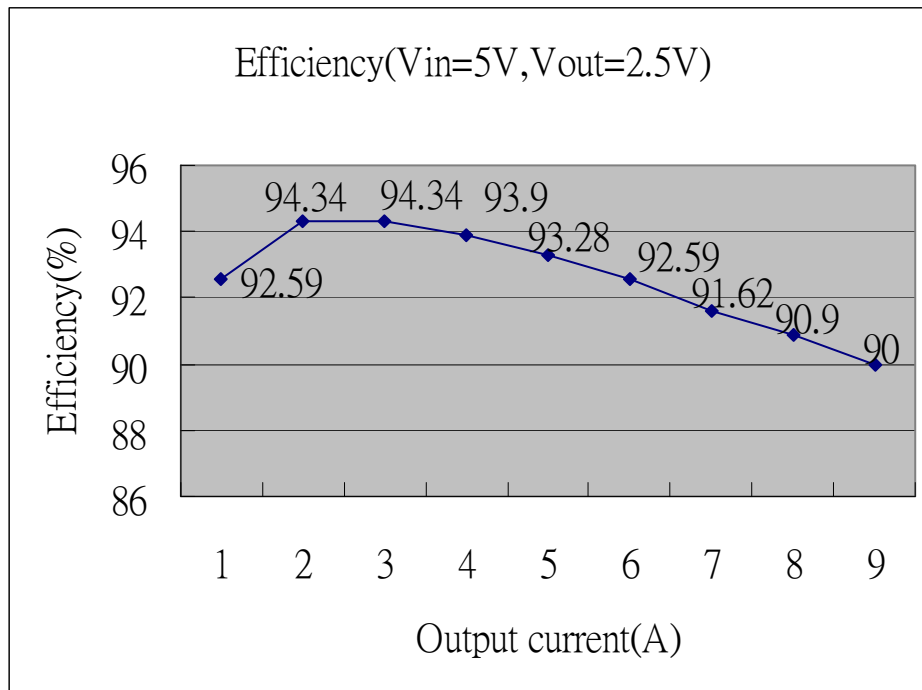
11. PACKAGE DIMENSION OUTLINE

14L SOP (150mil)

Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
H$_E$	5.80	6.20	0.228	0.244
Y	——	0.10	——	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8
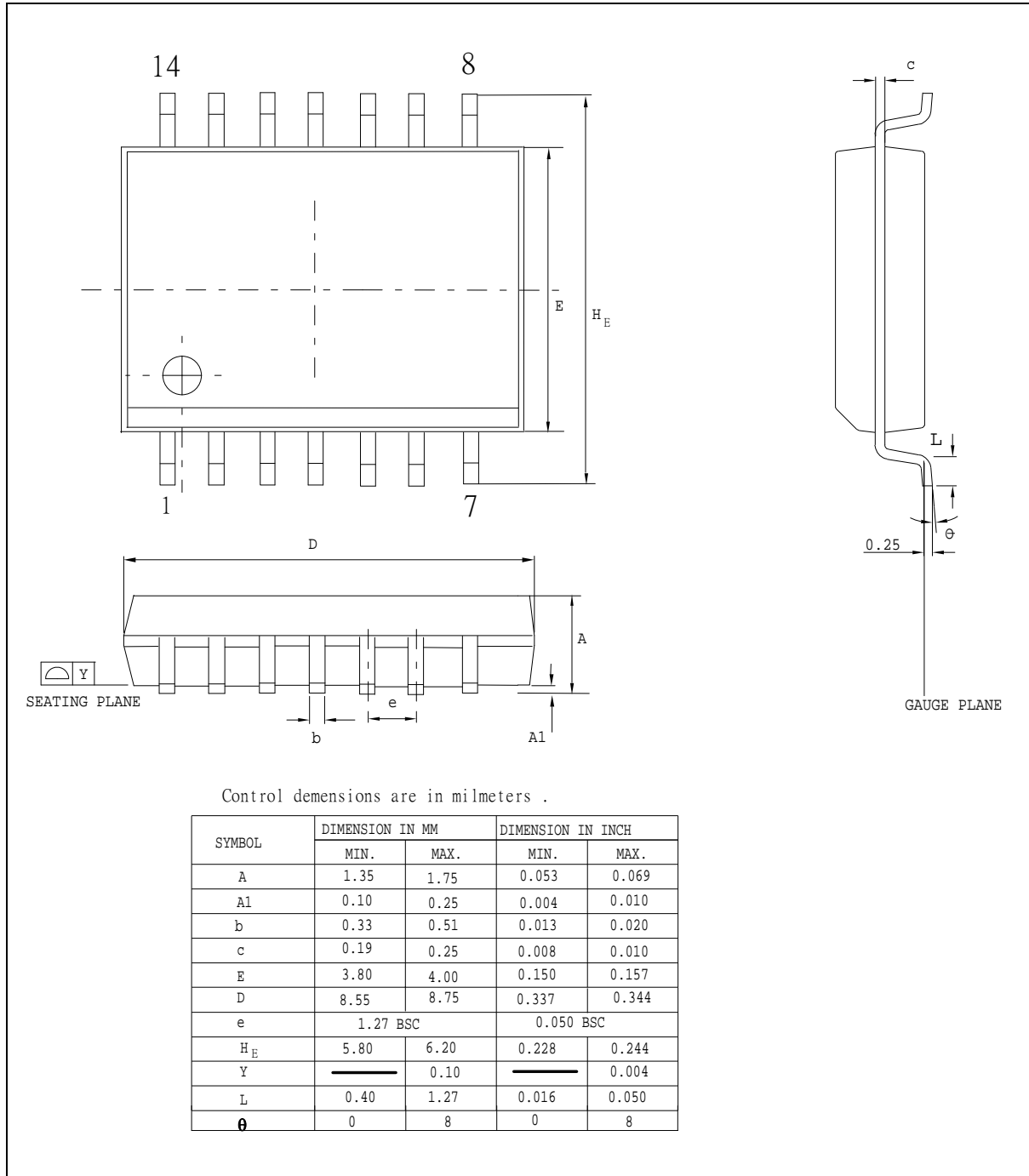
> TAPING SPECIFICATION
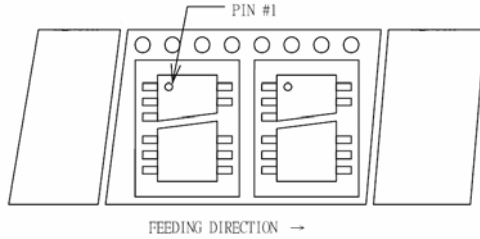
14 Pin SOP Package

12. ORDERING INSTRUCTION

PART NUMBER	PACKAGE TYPE	SUPPLIED AS	PRODUCTION FLOW
W83320G	14PIN SOP (Pb-free package)	E Shape: 56 units/Tube T Shape: 2,500 units/T&R	Commercial, 0℃ to +70℃

13. TOP MARKING SPECIFICATION

W83320G
2322906Z-N
523GA

Left Line: Nuvoton Logo

1st Line: Part No – **W83320G** is for Pb-free package.

2nd Line: IC Tracking Code

3rd Line: Manufacturing Date Code (X XX) + Assembly Code (X) + IC Version (X)

523: packages assembled in Year 05', week 23

G: assembly house ID; G means GR, O means OSE, etc.

A: the IC version (A means A, B means B and C means C…etc.)

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