NUP4304MR6

Low Capacitance Diode Array for ESD Protection in Four Data Lines

NUP4304MR6 is a MicroIntegration™ device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pF Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  - Machine Model = Class C
  - Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground

Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I^2C Bus Protection
- Pb−Free Package is Available

MAXIMUM RATINGS (Each Diode) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	200	mAdc
Peak Forward Surge Current	$I_{FM(surge)}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(AV)}$	715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non−Repetitive Peak Forward Current t = 1.0 μs t = 1.0 ms t = 1.0 S	I_{FSM}	 2.0 1.0 0.5	A

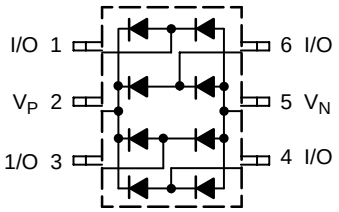
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

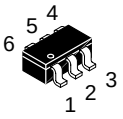
ON Semiconductor®

http://onsemi.com

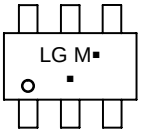
PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



TSOP−6
CASE 318F
PLASTIC



LG = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUP4304MR6T1	TSOP−6	3000/Tape & Reel
NUP4304MR6T1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	260	°C
Junction Temperature	T_J	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Each Diode)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Reverse Breakdown Voltage ($I_{(BR)}$ = 100 μA)		$V_{(BR)}$	70	−	−	Vdc
Reverse Voltage Leakage Current	(V_R = 70 Vdc) (V_R = 25 Vdc, T_J = 150°C) (V_R = 70 Vdc, T_J = 150°C)	I_R	− − −	− − −	2.5 30 50	μAdc
Capacitance (between I/O pins) (V_R = 0 V, f = 1.0 MHz)		C_D	−	0.8	1.5	pF
Capacitance (between I/O pin and ground) (V_R = 0 V, f = 1.0 MHz)		C_D	−	1.6	3	pF
Forward Voltage	(I_F = 1.0 mAdc) (I_F = 10 mAdc) (I_F = 50 mAdc) (I_F = 150 mAdc)	V_F	− − − −	− − − −	715 855 1000 1250	mV_{dc}

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

Curves Applicable to Each Cathode

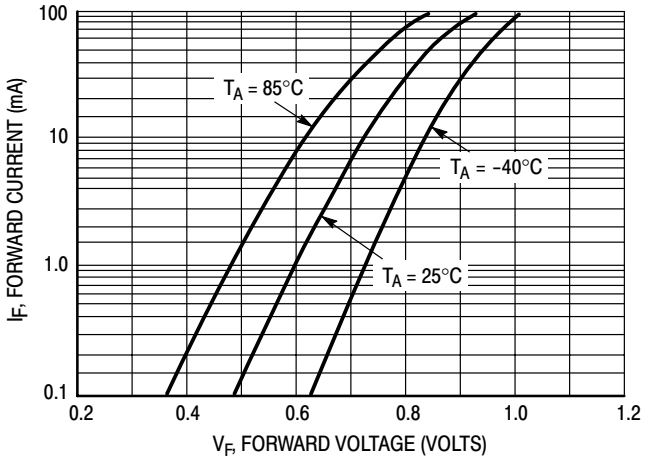


Figure 1. Forward Voltage

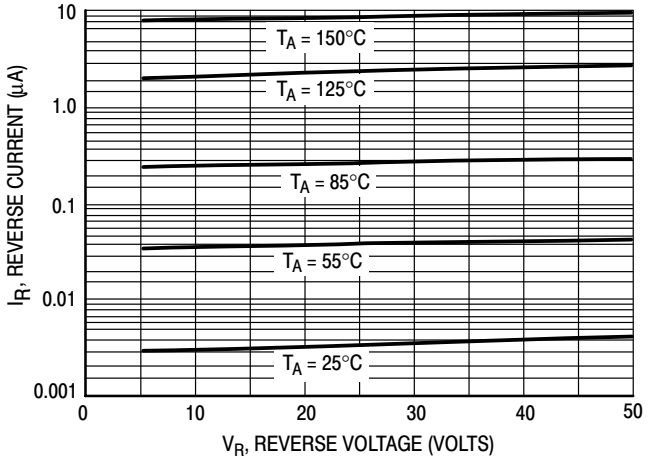


Figure 2. Leakage Current

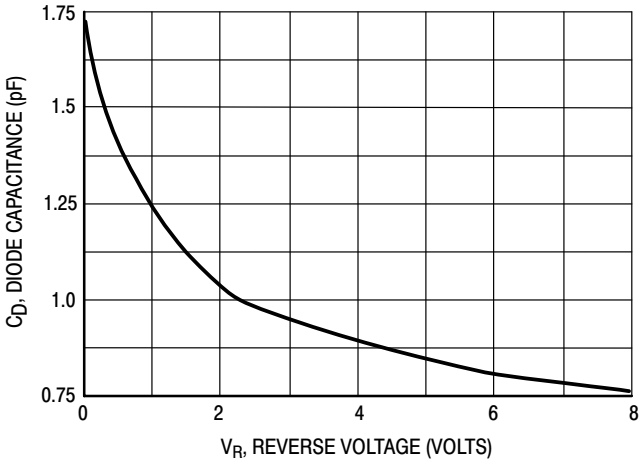


Figure 3. Capacitance

APPLICATIONS INFORMATION

The NUP4304MR6 is a low capacitance diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used on high speed I/O data lines. The integrated design of the NUP4304MR6 offers surge rated, low capacitance steering diodes integrated in a single package (TSOP−6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground.

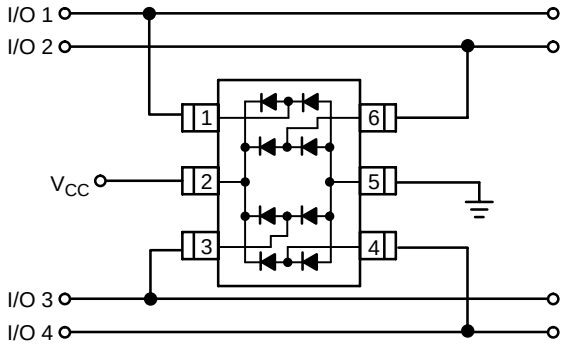
NUP4304MR6 Configuration Options

The NUP4304MR6 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (Vf or Vcc+Vf). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 5. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductance.

Option 1

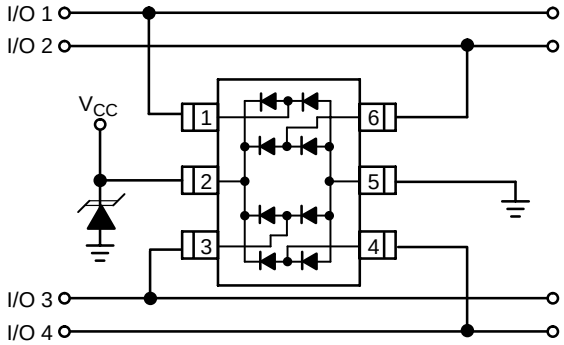
Protection of four data lines using Vcc as reference.



For this configuration, connect pin 2 directly to the positive supply rail (Vcc), the data lines are referenced to the supply voltage. Biasing of the steering diodes reduces their capacitance.

Option 2

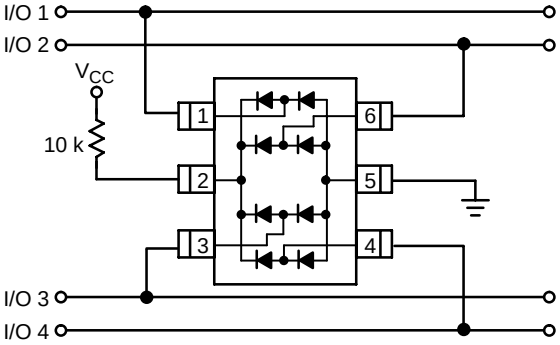
Protection of four data lines and the supply rail using V_{CC} as a reference and an external TVS diode.



If additional protection of the supply rail is desired, an external TVS diode may be added across V_{CC} and ground. This will prevent overvoltage conditions on the supply rail protecting the supply and other circuits connected to it.

Option 3

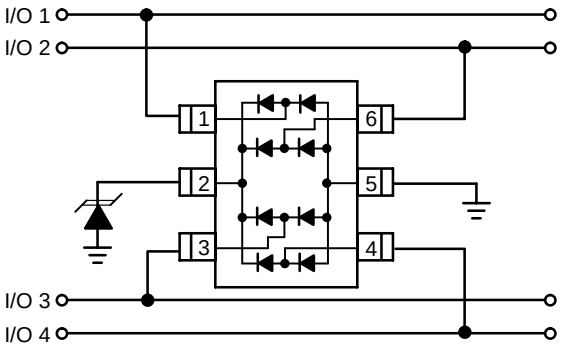
Protection of four data lines with bias and power supply isolation resistor.



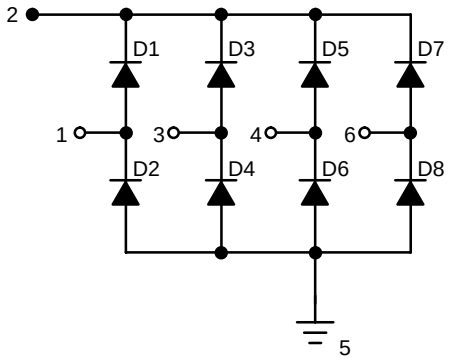
The NUP4304MR6 can be isolated from the power supply by connecting a series resistor between pin 2 and V_{CC}. A 10 kΩ resistor is recommended for this application. This will maintain bias on the internal steering diodes, reducing their capacitance.

Option 4

Protection of four data lines without biasing of the internal steering diodes.



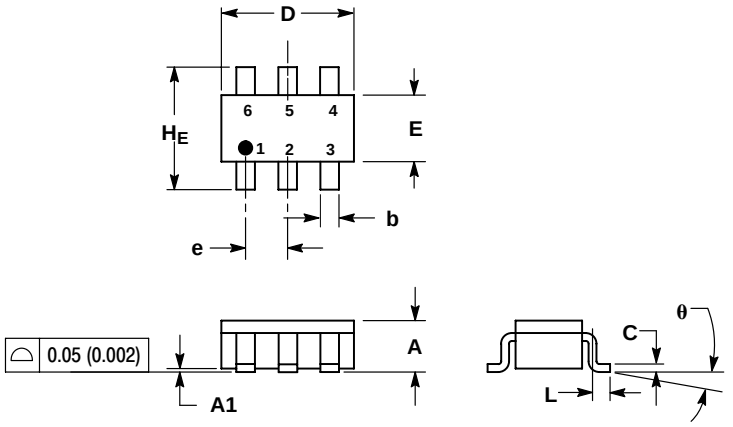
In applications lacking a positive supply reference an external TVS diode may be used as a reference. For these applications, the TVS is connected between pin 2 and the ground plane. The steering diodes will conduct whenever the voltage on the protected line exceeds their forward voltage plus the working voltage of the TVS diode (Vc=Vf + V_{TVS}). In this case, the effective capacitance of the steering diodes will be higher than if a bias was applied.



NUP4304MR6 Equivalent Circuit

PACKAGE DIMENSIONS

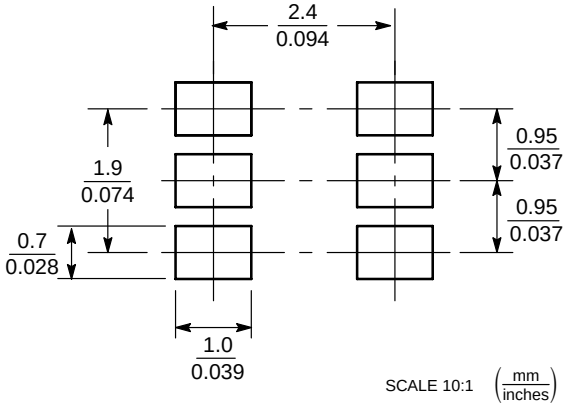
TSOP−6
CASE 318F−05
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03 OBSOLETE. NEW STANDARD 318F−04.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
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Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
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