BLC9G22XS-120AGWT

Power LDMOS transistor

AMPLEON

Rev. 1 — 7 February 2019 **Product data sheet**

1. Product profile

1.1 General description

120 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2200 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit with gull wing device. V_{DS} = 28 V; I_{Dq} = 200 mA (main); $V_{GS(amp)peak}$ = 0.6 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2200	28	15	16.8	45	–34 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

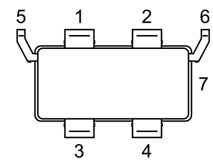
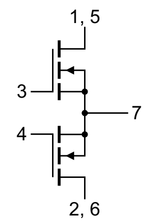
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		 aaa-007731
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G22XS-120AGWT	-	air cavity plastic earless flanged package; 6 leads	SOT1278-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 200 mA (main); $V_{GS(amp)peak}$ = 0.6 V; T_{case} = 80 °C		
		P_L = 15 W	0.55	k/W
		P_L = 19 W	0.54	k/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.4 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 200 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	7.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.0 A	-	2.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	-	340	573	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.72 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 72 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 360 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	13.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.6 A	-	5.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 2.52 A	-	190	323	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.9 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2197.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 200 mA (main); $V_{GS(amp)peak}$ = 1.0 V; T_{case} = 25 °C; unless otherwise specified; with a straight lead device in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 15 W	16.1	17.1	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 15 W	-	–12	–8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 15 W	40	44	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 15 W	-	–28	–24	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.9 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f = 2197.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 200 mA (main); $V_{GS(amp)peak}$ = 1.0 V; T_{case} = 25 °C; unless otherwise specified; with a straight lead device in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 25 W	6.3	6.8	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 25 W	105	120	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G22XS-120AGWT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 1.0 V; f = 2110 MHz; P_L = 44 W (5 dB OBO); 1-carrier W-CDMA; 100 % clipping; PAR = 9.9 dB.

7.2 Impedance information (straight lead)

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 200 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	14.6 – j16.6	5.4 – j7.2	56	61.2	16.8
2140	20.4 – j13.9	5.5 – j7.6	56	61.2	16.9
2170	24.5 – j6.8	5.1 – j7.3	56	60.0	16.7
2230	16.8 + j6.6	5.3 – j7.6	56	60.0	16.8
Maximum drain efficiency load					
2110	14.6 – j16.6	9.9 – j4.5	42	69.9	18.9
2140	20.4 – j13.9	10.4 – j4.2	40	69.8	19.2
2170	24.5 – j6.8	9.2 – j3.0	39	70.0	19.2
2230	16.8 + j6.6	8.4 – j2.5	38	67.9	19.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 420 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	11.0 – j13.8	3.8 – j6.4	100	60.0	16.4
2140	15.1 – j12.3	4.1 – j7.0	100	59.7	16.6
2170	18.5 – j7.8	4.3 – j7.1	100	60.7	16.8
2230	14.4 + j3.0	3.6 – j6.8	100	60.4	16.9
Maximum drain efficiency load					
2110	11.0 – j13.8	5.1 – j3.4	78	69.3	18.5
2140	15.1 – j12.3	4.8 – j3.4	75	69.2	18.7
2170	18.5 – j7.8	4.4 – j3.8	77	69.1	18.7
2230	14.4 + j3.0	3.9 – j4.2	75	68.9	18.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

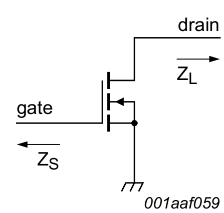


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design (gull wing)

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 200 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	14.6 – j16.6	7.2 – j7.0	53	36.5	20.3
2140	20.4 – j13.9	7.2 – j7.0	53	36.5	20.3
2170	24.5 – j6.8	7.0 – j6.4	52	36.5	20.3
2230	16.8 + j6.6	6.4 – j6.7	54	36.5	20.3

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 15 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 200 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	11.2 – j14.9	14.3 – j6.6	53	52.2	22.6
2140	15.2 – j14.2	14.3 – j6.5	54	52.5	22.9
2170	19.4 – j10.8	14.2 – j6.5	53	52.9	23.0
2230	19.7 + j1.7	14.2 – j6.4	52	52.1	23.1

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 15 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 420 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	8.3 – j12.5	6.4 – j 13.8	87	25.7	19.6
2140	10.9 – j12.2	6.3 – j 13.6	88	25.7	19.7
2170	14.0 – j10.4	6.2 – j 13.4	90	25.8	19.8
2230	15.7 – j 1.7	5.9 – j 13.0	90	26.3	20.1

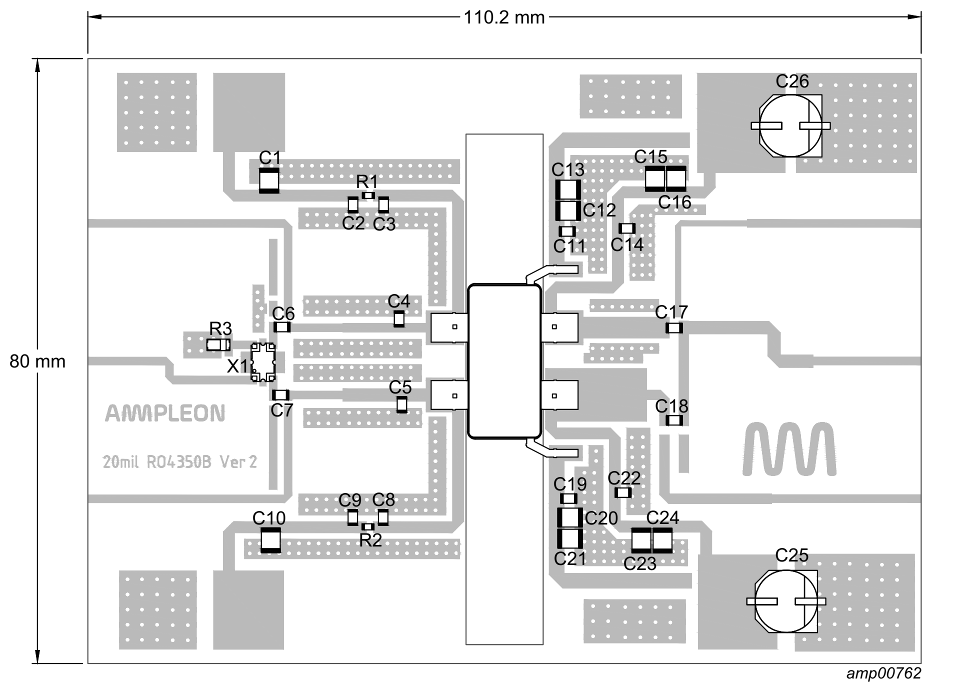
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 15 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
2110	1.4 – j1.5
2140	1.2 – j0.4
2170	1.0 – j0.5
2230	0.8 + j2.0

7.4 Test circuit



Printed-Circuit Board (PCB): RO4350B; thickness = 0.508 mm; thickness copper plating = 35 µm.
See Table 15 for a list of components.

Fig 2. Component layout

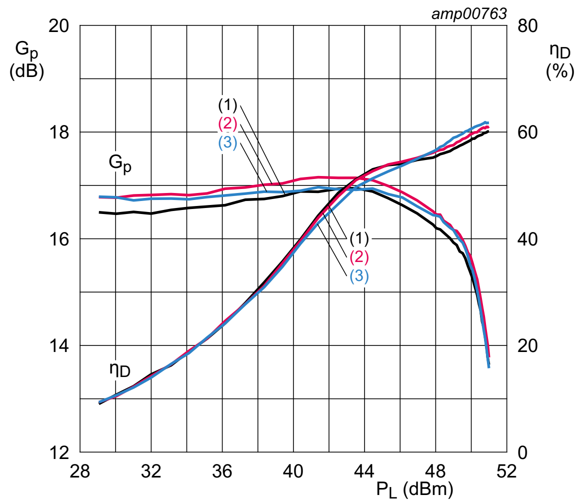
Table 15. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C10, C12, C13, C15, C16, C20, C21, C23, C24	multilayer ceramic chip capacitor	10 µF, 100 V	Murata: GQM2195C2E150FB15, SMD 0805
C2, C9	multilayer ceramic chip capacitor	10 nF, 10 V	Murata: GRM32ER71H106KA12L, SMD 0805
C3, C6, C7, C8, C14, C18, C22	multilayer ceramic chip capacitor	8.2 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C4	multilayer ceramic chip capacitor	2.0 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C5	multilayer ceramic chip capacitor	1.8 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C11, C19	multilayer ceramic chip capacitor	39 pF, 250 V	Murata: GQM2195C2E1R8BB15, SMD 0805
C17	multilayer ceramic chip capacitor	3.0 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C25, C26	electrolytic capacitor	220 µF, 50 V	
R1, R2	resistor	5.1 Ω, 1 %	SMD 805
R3	resistor	50 Ω, 25 W	Anaren: C8A50Z4A
X1	hybrid coupler	2 dB, 90°	Anaren: Xinger III, X3C20F1-02S

7.5 Graphical data (gull wing device)

7.5.1 Pulsed CW and CW (NVA sweep)



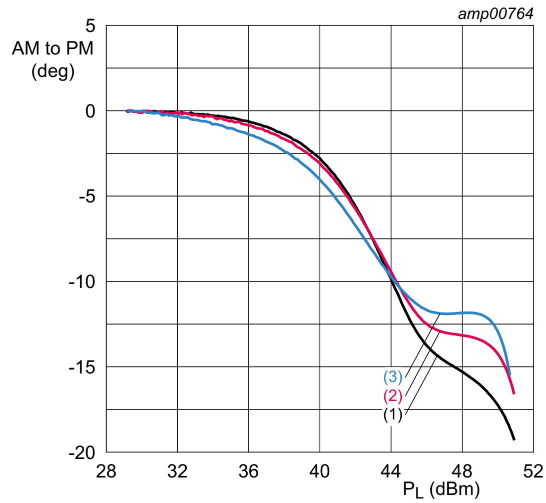
V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

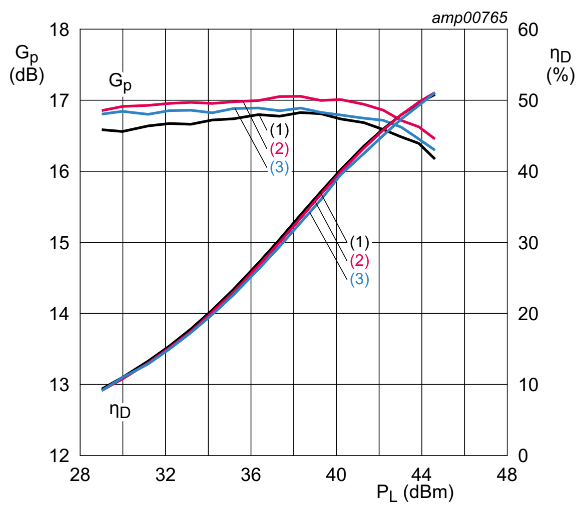
(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 64 DPCH (100 % clipping): PAR = 9.9 dB per carrier at 0.01 % probability on CCDF per carrier.



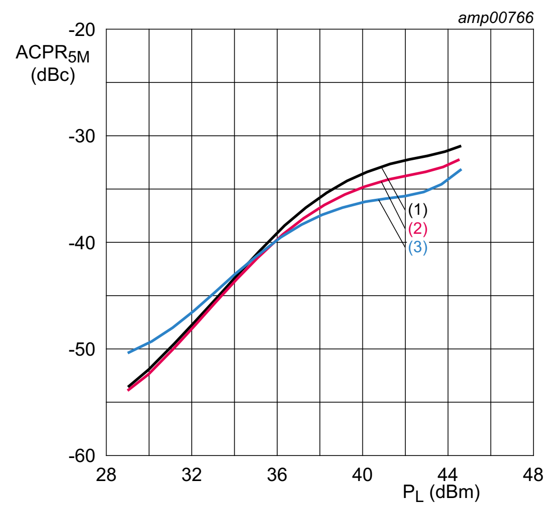
V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



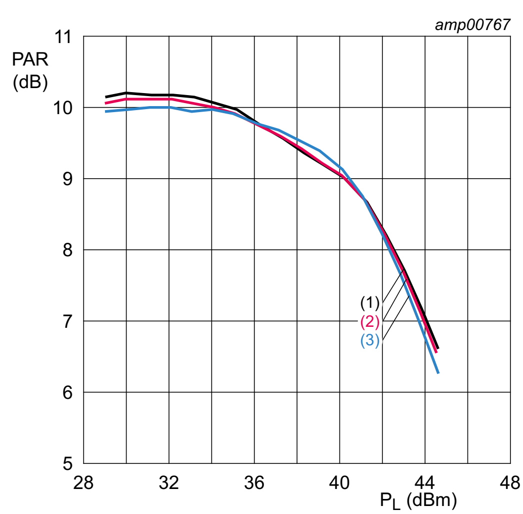
V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

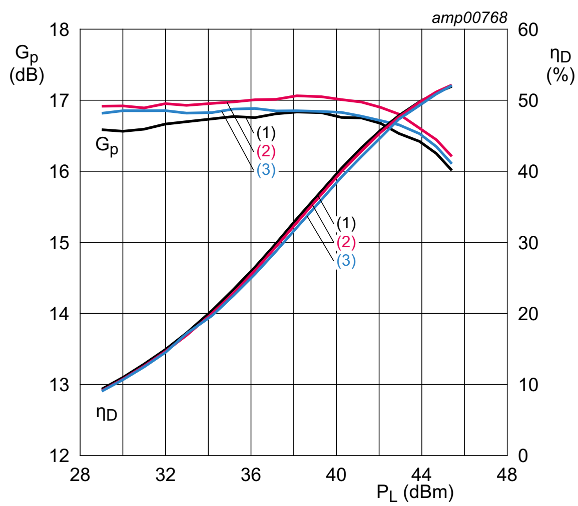
(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.5.3 1-Carrier LTE 20 MHz

1-Carrier LTE 20 MHz; PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



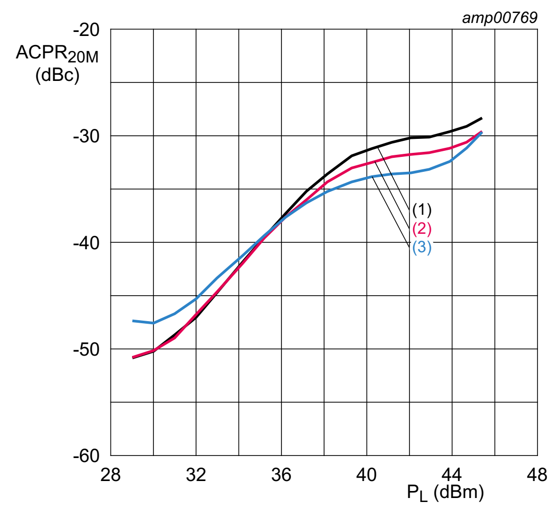
V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 2110 MHz

(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

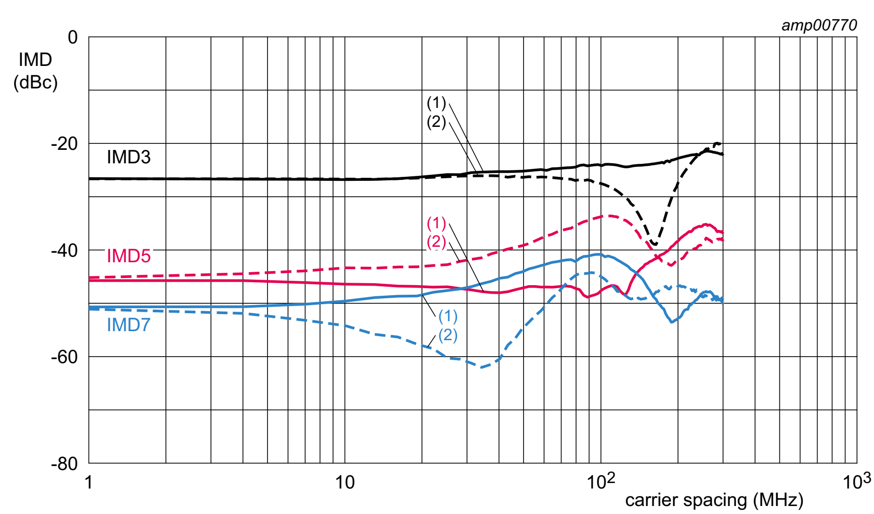
(1) f = 2110 MHz

(2) f = 2155 MHz

(3) f = 2200 MHz

Fig 9. Adjacent channel power ratio (20 MHz) as a function of output power; typical values

7.5.4 2-Tone VBW



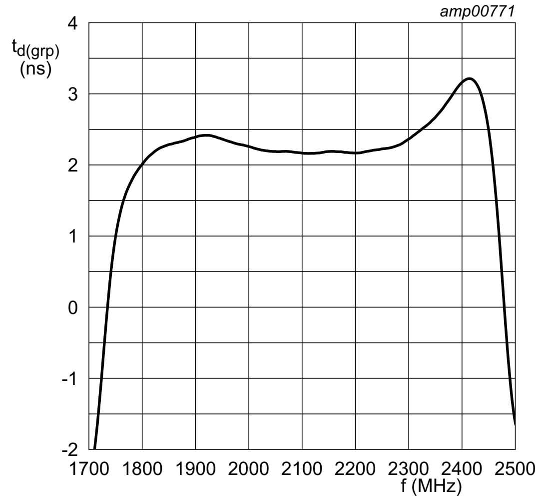
V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V; P_L = 41.8 dBm; f = 2155 MHz.

(1) IMD low

(2) IMD high

Fig 10. VBW capability

7.5.5 Group delay

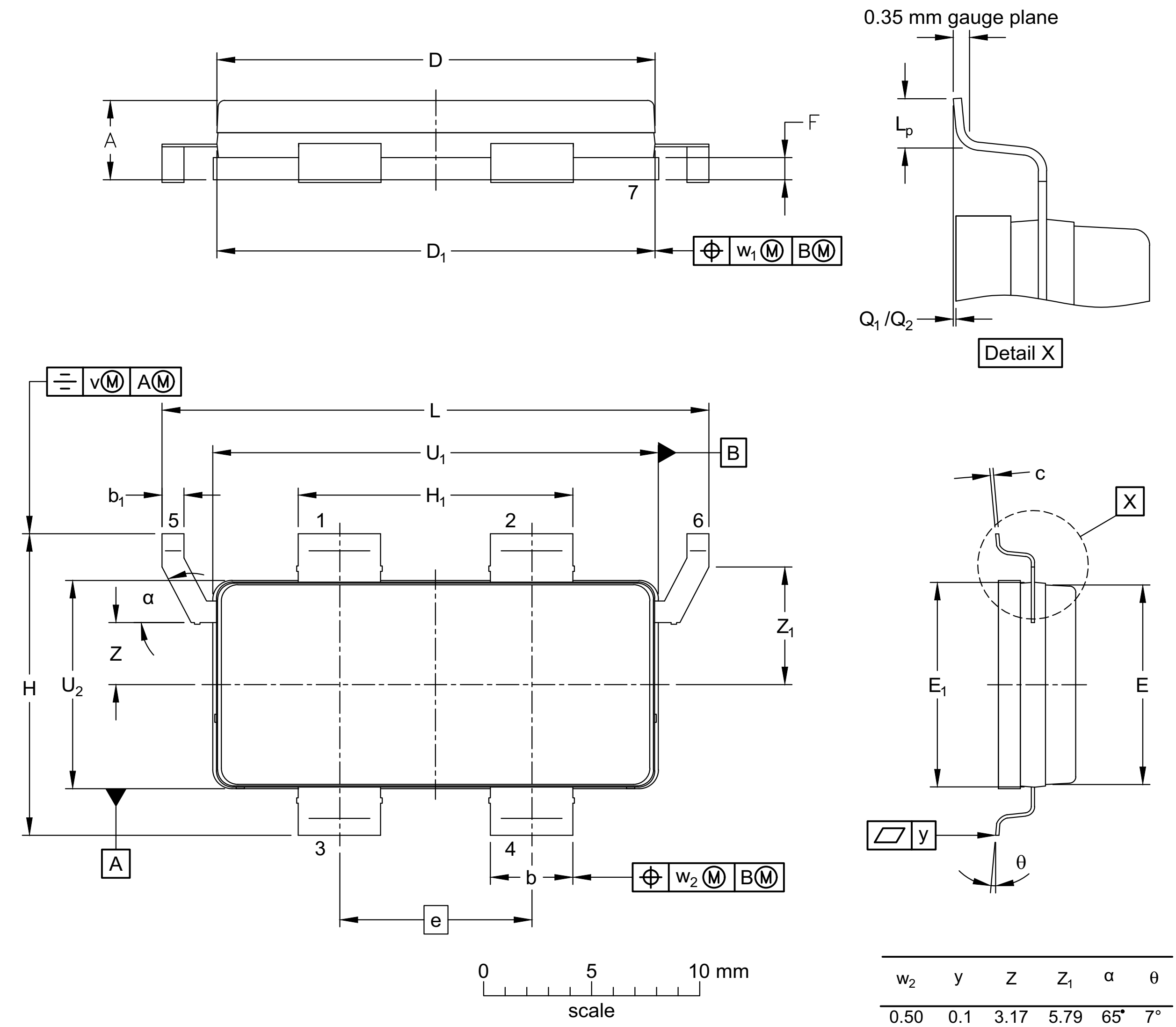


V_{DS} = 28 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = 0.6 V.

Fig 11. Group delay time as a function of frequency; typical values

8. Package outline

Air cavity plastic earless flanged package; 6 leads SOT1278-1



w_2	y	Z	Z_1	α	θ
0.50	0.1	3.17	5.79	65°	7°
		2.67	5.29	61°	0°

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Lp	Q_1(1)	Q_2(2)	U_1	U_2	v	w_1
mm	max	4.01	3.94	1.14	0.18	20.42	20.37	9.80	9.75		1.14	14.50	12.80	25.45	1.10	0.05	0.06	20.70	9.91	0.50	0.50
	nom									8.89											
	min	3.40	3.68	0.89	0.13	20.12	20.17	9.50	9.55		0.94	13.90	12.60	25.15	0.80	-0.05	-0.06	20.50	9.70		

Notes: 1) Q_1 applies to pins 1,2,3 & 4
2) Q_2 applies to pins 5 & 6
3) Ringframe and/or ringframe glue shall not overhang at the side of the flange

sot1278-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1278-1						18-04-17

Fig 12. Package outline SOT1278-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MTF	Median Time to Failure
NVA	Vector Network Analyzer
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G22XS-120AGWT v.1	20190207	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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13. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

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