PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-PTS/14/8446
Dated 07 May 2014

SO8 Package: Assembly site transfer from ST Muar to ST Shenzhen

Table 1. Change Implementation Schedule

Forecasted implementation date for change	30-Jun-2014
Forecasted availability date of samples for customer	30-Apr-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	30-Apr-2014
Estimated date of changed product first shipment	30-Jun-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see list
Type of change	Package assembly location change
Reason for change	Optimization and Service Improvement
Description of the change	Please be informed that products housed in SO8 package from ST Muar will be transferred to ST Shenzhen Assy Plant (conversion to Lead -Free, whenever applicable).
Change Product Identification	Marking code "99" identify Muar Assy plant
Manufacturing Location(s)	1]St Muar - Malaysia

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN APG-PTS/14/8446**
Please sign and return to STMicroelectronics Sales Office	**Dated 07 May 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Liporace, Nicola	Marketing Manager
Pernigotti, Elena Maria	Marketing Manager
Cassani, Fabrizio	Product Manager
Nicoloso, Riccardo	Product Manager
Minerva, Francesco	Q.A. Manager
Pintus, Alberto	Q.A. Manager

SO8 Package: Assembly site transfer from ST Muar to ST Shenzhen

WHAT:

Please be informed that product housed in SO8 package from ST Muar will be transferred to ST Shenzhen assembly Plant (conversion to Lead-Free, whenever applicable).

WHY:

- Our lead frame supplier DCI announced recently his "stamped" lead frame activity closure.
- Taking advantage of the need to immediately activate a second source qualification, we have decided to move the assy process to Shenzhen for production rationalization and service improvement reasons

HOW:

See enclosed the qualification Reports:
-**RR000414CT2235**
-**RR002314CS2039**
-RR002414CS2039

WHEN:

The change will be implemented starting from the end of June 2014. Please be informed that the DCI lead frame stock will allow the production continuity only until the end of 2014, forcing the transfer to Shenzhen early 2015 latest.

See below List of products involved

LINE	PRODUCT
U52003	L9820D
U52003	L9820D013TR
U53703	09352534TR
U53703	E-L9637D
U53703	E-L9637D013TR
U71303	L9613B
U71303	L9613B013TR
UH0103	L4979D
UH0103	L4979D-E
UH0103	L4979D013TR
UH0103	L4979DTR-E
UH2103	L4989D013TR
UH4403	L4993D
UH4403	L4993DTR
UH7103	L4988D
UH7103	L4988DTR
UN4303	L5150CS
UN4303	L5150CSTR

SO8 assembly site transfer from ST Muar to ST Shenzhen

BIPOLAR and $BCD_{OFF/2/3/4/5}$ technologies

Revision history			
Rev.	**Date of Release**	**Author**	**Changes description**
0.1	April 3, 2014	F. Ceraulo - APG Q&R Catania	Creation

Table of contents

Section	Pag	Content
1	3	Reliability evaluations overview
1.1	3	Objectives
1.2	4	Results
2	5	Traceability
3	6	Reliability qualification plan and results – Summary table

- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on several products chosen as test vehicles to qualify the SO8 assembly site transfer from ST Muar (Malaysia) to ST Shenzhen (China).

Here below the test vehicles matrix with the raw material details:

	ST silicon line					
Raw material	**W023**	**U356**	**U520**	**UC24**	**UH01**	**UN43**
FE Technology	BIP	BCD Offline	BCD2	BCD3	BCD4	BCD5
FE Diffusion Fab	AMK6					
Die size (mm2)	4.23	4.18	4.08	3.91	3.42	2.82
Die finishing front	SiN	SiN	SiN	SiN	USG-PSG-SiON-PIX	USG-PSG-SiON-PIX
Die finishing back	CrNi	Lapped silicon	CrNi	Raw Si	Raw Si	CrNIAu
L/F description	FRAME SO 8L 94x125					
Au wire diameter (mils)	1	1	1.3	1	1	1
Molding compound	SUMITOMO EME-G700KC					
Die attach	Glue ABLEBOND					

The qualification was done according to **AEC_Q100 Rev.G** specification applying a family approach due to specific similarity among the different test vehicles. In the below table the applied stress test as well as a comparison between the AEC-Q100 and ZVEI requirements is reported:

		Test Group A					Test Group B		Test Group C				Test Group D				
		THB	AC	TC	PTC	HTSL	HTOL	ELFR	WBS	WBP	SD	PD	HBM	CDM	LU	ED	GL
AEC-Q100		x	x	x	x		x	x	x	x	x	x				x	x
ZVEI		x	x	x	x		x	x	x	x	x	x				x	x
Commercial product	Silicon Line																
L4949	W023	x	x	x	NA	x	x	x	x	x	x	x	x	x	x	x	x
	U356	x	x	x	NA	x	x	x	x	x	x	x		x		x	
L9820D	U520		x	x	NA	x		x	x	x	x	x	x	x	x		
	UC24		x	x		x		x	x	x	x	x					
L4979D	UH01	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
L5150CJ	UN43		x	x		x		x	x	x	x	x	x	x	x		

In this report the results of the product identified in yellow in the above table are reported, per each of them see stress test details in section 3 of this report.

1.2 Results

All reliability tests have been completed with positive results neither functional nor parametric rejects were detected at final electrical testing.

The Wire Bond Pull/Shear tests (WBP, WBS) as Package Assembly Integrity (test Group C) pointed out neither abnormal break loads nor forbidden failure modes both before and after stress test.

Based on the overall positive results we consider the products qualified from a reliability point of view.

- 2. Traceability

Wafer fab information				
	L4949 W023	**L9820D U520**	**L4979D UH01**	**L5150CJ UN43**
Wafer fab manufacturing location	ST AMK6 Ang Mo Kio (Singapore)			
Wafer diameter (inches)	6			
Silicon process technology	BIP	BCD2	BCD4	BCD5
Die finishing back side	CrNi	CrNi	Raw Si	CrNIAu
Die size (mm2)	4.23	4.08	3.42	2.82
Metal levels / materials	2 layer / AlSi 1.2µm last level	2 layer/AlSi 3µm last level	2 layer/AlSiCu 1.1µm last level	3 layer / AlSiCu 3µm last level
Die finishing front side	SiN	SiN	USG-PSG-SiON-PIX	USG-PSG-SiON-PIX
Diffusion Lots #	1: 6222KTF 2: 62302LE 3: 62302LF	62348YE	6232T37	62149N2

Assembly Information				
	L4949 W023	**L9820D U520**	**L4979D UH01**	**L5150CJ UN43**
Assembly plant location	ST Shenzhen (China)			
Package description	SO8			
Molding compound	SUMITOMO EME-G700KC			
Wires bonding material/diameter	Au 1mils	Au 1.3mils	Au 1mils	Au 1mils
Die attach material	Glue ABLEBOND			
Assembly Lots #	1: 993050PU01(NN), 993050PURR(HH), 993050PURQ(LL), 2: 993050Q001(NN), 993050Q0RR(HH), 993050Q0RQ(LL), 3: 993050PW01(NN), 993050PWRR(HH), 993050PWRQ(LL), NOTE: the L4949 was chosen as main test vehicle having max die size representing the worst case. The reliability evaluation on this product was done by using lots with different assembly configurations both in terms of Bonding Force and Ultra-Sonic Power: 3 lots nominal (NN), 6 lots worst cases (HH: Highest Bonding Force and Highest US Power, LL: Lower Bonding Force and Lower US Power)	993180LY01 993180LX01 993180M001	993190DG01 993190DH01 993190DI01	993340DM01

Reliability Information	
Reliability test execution location	ST Catania (Italy)

- 3. Reliability qualification plan and results

Test group A: Accelerated Environment Stress					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
A1	**PC** Pre Cond	- Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40°C/+60°C - Reflow according to level 3 Jedec JSTD020D-1 - 100 Temperature Cycling Ta=-50°C/+150°C	Before THB, AC, TC, HTOL		
A2	**THB** Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 1000 hours	77/4	0/77/4	3 lots x W023 1 lot x UH01
A3	**AC** Autoclave	**ENV. SEQ.** Enviromental Sequence **TC** (Ta=-65°C / +150°C for 100 cycles) + **AC** (Ta=121°C, Pa=2atm for 96 hours)	77/16	0/77/16	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
A4	**TC** Temp. Cycling	Ta=-65°C / +150°C for 500 cycles	77/16	0/77/16	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
A5	**PTC** Power Temp. Cycling	Ta=-40°C / +125°C for 1000 cycles.	45/1	0/45/1	1 lot x UH01
A6	**HTSL** High Temp. Storage Life	Ta=150°C for 1000 hours.	45/16	0/45/16	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43

Test group B: Accelerated Lifetime Simulation					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
B1	**HTOL** High Temp. Op. Life	Bias Dynamic stress (JESD22-A108): Ta=125°C, Vcc=28V for 1000 hours	77/4	0/77/4	3 lots x W023 1 lot x UH01
B2	**ELFR** Early Life Failure Rate	Parts submitted to **HTOL** per JESD22-A108 requirements; GRADE 1: 24 hours at 150°C		Passed	Family data
B3	**EDR** Endurance Data Retention	Only for memory devices	-	-	Not Applicable

Test group C: Package Assembly Integrity					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
C1	**WBS** Wire Bond Shear	Per AEC-Q100-001	30 bonds /minimum 5 units/1 lot	All measurement within spec limits	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
C2	**WBP** Wire Bond Pull	Per MIL-STD883, M2011 Condition C or D	30 bonds /minimum 5 units/1 lot	All measurement within spec limits	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
C3	**SD** Solderability		15/16	All measurement within spec limits	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
C4	**PD** Physical Dimensions		10/16	All measurement within spec limits	9 lots x W023 3 lot x U520 3 lots x UH01 1 lot x UN43
C5	**SBS** Solder Ball Shear	Only for BGA package	-	-	Not Applicable
C6	**LI** Lead Integrity	Not required for Surface Mount Devices	-	-	Not Applicable

Test group D: Die Fabrication Reliability					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
D1	**EM** Electromigration				Not Applicable
D2	**TDDB** Time Dependent Dielectric Breakdown				Not Applicable
D3	**HCI** Hot Carrier Injection				Not Applicable
D4	**NBTI** Negative Bias Temperature Instability				Not Applicable
D5	**SM** Stress Migration				Not Applicable

Test group E: Electrical Verification

AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
E2	**ESD** HBM	HBM=[R=1.5kΩ, C=150pF]	1 lot	±2.0kV	1 lot x W023 1 lot x U520 1 lot x UH01 1 lot x UN43
E3	**ESD** CDM		1 lot	±500V ±750V (*Corner pins)*	1 lot x W023 1 lot x U520 1 lot x UH01 1 lot x UN43
E4	**LU** Latch-Up	Injection current : ±100mA Over voltage: 1.5 x Vop max	6/1	Inj-L/Inj-H@125°C: ±100mA all pins Inj+L/Inj+H@125°C: ±100mA all pins OV: passed	1 lot x W023 1 lot x U520 1 lot x UH01 1 lot x UN43
E5	**ED** Electrical Distributions		30/2	Done	1 lot x W023 1 lot x UH01
E7	**CHAR** Characterization			-	Not Applicable
E8	**GL** Gate Leakage		6/1	PASSED	1 lot x W023
E9	**EMC** Electromagnetic Compatibility		-	-	Not Applicable
E10	**SC** Short Circuit Characterization	According to **AEC-Q100-012**	-	Not Applicable	

Test group F: Defects Screening Tests

AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
F1	**PAT** Process Average Testing		Not performed on qualification lots listed on traceability section of this report. To be implemented starting from first production lot		
F2	**SBA** Statistical Bin/Yield Analysis				

Test group G: Cavity Package Integrity Tests					
AEC #	**Test Name**	**STM Test Conditions**	**Sample Size/ Lots**	**Results Fails/SS/Lots**	**Comments**
G1	**MS** Mechanical Shock	Not applicable: not for plastic packaged devices			
G2	**VFV** Variable Frequency Vibration				
G3	**CA** Constant Acceleration				
G4	**GFL** Gross/Fine Leak				
G5	**DROP** Package Drop				
G6	**LT** Lid Torque				
G7	**DS** Die Shear				
G8	**IWV** Internal Water Vapor				

APG

Reliability Report
U356ba6 - L9856
SO8 transfer to Shenzhen

General Information	
Product line / version	*U356 / ba*
Commercial name	*L9856*
Product description	*High voltage high-side driver*
Product group / division	*APG / Powertrain & Safety*
Package	*SO 08 Strip single island4+3+1*
Silicon process technology	*BCD OFFLINE*

Locations	
Wafer fab	*Ang Mo Kio 6"*
Assembly plant	*ST Shenzhen*
Reliability assessment	*Passed*

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW 3
- 1.1 OBJECTIVES 3
- 1.2 EXTRACT FROM AEC-Q100 PROCESS CHANGE QUALIFICATION GUIDELINES. 4
- 1.3 CONCLUSION 4

2 DEVICE CHARACTERISTICS 5
- 2.1 DEVICE DESCRIPTION 5
- 2.2 PINOUT 5
- 2.3 PIN DESCRIPTION 5
- 2.4 PACKAGE OUTLINE DESCRIPTION 6
- 2.5 BONDING DIAGRAM 8
- 2.6 TRACEABILITY 9

3 RELIABILITY TEST RESULTS 10
- 3.1 RELIABILITY TEST PLAN AND RESULT SUMMARY 10
- 3.2 TEST RESULT SUMMARY BASING ON AEC-Q100 QUALIFICATION TEST PLAN TEMPLATE 11
- 3.3 TEST DESCRIPTION 15

4 ATTACHMENTS 16
- 4.1 HTOL SCHEMATIC 16
- 4.2 HTOL PATTERN 17
- 4.3 HTOL WAVEFORMS OVERVIEW 18
- 4.4 THB / HTRB SCHEMATIC 19

5 TEST GLOSSARY 20

6 REVISION HISTORY 20

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on *U356ba6 (L9856) assembled in SO8 Shenzhen.*

U356 is one of TV.s used to qualify the S08 transfer to *Shenzhen.*
Here below the devices in the same package on which qualification has been done.

DEVICE	U356	UC24	U520
RL	SMKU*U356BA6	SMKU*UC24AA6	SMKU*U520CB6
FE Process	BCD Offline	BCD3	BCD2
FE Fab	AMK6	AMK6	AMK6
BPO	90*90	90*90	127*127
Die area	2200*1900	1680*2330	2270*1800
Front/back side metal	SiN (nitride) / Lapped silicon	SiN (nitride) / Raw Si	SiN (nitride) / CrNi
L/F descr	FRAME SO 8L 94x125	FRAME SO 8L 94x125	FRAME SO 8L 94x125
Frame option	C	C	D
Au wire	1.0mil 3N	1.0mil 3N	1.3mil 4N
Resin	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC
Glue	ABLEBOND	ABLEBOND	ABLEBOND
Down bonding	No	No	Wire on BTWG

DEVICE	UN43	UH01	W023
RL	SMKU*UN43BA6	SMKU*UH01BB6	SMKU*W023FB6
FE Process	BCD5	BCD4	BIP
FE Fab	AMK6	AMK6	AMK6
BPO		90*90	101*101
Die area	1530*1840	1700*2010	2160*1960
Front/back side metal		USG-PSG-SiON-PIX / Raw Si	SiN (nitride) / CrNi
L/F descr	FRAME SO 8L 94x125	FRAME SO 8L 94x125	FRAME SO 8L 94x125
Frame option	C	C	C
Au wire	1.0mil 3N	1.0mil 3N	1.0mil 4N
Resin	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC
Glue	ABLEBOND	ABLEBOND	ABLEBOND
Down bonding		No	No

U356 - L9856 is a driver for common-rail magnetic valve application.
For the reliability evaluation, the following tests have been carried out:

- PC (JL3) + 100cy TC + HTOL
- HTRB
- PC (JL3) + 100cy TC + THB
- PC (JL3) + 100cy TC + TC
- PC (JL3) + 100cy TC + AC
- HTSL
- ESD - CDM
- WBP and WBS.

1.2 Extract from AEC-Q100 process change qualification guidelines

A2	Temperature Humidity Bias or HAST	C4	Physical Dimensions	E5	Electrical Distribution
A3	Autoclave or Unbiased HAST	C5	Solder Ball Shear	E7	Characterization
A4	Temperature Cycling	C6	Lead Integrity	E8	Gate Leakage
A5	Power Temperature Cycling	D1	Electromigration	E9	Electromagnetic Compatibility
A6	High Temperature Storage Life	D2	Time Dependent Dielectric Breakdown	E10	Short Circuit Characterization
B1	High Temperature Operating Life	D3	Hot Carrier Injection	E11	Soft Error Rate
B2	Early Life Failure Rate	D4	Negative Bias Temperature Instability	G1-4	Mechanical Series
B3	NVM Endurance, Data Retention	D5	Stress Migration	G5	Package Drop
C1	Wire Bond Shear	E2	Human Body / Machine Model ESD	G6	Lid Torque
C2	Wire Bond Pull	E3	Charged Device Model ESD	G7	Die Shear
C3	Solderability	E4	Latch-up	G8	Internal Water Vapor

Note: A letter or "●" indicates that performance of that stress test should be **considered** for the appropriate process change

Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E8	E9	E10	E11	G1-G4	G5	G6	G7	G8
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	EM	TDDB	HCI	NBTI	SM	HBM / MM	CDM	LU	ED	CHAR	GL	EMC	SC	SER	MECH	DROP	LT	DS	IWV
ASSEMBLY																																	
Die Overcoat / Underfill	●	●	●	M	●	●																			S			●					H
Leadframe Plating	●	●	●	M	●					C	●			●																		H	
Bump Material / Metal System	●	●	●	M	●	●						●	●															●					
Leadframe Material		●	●	M	●					●	●	●		●													●		H			H	
Leadframe Dimension		●	●	M							●	●		●													●		H				
Wire Bonding		●	●	Q	●				●	●													M				●		H				
Die Scribe/Separate	●	●	●	M																													
Die Preparation / Clean	●	●		M		●			●	●																						H	
Package Marking											B																						
Die Attach	●	●	●	M		●																	●				●		H			H	H
Molding Compound	●	●	●	M	●	●	●				●	●		●											S			●					
Molding Process	●	●	●	M	●	●					●	●		●											S								
Hermetic Sealing		H	H		H							H		H															H		H		H
New Package	●	●	●	M	●	●	●		●	●	●	●	T	●						●	●		●		S		●		H			H	H
Substrate / Interposer	●	●	●	M	●	●			●	●			T												S				H			H	H
Assembly Site Transfer	●	●	●	M		●	●		●	●	●	●	T	●									●		S				H			H	H

A	Only for peripheral routing	G	Only from non-100% burned-in parts	N	Passivation and gate oxide
B	For symbol rework, new cure time, temp	H	Hermetic only	P	Passivation and interlevel dielectric
C	If bond to leadfinger	J	EPROM or E^2PROM	Q	Wire diameter decrease
D	Design rule change	K	Passivation only	S	For plastic SMD only
E	Thickness only	M	For devices requiring PTC	T	For Solder Ball SMD only
F	MEMS element only				

Note1

In red the changes respect to previous.

Note2

PTC, SC	not applicable (pre-driver device, doesn't drive directly inductor, P_d<1W).
SBS	not applicable (required for BGA only).
SER, MECH, DS, IWV	not applicable (required for hermetic package only).
LI	not applicable (required for through-hole package only).
GL	not done, not mandatory.

Note3

WBS, SD, PD	data from assy report.
ELFR	data from burnin.

1.3 Conclusion

The reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing; no significant parameter drift has been found after HTOL and HTRB tests. WBP done after TC and HTSL is positive.
On the basis of the overall positive results, *U356ba6 in SO8 (Shenzhen)* can be qualified from a reliability point of view.

2 DEVICE CHARACTERISTICS

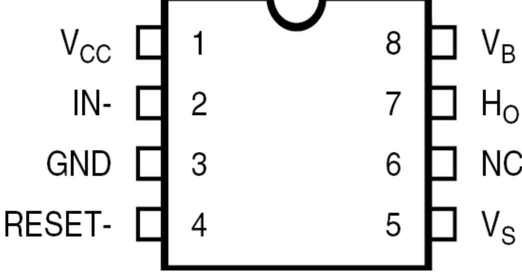
2.1 Device description

L9856 is an high voltage device, manufactured in BCD "OFFLINE" technology.
It has the capability of driving N-channel power MOS transistors. The upper (floating) section is enabled to work with voltage rail up to 160V. The logic inputs are CMOS/TTL compatible.

Features

High voltage rail up to 160V
dV/dt immunity ±50V/nsec in full temperature range
Driver current capability:
 500mA source,
 500mA sink
Switching times 100ns rise/fall with 2.5nF load
CMOS/TTL Schmitt trigger inputs with hysteresis
Under voltage lock out
Clamping on V_{cc}
Loading circuit for external bootstrap capacitor
Inverting input
Reset circuitry

2.2 Pinout



2.3 Pin description

PIN#	NAME	DESCRIPTION	I/O
1	Vcc	Driver Supply, typically 5V	POWER
2	IN-	Driver Control Signal Input (negative logic)	Input
3	GND	Ground	GND
4	RESET-	Driver Enable Signal Input (negative logic)	Input
5	Vs	MOSFET Source Connection	Output
6	NC	No connention (no bondwire)	---
7	Ho	MOSFET Gate Connection	Output
8	V_B	Driver Output Stage Supply	POWER

2.4 Package outline description

TITLE: PLASTIC SMALL OUTLINE PACKAGE 8L (ST & ASE subcon)

PACKAGE CODE: O7 (O like OSCAR), KU e K2
PACKAGE WEIGHT: 0,0765 g/unit typ
JEDEC/EIAJ REFERENCE NUMBER: JEDEC MS-012-AA

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.75			1.74	
A1	0.10		0.25	0.12	0.15	0.18	
A2	1.25			1.48	1.52	1.56	
b	0.28		0.48	0.375	0.40	0.425	
c	0.17		0.23	0.192	0.20	0.225	
D	4.80	4.90	5.00	4.87	4.90	4.93	(1)
E	5.80	6.00	6.20	5.90	6.00	6.10	
E1	3.80	3.90	4.00	3.87	3.90	3.93	(2)
e		1.27			1.27		
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	SEE LEADFRAME OPTIONS			
L1		1.04			1.05		
k	0		8	2	4	8	DEGREES
ccc			0.10			0.04	

	LEADFRAME OPTIONS						
	PREPLATED			POSTPLATED			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
L	0.567	0.617	0.667	0.585	0.635	0.685	

NOTES:

(1) – Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).

(2) – Dimension “E1” does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.

ST RESTRICTED - ST RESTRICTED - ST RESTRICTED - S

FIGURE : 1 — DOC. NUMBER : 0016023

TITLE : POA PLASTIC SMALL OUTLINE PACKAGE 8L (ST type & ASE subcon type)

D
A
A2
A1
b
ccc C
8
5
1
4
E1
E
e
hx45°
C
SEE VIEW "C"
0.25 GAUGE PLANE
K
SEATING PLANE
c
L
L1
SEE VIEW "C"

MATERIAL

NATIVE SCALE

PROJECTION

DIM are in mm – Unspecified tolerance						
Precision rate	0 mm 6 mm	6,01 mm 30 mm	30,01mm 120 mm	120,01mm 315 mm	over 315 mm	Angular
Coarse	±0.2	±0.5	±0.8	±1.2	±2	±1°
Medium	±0.1	±0.2	±0.3	±0.5	±0.8	±0°30'
Fine	±0.05	±0.1	±0.15	±0.2	±0.3	±0°20'

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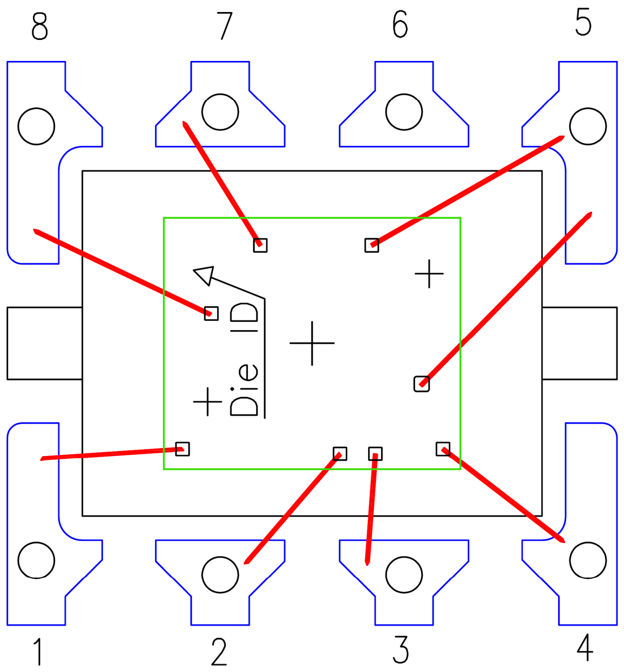
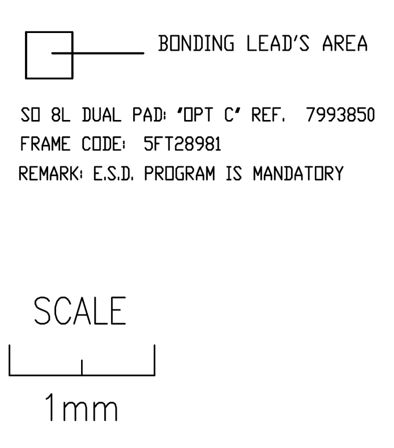
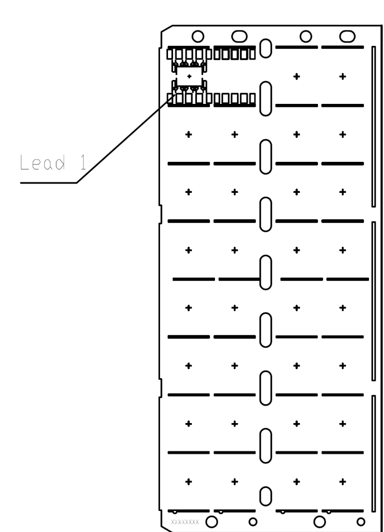
2.5 Bonding diagram

FRAME PAD : 94 x 125 mils / 2,388 x 3,175 mm







2.6 Traceability

Wafer fab information		
Manufacturing location	*Ang Mo Kio 6”*	
Silicon process technology	*BCD OFFLINE*	
Die size	*2200 µm, 1900 µm*	
Passivation	*SiN*	
Back side die finishing	*Lapped silicon*	
Metallization	*1 metal layer*	
Raw line code	*SMKU*U356BA6*	
Diffusion lots	*V6235K3V*	*V6313K9F*
Trace codes	*GK3090HB*	*GK33309Y*
Markings	*U356NN / ST GK309* *U356HH / ST GK309* *U356LL / ST GK309*	*L9856 / ST GK333*

Assembly information	
Assembly plant	*ST Shenzhen - China*
Package	*SO 08 Strip single island 4+3+1*
Wire	*Au 3N 1 mil*
Resin	*Sumitomo EME-G700KC*
Die attach	*Ablebond 8601S-25*
Frame description	*SO 8L 94x125 Mt HD OpC NiThPdAgAu*

Testing information	
Tester	*QT200 pwr*
Programs	*U356FA01, U356FH01, U356FC01*
Testing site	*Muar*

3 RELIABILITY TEST RESULTS

3.1 Reliability test plan and result summary

Tracecode: GK3090HB

N.	Test name	Condition	Result Fail / Sample size	Note
1	PC (JL3)	24h bake, 192h 30°C / 60%, 3 reflow (T_{peak}=260°C) + + 100cy [1]	0 / 308-135-135	Before HTOL, THB, AC, TC
2	HTRB	T_j= 150°C, V_B=418V, V_{CC}=18V, t=1000h extended to 2000h	0 / 45	2
3	HTOL	T_j=150°C, V_{BVD}=150V, V_{BD}=18V, V_{CCD}=5V, t=1000h	0 / 77	3, 4
4	THB	T_a=85°C, R.H.=85%, V_B=100V, V_{CC}=18V, t=1000h extended to 2000h	0 / 77-45-45	5
5	TC	T_a= -50°C / 150°C, n=1000cy extended to 2000cy	0 / 77-45-45	5, 6
6	AC	T_a=121°C, P=2.08atm, t=96h	0 / 77-45-45	
7	HTSL	T_a= 150°C, t=1000h extended to 2000h	0 / 45-40-40	5, 6
8	ESD	Charge Device Model	0 / 15	5, 6, 7

Notes
[1] After PC (JL3), TC (100cy, -50°C/+150°C) has been performed.
[2] No significant drift on key parameters after 0h-2000h drift analysis.
[3] No significant drift on key parameters after 0h-1000h drift analysis.
[4] Tested at 3T (hot / cold gonogo, ambient with datalog).
[5] Tested at 2T (hot / ambient gonogo).
[6] Wire Bond Pull (WBP) and Wire Ball Shear (WBS) have been performed on virgin parts with positive results (data from assy report). After TC and HTSL (2000cy/2000h) tests, WBP has been performed with positive results (data in U356BA SO8_SHZ Physical Analysis report).
[7] ESD details:

Level	Combination	Result
+/-250V	All pins	3 good
+/-500V	All pins	3 good
+/-750V	Corner pins	3 good
Extended level:		
+/-1000V	All pins	3 good
+/-1500V	All pins	3 good

Tracecode:GK33309Y

N.	Test name	Condition	Result Fail / Sample size	Note
1	PC (JL3)	24h bake, 192h 30°C / 60%, 3 reflow (T_{peak}=260°C) + + 100cy [1]	0 / 308	Before HTOL, THB, ES, TC
2	HTRB	T_j= 150°C, V_B=418V, V_{CC}=18V, t=1000h	0 / 45	2
3	HTOL	T_j=150°C, V_{BVD}=150V, V_{BD}=18V, V_{CCD}=5V, t=1000h	0 / 77	2, 3
4	THB	Ta=85°C, R.H.=85%, V_B=100V, V_{CC}=18V, t=1000h	0 / 77	4
5	TC	T_a= -50°C / 150°C, n=1000cy	0 / 77	4, 5
6	ES	100cy + T_a=121°C, P=2.08atm, t=96h	0 / 77	
7	HTSL	T_a= 150°C, t=1000h	0 / 45	4, 5

Notes
[1] After PC (JL3), TC (100cy, -50°C/+150°C) has been performed.
[2] No significant drift on key parameters after 0h-1000h drift analysis.
[3] Tested at 3T (hot / cold gonogo, ambient with datalog).
[4] Tested at 2T (hot / ambient gonogo).
[5] Wire Bond Pull (WBP) and Wire Ball Shear (WBS) have been performed on virgin parts with positive results (data from assy report). After TC and HTSL tests, WBP has been performed with positive results (data in U356BA SO8_SHZ Physical Analysis report).

3.2 Test result summary basing on AEC-Q100 qualification test plan template

TEST GROUP A - ACCELERATED ENVIRONMENT STRESS TESTS								
AEC#	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	*Tracecode: GK3090HB* **Fails / Parts for each split / Lot**	*Tracecode: GK33309Y* **Fails / Parts / Lot**	**Note**
A1	**PC** Pre-Cond	JEDEC J-STD-020	24h bake T_a=125°C 192h T_a=30°C/60%=RH 3 reflow simulation T_{max}=260°C	Room	All prior to: AC, ES, THB, TC	0 / 308+135+135 / 1	0 / 308 / 1	PC has been applied also on HTOL parts
A2	**THB** Temperature Humidity Bias	JESD22 A101/A110	T_a=85°C RH=85% 1000h	Room Hot	77 / 3	0 / 77+45+45 / 1	0 / 77 / 1	
A3	**AC** Auto-clave	JESD22 A102/A118	P=2.08atm T_a=121°C 96h	Room	77 / 3	0 / 77+45+45 / 1	0 / 77 / 1	
A4	**TC** Temperature Cycling	JESD22 A104	T_a=-50/+150°C 1000cy	Hot (and also Room)	77 / 3	0 / 77+45+45 / 1 WBP after 2000cy passed (> 3gr)	0 / 77 / 1 WBP after 1000cy passed (> 3gr)	
A5	**PTC** Power Temperature Cycle	JESD22 A105	Tj=-40/+150°C 1000cy	Room Hot	45 / 1			Not applicable (pre-driver device, doesn't drive directly inductor, P_d<1W)
A6	**HTSL** High Temperature Storage Life	JESD22 A103	T_a=150°C 1000h	Room Hot	45 / 1	0 / 77+45+45 / 1 WBP after 2000h passed (> 3gr)	0 / 45 / 1 WBP after 1000h passed (> 3gr)	

Note

Additional tests

High Temperature Reverse Bias [Tj= 150°C, 1000h] has been done with no failures.
Enviroment Storage [TC (100cy -50ºC / 150°C) + AC 96h] has been done with no failures.

Extended tests

High Temperature Reverse Bias	2000h	No fails: 0 / 45 / 1 lot.
Temperature Humidity Bias	2000h	No fails: 0 / 77+45+45 / 1 lot.
Temperature Cycling	2000cy	No fails: 0 / 77+45+45 / 1 lot.
High Temperature Storage Life	2000h	No fails: 0 / 77+45+45 / 1 lot.

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TEST								
AEC#	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	*Tracecode: GK3090HB* **Fails / Parts / Lot**	*Tracecode: GK33309Y* **Fails / Parts/ Lot**	**Note**
B1	**HTOL** High Temperature Operating Life	JESD22 A108	T_j=150°C 1000h	Room Hot Cold	77 / 3	0 / 77 / 1	0 / 77 / 1	
B2	**ELFR** Early Life Failure Rate	AEC Q100 008	T_j=125°C 24h	Room Hot	800 / 3	-	-	Data from Burnin
B3	**EDR** Endurance Data Retention Op. Life	AEC Q100 005						Not applicable (no memory inside)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS								
C1	**WBS** Wire Bond Shear	AEC Q100 001			30 bonds 5 devices	Passed	Passed	Done in assy plant on virgin samples.
C2	**WBP** Wire Bond Pull	MIL-STD 883 – 2011			30 bonds 5 devices	Passed	Passed	Done in assy plant on virgin samples. Done after TC. Done also after HTSL.
C3	**SD** Solderability	JESD22 B102			15 / 1	Passed	Passed	Done in assy plant on virgin samples.
C4	**PD** Physical Dimension	JESD22 B100/B108			10 / 3	Passed	Passed	Done in assy plant on virgin samples.
C5	**SBS** Solder Ball Shear	AEC Q100 010			5 balls 10 devices	-	-	Not applicable. For BGA only
C6	**LI** Lead Integrity	JESD22 B105		No lead breakage or finish cracks	5 / 1	-	-	Not required for surface mount devices.

TEST GROUP D – DIE FABBRICATION RELIABILITY TEST							
AEC#	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	**Results Fails / Parts / Lot**	**Note**
D1	**EM** Electro-migration					BCD OFFLINE process qual.	
D2	**TDDB** Time Dependent Dielectric BV					BCD OFFLINE process qual.	
D3	**HCI** Hot Carrier Injection					BCD OFFLINE process qual.	
D4	**NBTI** Negative Bias Temperature Instability					BCD OFFLINE process qual.	
D5	**SM** Stress Migration					BCD OFFLINE process qual.	

TEST GROUP E – ELECTRICAL VERIFICATION TESTS								
AEC #	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	*Tracecode: GK3090HB* **Results Fails/ Parts/ Lot**	*Tracecode: GK33309Y* **Results Fails / Parts/ Lot**	**Note**
E1	**TEST**				All units	All units	All units	
E2	**ESD MM / HBM** Electrostatic Discharge	AEC Q100 002/3		Room Hot	3 x Vlevel x pin comb. / 2			Not required
E3	**ESD CDM** Electrostatic Discharge	AEC Q100 011	±500V All pins ±750V Corner pins	Room Hot	3 x Vlevel / 2	0 / 15 / 1		Done but not required
E4	**LU** Latch-up	AEC Q100 004	Current Injection Power supply sequence Overvoltage on power supply Room / Hot	Room Hot	12 / 2			Not required
E5	**ED**	AEC Q100 009	Electrical Distribution			passed	passed	
E6	**FG**	AEC Q100 007	Fault Grading					Not applicable
E7	**CHAR**	AEC Q003	Characterization (Rm/Hot/Cold)					
E8	**GL** Electrothermally Induced Gate Leakage	AEC Q100 006	Electro-Thermally Induced Gate Leakage: (Rm)	Room Hot	6 / 1	-		Not mandatory
E9	**EMC** Electromagnetic Compatibility	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions): <40dBuV at 10kHz-1MHz		-	-		Not applicable
E10	**SC** Short Circuit	AEC Q100 012	Short Circuit Characterization	-	-	-		Not applicable
E11	**SER**	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-		Not applicable

TEST GROUP F – DEFECT SCREENING TEST							
AEC #	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	**Results**	**Note**
F1	**PAT** Process Average Testing	AEC Q001	See AEC Q001				
F2	**SBA** Statistical Bin Yield Analysis	AEC Q002	See AEC Q002				

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS							
AEC #	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	**Results Fails / Parts/ Lot**	**Note**
G1	**MS** Mechanical Shock	JEDEC JESD22 B104				-	Not required for surface mount devices.
G2	**VFV** Variable Frequency Vibration	JEDEC JESD22 B103				-	Not required for surface mount devices.
G3	**CA** Constant Acceleration	MIL-STD 883 Method 2001				-	Not required for surface mount devices.
G4	**GFL** Gross/Fine Leak	MIL-STD 883 Method 1014				-	Not required for surface mount devices.
G5	**DROP** Package Drop	-				-	Not required for surface mount devices.
G6	**LT** Lid Torque	MIL-STD 883 Method 2024				-	Not required for surface mount devices.
G7	**DS** Die Shear	MIL-STD 883 Method 2019				-	Not required for surface mount devices.
G8	**IWV** Internal Water Vapor	MIL-STD 883 Method 1018				-	Not required for surface mount devices.

3.3 Test description

Test name	Description	Purpose
PC (JL3) Preconditioning (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.	*As stand-alone test:* to investigate the level of moisture sensitivity. *As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, approaching the absolute ratings in terms of junction temperature and supply voltage, minimizing the power dissipation.	The main failure mechanisms can be divided into two groups: the first group includes those degradation phenomena which take place in the silicon active areas and interconnections due to the combined action of temperature and electrical fields. The second is linked to the plastic package. The key package elements are the wire bonds and the pads. The test focuses the attention on oxide ageing, parasitic surface effects induced by mobile charge contamination.
HTOL High Temperature Operating Life	The device is stressed in dynamic configuration, approaching the max. operative ratings in terms of junction temperature, load current, internal power dissipation.	To simulate the worst-case application stress conditions. The typical failure modes are related to electro-migration, wire-bonds degradation, oxide faults, thermo-migration.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failures, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.
AC Autoclave	The unbiased device is stored in a saturated steam, at fixed and controlled conditions of pressure and temperature.	This test is performed to point out critical water entry paths with consequent corrosion effects affecting die or package materials, related to chemical contamination.
ES Enviroment sequence (JL3+TC200cy+AC96h)	The unbiased device is submitted to cycled temperature excursions, between a hot and a cold chamber in air and then is stored in a saturated steam, at fixed and controlled conditions of pressure and temperature.	This test is performed to point out critical water entry paths with consequent corrosion effects affecting die or package materials, related to chemical contamination. To emphatize the failure modes linked to water entry paths, the parts have been preceeded by JL3+TC200cy
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, metal stress-voiding.
ESD (CDM) Electrostatic Discharge (Charged Device Model)	Each device lies on its back. It is charged by field or by a charging probe. Each pin individually is discharged through a discharging probe connected to ground.	To evaluate adequate pin protections to electrostatic discharge.

4 ATTACHMENTS

4.1 HTOL schematic

TEST CONDITION
VCC = + 5V VB = + 18V VBV = + 150V
DIGITAL STIM
IN-(freq.)=50KHz IN- = 0-5V RESET- = 0-5 V VSTIM= 0-5 V

WIRE MODIFICATION

ELES SEMICONDUCTOR EQUIPMENT

P/N SCH00572700

U356 OLT
SOP8 DUT2
(RACK HV OVEN)

DESIGNED BY: FABRIZIO FIDENZI
CHECKED BY:
APPROVED BY:
FILE NAME: DUT
3-6-2013_10:46
SHEET 6 OF 6

REVISION HISTORY
REV1 N. .... OF ../../.... SEE PDM N. ../.....
REV2 N. .... OF ../../.... SEE PDM N. ../.....
REV3 N. .... OF ../../.... SEE PDM N. ../.....

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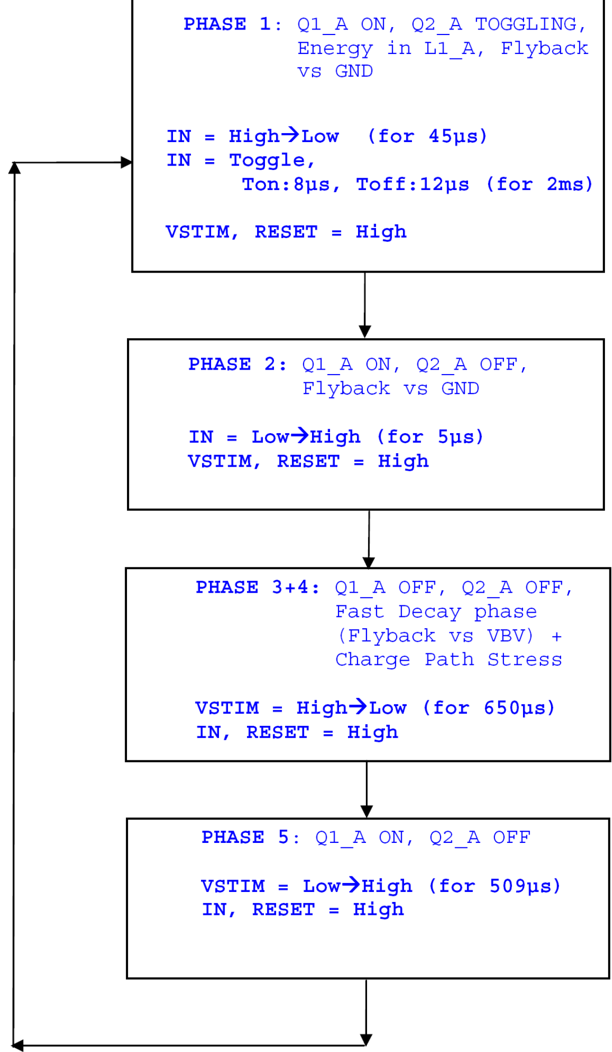
ANY USE BY A THIRD PART WITHOUT PRIOR AUTHORIZATION BY THE COMPANY SHALL BE PURSUED ACCORDING TO LAW

Note
Jumper settings: JP1, JP3, JP4: open; JP2, JP7 closed.

4.2 HTOL pattern



4.3 HTOL waveforms overview

Pattern cycle

Fig. 1: CH1: IN, CH2: VSTIM, CH3: RESET

HO, VS during pattern cycle

Fig. 15: CH1: IN, CH2: VSTIM, CH3: HO_A, CH4: VS_A

IN, VS, HO detail

Fig. 10: CH1: IN, CH2: Voltage on Pin 5 DUT, CH3: Voltage on Pin 8 DUT
M: CH3-CH2 = V_C2

V_C2 (little overload)

Fig. 17: CH1: V_C2 CH2: IN
NOTE: IN: voltage on IN signal vs VS

V_a negative peaks

Fig. 7: CH1: Va, CH3: IN, CH4: I_D2_A

V_a negative peak detail

Fig. 8: CH1: Va, CH3: IN

4.4 THB / HTRB schematic

VIN
JP3 1 2 3
1K R8
VCC R7 1K
C1 100NF 100V
VRES
JP4 1 2 3
1K R9

DUT1
U356
VCC 1
IN- 2
GND 3
RESET- 4
8 VB
7 HO
6 NC
5 VS
OTS-8(16)-1,27-03 ENPLAS ZOCC
ENPLAS

R30 200K N HO
JP1
JP2
R5 10K VB
18V DZ1 5W
C2 100NF 100V
R6 200K N VS
(+ 400 V)
R1 1M21 R264 1M21
R2 1M21 R263 1M21
R3 1M21 R262 1M21
R4 1M21 R261 1M21
GND

TEST CONDITION

HTRB	THB
VCC = + 18V VB = + 418V	VCC = + 18V VB = + 100V
VRES = +18V VIN = floating	VRES = +18V VIN = floating

JUMPER CONFIGURATION

JP1	JP2	JP3	JP4
open	closed	1-2	2-3

IN-	RESET-
0V	18V

REVISION HISTORY
REV1 N. ... OF ../../.... SEE PDM N. ../.....
REV2 N. ... OF ../../.... SEE PDM N. ../.....
REV3 N. ... OF ../../.... SEE PDM N. ../.....
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ELES SEMICONDUCTOR EQUIPMENT
P/N SCH00568801
U356 HTRB/THB
SOP8 DUT24
150X400
DESIGNED BY: FABRIZIO FIDENZI
CHECKED BY:
APPROVED BY:
FILE NAME: DUT
9-10-2013_11:41
SHEET 3 OF 3

Note
The 400V value at Vs test point is valid only for HTRB.

5 TEST GLOSSARY

Test name	Description
ESD (CDM)	Electrostatic Discharge (Charged Device Model)
HTSL	High Temperature Storage Life test
HTOL	High Temperature Operating Life test
THB	Temperature Humidity Bias test
TC	Temperature Cycling test
AC	Autoclave
ES	Environmental Sequence
HTRB	High Temperature Reverse Bias test
PC (JL3)	Preconditioning (Jedec Level 3)
WBP	Wire Bond Pull
WBS	Wire Ball Shear

6 REVISION HISTORY

Version	Date	Pages	Author
1.0	April 14th 2014	20	M.Corradini

Reliability Report
UC24aa6
SO8 transfer to Shenzhen

General Information	
Product line / version	*UC24 / aa*
Commercial name	*UC24-TR-X-S*
Product group / division	*APG / Powertrain & Safety*
Package	*SO 08 Strip single island4+3+1*
Silicon process technology	*BCD3*

Locations	
Wafer fab	*Ang Mo Kio 6”*
Assembly plant	*ST Shenzhen*
Reliability assessment	*Passed*

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW 3
1.1 OBJECTIVES 3
1.2 EXTRACT FROM AEC-Q100 PROCESS CHANGE QUALIFICATION GUIDELINES. 4
1.3 CONCLUSION 4
2 PACKAGE OUTLINE DESCRIPTION 5
2.1 BONDING DIAGRAM 7
2.2 TRACEABILITY 8
3 RELIABILITY TEST RESULTS 9
3.1 RELIABILITY TEST PLAN AND RESULT SUMMARY 9
3.2 TEST RESULT SUMMARY BASING ON AEC-Q100 QUALIFICATION TEST PLAN TEMPLATE 10
3.3 TEST DESCRIPTION 14
4 TEST GLOSSARY 15
5 REVISION HISTORY 15

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on *UC24aa6 assembled in SO8 Shenzhen.*

UC24 is one of TV.s used to qualify the S08 transfer to *Shenzhen.*
Here below the devices in the same package on which qualification has been done.

DEVICE	U356	UC24	U520
RL	SMKU*U356BA6	SMKU*UC24AA6	SMKU*U520CB6
FE Process	BCD Offline	BCD3	BCD2
FE Fab	AMK6	AMK6	AMK6
BPO	90*90	90*90	127*127
Die area	2200*1900	1680*2330	2270*1800
Front/back side metal	SiN (nitride) / Lapped silicon	SiN (nitride) / Raw Si	SiN (nitride) / CrNi
L/F descr	FRAME SO 8L 94x125	FRAME SO 8L 94x125	FRAME SO 8L 94x125
Frame option	C	C	D
Au wire	1.0mil 3N	1.0mil 3N	1.3mil 4N
Resin	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC
Glue	ABLEBOND	ABLEBOND	ABLEBOND
Down bonding	No	No	Wire on BTWG

DEVICE	UN43	UH01	W023
RL	SMKU*UN43BA6	SMKU*UH01BB6	SMKU*W023FB6
FE Process	BCD5	BCD4	BIP
FE Fab	AMK6	AMK6	AMK6
BPO		90*90	101*101
Die area	1530*1840	1700*2010	2160*1960
Front/back side metal		USG-PSG-SiON-PIX / Raw Si	SiN (nitride) / CrNi
L/F descr	FRAME SO 8L 94x125	FRAME SO 8L 94x125	FRAME SO 8L 94x125
Frame option	C	C	C
Au wire	1.0mil 3N	1.0mil 3N	1.0mil 4N
Resin	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC	SUMITOMO EME-G700KC
Glue	ABLEBOND	ABLEBOND	ABLEBOND
Down bonding		No	No

For the reliability evaluation of UC24, the following tests have been carried out:

- PC (JL3) + 100cy TC + TC.
- PC (JL3) + 100cy TC + AC/ES.
- HTSL.
- WBP and WBS.

1.2 Extract from AEC-Q100 process change qualification guidelines.

A2 Temperature Humidity Bias or HAST
A3 Autoclave or Unbiased HAST
A4 Temperature Cycling
A5 Power Temperature Cycling
A6 High Temperature Storage Life
B1 High Temperature Operating Life
B2 Early Life Failure Rate
B3 NVM Endurance, Data Retention
C1 Wire Bond Shear
C2 Wire Bond Pull
C3 Solderability
C4 Physical Dimensions
C5 Solder Ball Shear
C6 Lead Integrity
D1 Electromigration
D2 Time Dependent Dielectric Breakdown
D3 Hot Carrier Injection
D4 Negative Bias Temperature Instability
D5 Stress Migration
E2 Human Body / Machine Model ESD
E3 Charged Device Model ESD
E4 Latch-up
E5 Electrical Distribution
E7 Characterization
E8 Gate Leakage
E9 Electromagnetic Compatibility
E10 Short Circuit Characterization
E11 Soft Error Rate
G1-4 Mechanical Series
G5 Package Drop
G6 Lid Torque
G7 Die Shear
G8 Internal Water Vapor

Note: A letter or "●" indicates that performance of that stress test should be **considered** for the appropriate process change

Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E8	E9	E10	E11	G1-G4	G5	G6	G7	G8
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	EM	TDDB	HCI	NBTI	SM	HBM / MM	CDM	LU	ED	CHAR	GL	EMC	SC	SER	MECH	DROP	LT	DS	IWV
ASSEMBLY																																	
Die Overcoat / Underfill	●	●	●	M	●	●																			S			●					H
Leadframe Plating	●	●	●	M	●					C	●			●																		H	
Bump Material / Metal System	●	●	●	M	●	●						●	●															●					
Leadframe Material		●	●	M	●					●	●	●		●													●		H			H	
Leadframe Dimension		●	●	M							●	●		●													●		H				
Wire Bonding		●	●	Q	●				●	●													M				●		H				
Die Scribe/Separate	●	●	●	M																													
Die Preparation / Clean	●	●		M		●			●	●																						H	
Package Marking											B																						
Die Attach	●	●	●	M		●																	●				●		H			H	H
Molding Compound	●	●	●	M	●	●	●				●	●		●											S			●					
Molding Process	●	●	●	M	●	●					●	●		●											S								
Hermetic Sealing		H	H		H							H		H															H		H		H
New Package	●	●	●	M	●	●	●		●	●	●	●	T	●						●	●		●		S		●		H			H	H
Substrate / Interposer	●	●	●	M	●	●			●	●			T												S				H			H	H
Assembly Site Transfer	●	●	●	M		●	●		●	●	●	●	T	●									●		S				H			H	H

A Only for peripheral routing
B For symbol rework, new cure time, temp
C If bond to leadfinger
D Design rule change
E Thickness only
F MEMS element only
G Only from non-100% burned-in parts
H Hermetic only
J EPROM or E^2PROM
K Passivation only
M For devices requiring PTC
N Passivation and gate oxide
P Passivation and interlevel dielectric
Q Wire diameter decrease
S For plastic SMD only
T For Solder Ball SMD only

Note1

In red the changes respect to previous.

Note2

PTC, SC	not applicable (Pd < 1W).
SBS	not applicable (required for BGA only).
SER, MECH, DS, IWV	not applicable (required for hermetic package only).
LI	not applicable (required for through-hole package only).
GL	not done, not mandatory.
THB, HTOL, ELFR	not done (performed on other test vehicles).

Note3

WBS, SD, PD	data from assy report / assy data.

1.3 Conclusion

The reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.
WBP done after TC and HTSL is positive.
On the basis of the overall positive results, *UC24aa6 in SO8 (Shenzhen)* can be qualified from a reliability point of view.

2 PACKAGE OUTLINE DESCRIPTION

TITLE: PLASTIC SMALL OUTLINE PACKAGE 8L (ST & ASE subcon)

PACKAGE CODE: O7 (O like OSCAR), KU e K2
PACKAGE WEIGHT: 0,0765 g/unit typ
JEDEC/EIAJ REFERENCE NUMBER: JEDEC MS-012-AA

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.75			1.74	
A1	0.10		0.25	0.12	0.15	0.18	
A2	1.25			1.48	1.52	1.56	
b	0.28		0.48	0.375	0.40	0.425	
c	0.17		0.23	0.192	0.20	0.225	
D	4.80	4.90	5.00	4.87	4.90	4.93	(1)
E	5.80	6.00	6.20	5.90	6.00	6.10	
E1	3.80	3.90	4.00	3.87	3.90	3.93	(2)
e		1.27			1.27		
h	0.25		0.50	0.425		0.50	
L	0.40		1.27	SEE LEADFRAME OPTIONS			
L1		1.04			1.05		
k	0		8	2	4	8	DEGREES
ccc			0.10			0.04	

	LEADFRAME OPTIONS						
	PREPLATED			POSTPLATED			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
L	0.567	0.617	0.667	0.585	0.635	0.685	

NOTES:

(1) – Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).

(2) – Dimension “E1” does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.

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TITLE : POA PLASTIC SMALL OUTLINE PACKAGE 8L (ST type & ASE subcon type)

FIGURE : 1

DOC. NUMBER : 0016023

NATIVE SCALE

PROJECTION

MATERIAL

DIM are in mm - Unspecified tolerance

Precision rate	0 mm 6 mm	6,01 mm 30 mm	30,01mm 120 mm	120,01mm 315 mm	over 315 mm	Angular
Coarse	±0.2	±0.5	±0.8	±1.2	±2	±1°
Medium	±0.1	±0.2	±0.3	±0.5	±0.8	±0°30'
Fine	±0.05	±0.1	±0.15	±0.2	±0.3	±0°20'

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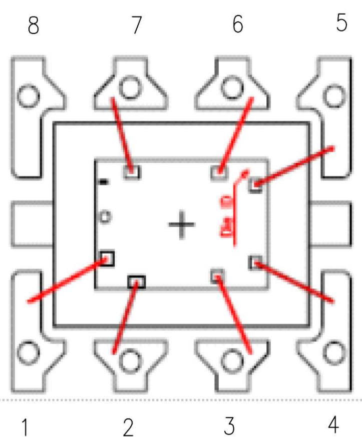
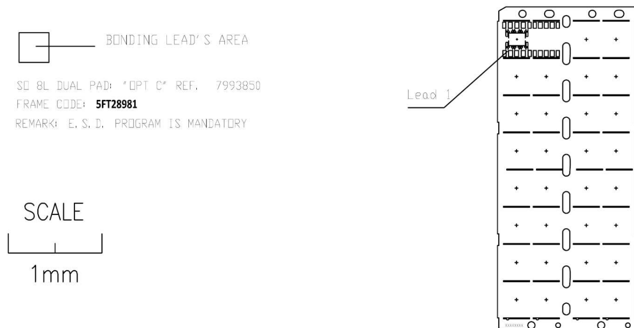
2.1 Bonding diagram

BONDING DIAGRAM FOR LINE : UC24 IN SO8 OPT C HD SHENZHEN

FRAME PAD : $\frac{94 \text{ x } 125 \text{ mils}}{2,388 \text{ x } 3,175 \text{ mm}}$





2.2 Traceability

Wafer fab information		
Manufacturing location	*Ang Mo Kio 6"*	
Silicon process technology	*BCD3*	
Die size	*1680 µm, 2330 µm*	
Passivation	*SiN*	
Back side die finishing	*Raw silicon*	
Metallization	*2 metal layers*	
Raw line code	*SMKU*UC24AA6*	
Diffusion lots	*V62306VX*	*V6316KXV*
Trace codes	*GK3100AV*	*GK330A0*
Markings	*UC24NN / ST GK310* *UC24HH / ST GK310* *UC24LL / ST GK310*	*40060 / ST GK333*

Assembly information	
Assembly plant	*ST Shenzhen - China*
Package	*SO 08 Strip single island 4+3+1*
Wire	*Au 3N 1 mil*
Resin	*Sumitomo EME-G700KC*
Die attach	*Ablebond 8601S-25*
Frame description	*SO 8L 94x125 Mt HD OpC NiThPdAgAu*

Testing information	
Tester	Sz
Program	UC24FH01
Testing site	*Muar*

3 RELIABILITY TEST RESULTS

3.1 Reliability test plan and result summary

Tracecode: GK3100AV

N.	Test name	Condition	Result Fail / Sample size	Note
1	**PC (JL3)**	24h bake, 192h 30°C / 60%, 3 reflow (T_{peak}=260°C) + + 100cy [1]	0 / 144-90-90	Before AC, TC
2	**TC**	T_a= -50°C / 150°C, n=1000cy extended to 1500cy	0 / 77-45-45	[2, 3]
3	**AC**	T_a=121°C, P=2.08atm, t=96h	0 / 77-45-45	[2]
4	**HTSL**	T_a= 150°C, t=1000h extended to 2000h	0 / 45-40-40	[2, 3]

Notes
[1] After PC (JL3), TC (100cy, -50°C/+150°C) has been performed.
[2] Tested at 1T (hot).
[3] Wire Bond Pull (WBP) and Wire Ball Shear (WBS) have been performed on virgin parts with positive results (data from assy report).
After TC and HTSL (1500cy/2000h) tests, WBP has been performed with positive results (data in UC24AA SO8_SHZ Physical Analysis report).

Tracecode: GK330A0

N.	Test name	Condition	Result Fail / Sample size	Note
1	**PC (JL3)**	24h bake, 192h 30°C / 60%, 3 reflow (T_{peak}=260°C) + + 100cy [1]	0 / 144	Before ES, TC
5	**TC**	T_a= -50°C / 150°C, n=1000cy	0 / 77	[2, 3]
6	**ES**	100cy + T_a=121°C, P=2.08atm, t=96h	0 / 77	[2]
7	**HTSL**	T_a= 150°C, t=1000h	0 / 45	[2, 3]

Notes
[1] After PC (JL3), TC (100cy, -50°C/+150°C) has been performed.
[2] Tested at 1T (hot).
[3] Wire Bond Pull (WBP) and Wire Ball Shear (WBS) have been performed on virgin parts with positive results (data from assy report).
After TC tests, WBP has been performed with positive results (data in UC24AA SO8_SHZ Physical Analysis report).

3.2 Test result summary basing on AEC-Q100 qualification test plan template

TEST GROUP A - ACCELERATED ENVIRONMENT STRESS TESTS								
AEC#	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	*Tracecode: GK3100AV* **Fails / Parts for each split / Lot**	*Tracecode: GK330A0* **Fails / Parts / Lot**	**Note**
A1	**PC** Pre-Cond	JEDEC J-STD-020	24h bake T_a=125°C 192h T_a=30°C/60%=RH 3 reflow simulation T_{max}=260°C	Room	All prior to: AC, ES, TC	0 / 144-90-90 / 1	0 / 144 / 1	
A2	**THB** Temperature Humidity Bias	JESD22 A101/A110	T_a=85°C RH=85% 1000h	Room Hot	77 / 3			Not done (performed on other test vehicles).
A3	**AC** Auto-clave	JESD22 A102/A118	P=2.08atm T_a=121°C 96h	Room	77 / 3	0 / 77+45+45 / 1	0 / 77 / 1	
A4	**TC** Temperature Cycling	JESD22 A104	T_a=-50/+150°C 1000cy	Hot (and also Room)	77 / 3	0 / 77+45+45 / 1 WBP after 1500cy passed (> 3gr)	0 / 77 / 1 WBP after 1000cy passed (> 3gr)	
A5	**PTC** Power Temperature Cycle	JESD22 A105	Tj=-40/+150°C 1000cy	Room Hot	45 / 1			Not applicable (P_d<1W)
A6	**HTSL** High Temperature Storage Life	JESD22 A103	T_a=150°C 1000h	Room Hot	45 / 1	0 / 45+40+40 / 1 WBP after 2000h passed (> 3gr)	0 / 45 / 1	

Note

Additional test

Enviroment Storage [TC (100cy -50ºC / 150°C) + AC 96h] has been done with no failures.

Extended tests

Temperature Cycling	1500cy	No fails: 0 / 77+45+45 / 1 lot.
High Temperature Storage Life	2000h	No fails: 0 / 45+40+40 / 1 lot.

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TEST

AEC#	Test	Q100 reference	Test conditions	Testing temperature	Q100 sample s./ lots	*Tracecode: GK3100AV* Fails / Parts / Lot	*Tracecode: GK330A0* Fails / Parts/ Lot	Note
B1	**HTOL** High Temperature Operating Life	JESD22 A108	T_j=150°C 1000h	Room Hot Cold	77 / 3			Not done (performed on other test vehicles).
B2	**ELFR** Early Life Failure Rate	AEC Q100 008	T_j=125°C 24h	Room Hot	800 / 3	-	-	Not done (performed on other test vehicles).
B3	**EDR** Endurance Data Retention Op. Life	AEC Q100 005						Not applicable (no memory inside)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

AEC#	Test	Q100 reference	Test conditions	Testing temperature	Q100 sample s./ lots	Fails / Parts / Lot	Fails / Parts/ Lot	Note
C1	**WBS** Wire Bond Shear	AEC Q100 001			30 bonds 5 devices	Passed	Passed	Done in assy plant on virgin samples.
C2	**WBP** Wire Bond Pull	MIL-STD 883 – 2011			30 bonds 5 devices	Passed	Passed	Done in assy plant on virgin samples. Done after TC. Done also after HTSL.
C3	**SD** Solderability	JESD22 B102			15 / 1	Passed	Passed	Done in assy plant on virgin samples.
C4	**PD** Physical Dimension	JESD22 B100/B108			10 / 3	Passed	Passed	Done in assy plant on virgin samples.
C5	**SBS** Solder Ball Shear	AEC Q100 010			5 balls 10 devices	-	-	Not applicable. For BGA only
C6	**LI** Lead Integrity	JESD22 B105		No lead breakage or finish cracks	5 / 1	-	-	Not required for surface mount devices.

TEST GROUP D – DIE FABBRICATION RELIABILITY TEST

AEC#	Test	Q100 reference	Test conditions	Testing temperature	Q100 sample s./ lots	Results Fails / Parts / Lot	Note
D1	**EM** Electro-migration					BCD3 process qual.	
D2	**TDDB** Time Dependent Dielectric BV					BCD3 process qual.	
D3	**HCI** Hot Carrier Injection					BCD3 process qual.	
D4	**NBTI** Negative Bias Temperature Instability					BCD3 process qual.	
D5	**SM** Stress Migration					BCD3 process qual.	

TEST GROUP E – ELECTRICAL VERIFICATION TESTS

AEC #	Test	Q100 reference	Test conditions	Testing temperature	Q100 sample s./ lots	*Tracecode: GK3100AV* Results Fails/ Parts/ Lot	*Tracecode: GK330A0* Results Fails / Parts/ Lot	Note
E1	**TEST**				All units	All units	All units	
E2	**ESD MM / HBM** Electrostatic Discharge	AEC Q100 002/3		Room Hot	3 x Vlevel x pin comb. / 2			Not required
E3	**ESD CDM** Electrostatic Discharge	AEC Q100 011	±500V All pins ±750V Corner pins	Room Hot	3 x Vlevel / 2			Not required
E4	**LU** Latch-up	AEC Q100 004	Current Injection Power supply sequence Overvoltage on power supply Room / Hot	Room Hot	12 / 2			Not required
E5	**ED**	AEC Q100 009	Electrical Distribution					
E6	**FG**	AEC Q100 007	Fault Grading					Not applicable
E7	**CHAR**	AEC Q003	Characterization (Rm/Hot/Cold)					
E8	**GL** Electrothermally Induced Gate Leakage	AEC Q100 006	Electro-Thermally Induced Gate Leakage: (Rm)	Room Hot	6 / 1	-		Not mandatory
E9	**EMC** Electromagnetic Compatibility	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions): <40dBuV at 10kHz-1MHz		-	-		Not applicable
E10	**SC** Short Circuit	AEC Q100 012	Short Circuit Characterization	-	-	-		Not applicable
E11	**SER**	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-		Not applicable

TEST GROUP F – DEFECT SCREENING TEST

AEC #	Test	Q100 reference	Test conditions	Testing temperature	Q100 sample s./ lots	Results	Note
F1	**PAT** Process Average Testing	AEC Q001	See AEC Q001				
F2	**SBA** Statistical Bin Yield Analysis	AEC Q002	See AEC Q002				

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS							
AEC #	**Test**	**Q100 reference**	**Test conditions**	**Testing temperature**	**Q100 sample s./ lots**	**Results Fails / Parts/ Lot**	**Note**
G1	**MS** Mechanical Shock	JEDEC JESD22 B104				-	Not required for surface mount devices.
G2	**VFV** Variable Frequency Vibration	JEDEC JESD22 B103				-	Not required for surface mount devices.
G3	**CA** Constant Acceleration	MIL-STD 883 Method 2001				-	Not required for surface mount devices.
G4	**GFL** Gross/Fine Leak	MIL-STD 883 Method 1014				-	Not required for surface mount devices.
G5	**DROP** Package Drop	-				-	Not required for surface mount devices.
G6	**LT** Lid Torque	MIL-STD 883 Method 2024				-	Not required for surface mount devices.
G7	**DS** Die Shear	MIL-STD 883 Method 2019				-	Not required for surface mount devices.
G8	**IWV** Internal Water Vapor	MIL-STD 883 Method 1018				-	Not required for surface mount devices.

3.3 Test description

Test name	Description	Purpose
PC (JL3) Preconditioning (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.	*As stand-alone test:* to investigate the level of moisture sensitivity. *As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failures, die-attach layer degradation.
AC Autoclave	The unbiased device is stored in a saturated steam, at fixed and controlled conditions of pressure and temperature.	This test is performed to point out critical water entry paths with consequent corrosion effects affecting die or package materials, related to chemical contamination.
ES Enviroment sequence (JL3+TC200cy+AC96h)	The unbiased device is submitted to cycled temperature excursions, between a hot and a cold chamber in air and then is stored in a saturated steam, at fixed and controlled conditions of pressure and temperature.	This test is performed to point out critical water entry paths with consequent corrosion effects affecting die or package materials, related to chemical contamination. To emphatize the failure modes linked to water entry paths, the parts have been preceeded by JL3+TC200cy
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, metal stress-voiding.

4 TEST GLOSSARY

Test name	Description
HTSL	High Temperature Storage Life test
TC	Temperature Cycling test
AC	Autoclave
ES	Environmental Sequence
PC (JL3)	Preconditioning (Jedec Level 3)
WBP	Wire Bond Pull
WBS	Wire Ball Shear

5 REVISION HISTORY

Version	Date	Pages	Author
1.0	April 11th 2014	15	M.Corradini

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