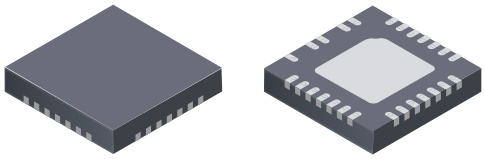
Wide Input Voltage Range, High Efficiency Fault Tolerant LED Driver

FEATURES AND BENEFITS

- Integrated 2 MHz capable boost converter with 60 V DMOS switch with OVP protection
- Sync function to synchronize boost converter switching frequencies up to 2.3 MHz
- LED current up to 40 mA per LED channel into 8 channels
- Drives up to 12 series LEDs in 8 parallel strings (V_f = 3.5 V, I_f = 40 mA), V_{IN} = 8 V, switching frequency of 1 MHz
- Single EN/PWM pin interface for PWM dimming and enable functions
- APWM pin for fine-tuning color adjustment and/or maximizing contrast ratio
- Integrated driver for optional external PMOS input disconnect switch
- Typical LED accuracy of 0.7% and 0.8% for LED-to-LED matching
- Internal bias supply for single-supply operation from 5 to 40 V
- Extensive protection features

PACKAGE: 26-PIN QFN (SUFFIX EC)



Not to scale

DESCRIPTION

The A8510 is a multi-output white LED driver for LCD backlighting. It integrates a current-mode boost converter with internal power switch and 8 current sinks. The boost converter can drive up to 96 LEDs with 12 LEDs at 40 mA per string. The LED sinks can also be paralleled together to achieve even higher LED currents, up to 320 mA. The A8510 can operate from a single power supply, from 5 to 40 V.

If required, the A8510 can drive an external P-FET to disconnect the input supply from the system in the event of a fault. The A8510 provides protection against output short and overvoltage, open or shorted diode, open or shorted LED pin, and overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects the internal current switch against high current overloads.

The A8510 has a synchronization pin that allows PWM switching frequencies to be synchronized in the range of 580 kHz to 2.3 MHz.

The device package is a 26-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

APPLICATIONS

- Industrial LCD displays
- Backlighting LCD displays
- Infotainment displays

Typical Application Diagram

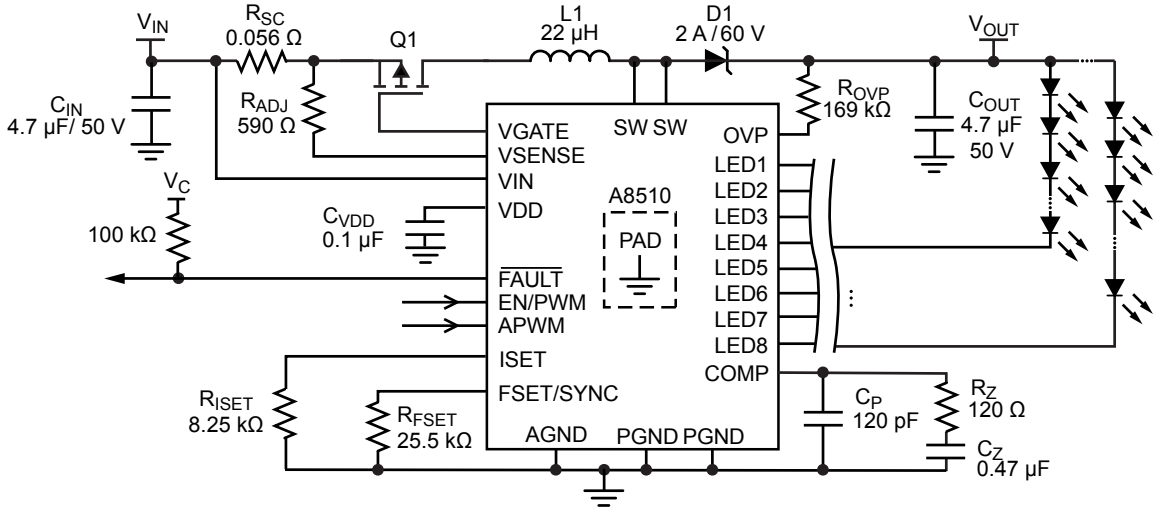


Figure 1. Typical Application Circuit showing VIN to GND short protection using P-MOSFET sensing

SELECTION GUIDE

Part Number	Packing
A8510GECTR-T	7000 pieces per 13-in. reel

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pin			–0.3 to 55	V
OVP Pin			–0.3 to 60	V
VIN, VSENSE, VGATE Pins		V_{SENSE} and V_{GATE} should not exceed V_{IN} by more than 0.4 V.	–0.3 to 40	V
SW Pin		Continuous	–0.6 to 62	V
		t < 50 ns	–1.0	V
$\overline{\text{FAULT}}$ Pin			–0.3 to 40	V
ISET, FSET/SYNC, APWM, and COMP Pins			–0.3 to 5.5	V
All other pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range G	–40 to 105	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute-Maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer, 3 in. × 3 in. PCB	48.5	°C/W

[2] Additional thermal information available on the Allegro website

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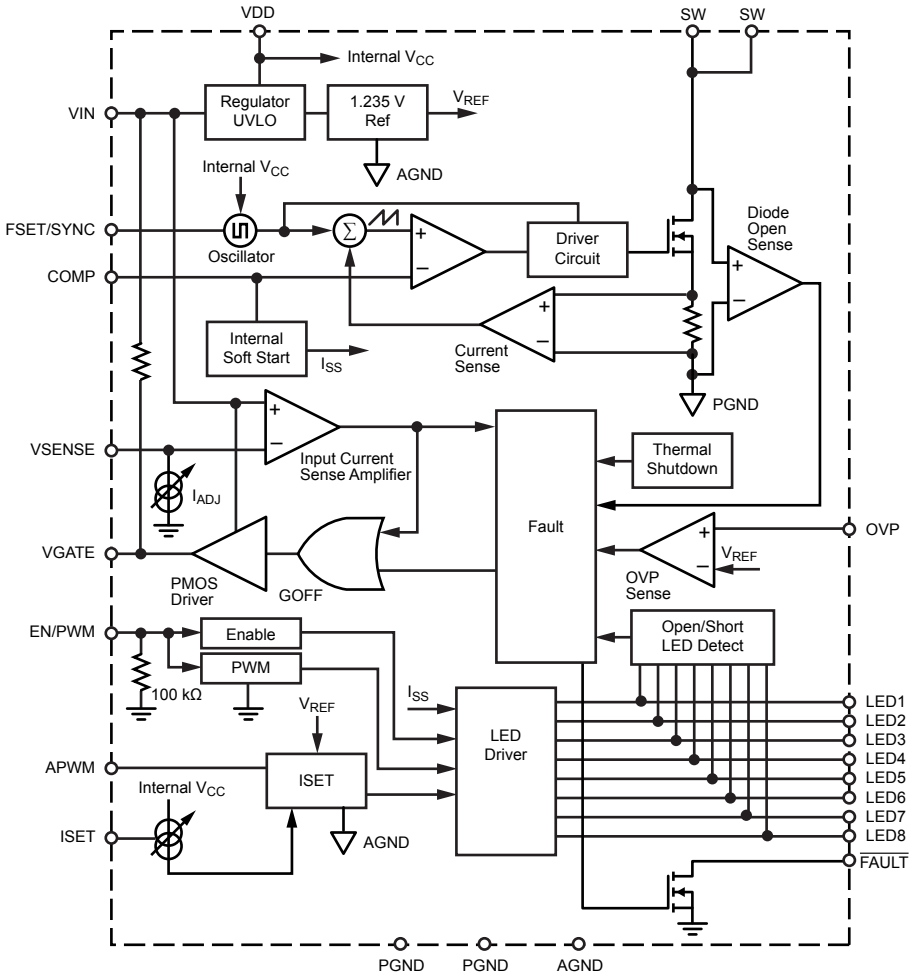
Functional Block Diagram



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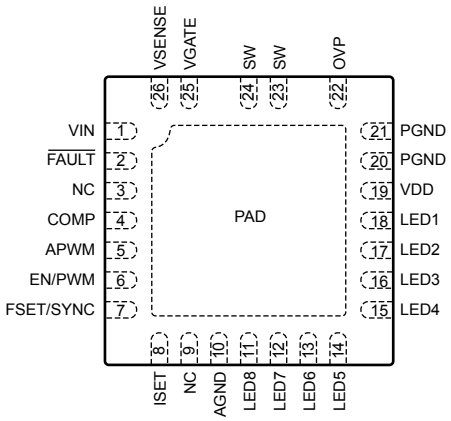
Pinout Diagram



Terminal List Table

Number	Name	Function
1	VIN	Input power to the A8510 as well as the positive input used for the current sense resistor.
2	$\overline{\text{FAULT}}$	This pin is used to indicate a fault condition, it is an open drain type configuration that will be pulled low when a fault occurs; connect a 100 kΩ resistor between this pin and the required logic level voltage.
3, 9	NC	No connect.
4	COMP	Output of the error amplifier and compensation node; connect a series $R_Z C_Z$ network from this pin to GND for control loop compensation.
5	APWM	Analog trimming option or dimming; applying a digital PWM signal to this pin adjusts the internal I_{SET} current.
6	EN/PWM	PWM dimming pin used to control the LED intensity by using pulse width modulation, with the typical PWM dimming frequency is in the range of 200 Hz to 1 kHz; also used to enable the A8510.
7	FSET/SYNC	Frequency/synchronization pin; connect a resistor R_{FSET} from this pin to GND to set the switching frequency. This pin can also be used to synchronize two or more converters in the system; the maximum synchronization frequency is 2.3 MHz.
8	ISET	Connect the R_{ISET} resistor between this pin and GND to set the LED 100% current level.
10 to 18	LED8 to LED1	Connect the cathode of each LED string to these pins.
19	VDD	Output of internal LDO; connect a 0.1 µF decoupling capacitor between this pin and GND.
20, 21	PGND	Power ground for internal NMOS device.
22	OVP	This pin is used to sense an overvoltage condition; connect the R_{OVP} resistor from V_{OUT} to this pin to adjust the Overvoltage Protection (OVP) function.
23, 24	SW	The drain of the internal NMOS switch of the boost converter.
25	VGATE	Gate driver pin for external P-MOSFET disconnect switch.
26	VSENSE	Connect this pin to the negative sense side of the current sense resistor R_{SC}; the threshold voltage is measured as $V_{IN} - V_{SENSE}$.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation; this pad must be connected to the ground plane(s) of the PCB with at least 8 thermal vias, directly in the pad.

ELECTRICAL CHARACTERISTICS [1]: Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over the full operating temperature range with $T_A = T_J$ = –40°C to 105°C, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range [3]	V_{IN}		•	5	–	40	V
UVLO Start Threshold	$V_{UVLOrise}$	V_{IN} rising	•	–	–	4.35	V
UVLO Stop Threshold	$V_{UVLOfall}$	V_{IN} falling	•	–	–	3.90	V
UVLO Hysteresis [4]	$V_{UVLOhys}$		•	–	450	–	mV
INPUT CURRENTS							
Input Quiescent Current	I_Q	EN/PWM = V_{IH}; SW = 2 MHz, no load	•	–	5.5	–	mA
Input Sleep Supply Current	I_{QSLEEP}	V_{IN} = 16 V, EN/PWM = SYNC = 0 V	•	–	2	10.0	µA
INPUT LOGIC LEVELS (EN/PWM, APWM)							
Input Logic Level-Low	V_{IL}	V_{IN} throughout operating input voltage range	•	–	–	400	mV
Input Logic Level-High	V_{IH}	V_{IN} throughout operating input voltage range	•	1.5	–	–	V
EN/PWM Pin Pin Pull-Down Resistor	R_{EN}	EN/PWM = 5 V		–	100	–	kΩ
APWM Pin Pull-Down Resistor	R_{APWM}	APWM = V_{IH}		–	100	–	kΩ
APWM							
APWM Frequency	f_{APWM}		•	20	–	1000	kHz
ERROR AMPLIFIER							
Open Loop Voltage Gain	A_{VOL}			–	48	–	dB
Transconductance	g_m	ΔI_{COMP} = ±10 µA	•	–	990	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–350	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	350	–	µA
COMP Pin Pull-Down Resistor	R_{COMP}			–	2000	–	Ω
OVERVOLTAGE PROTECTION							
Overvoltage Threshold	$V_{OVP(th)}$	OVP connected to V_{OUT}	•	7.7	8.1	8.5	V
OVP Sense Current	I_{OVPH}		•	188	199	210	µA
OVP Leakage Current	I_{OVPLKG}	R_{OVP} = 40.2 kΩ, V_{IN} = 16 V, EN/PWM = V_{IL}	•	–	0.1	1	µA
Secondary Overvoltage Protection	$V_{OVP(sec)}$		•	–	55	–	V
BOOST SWITCH							
Switch On-Resistance	R_{SW}	I_{SW} = 0.750 A, V_{IN} = 16 V		–	300	–	mΩ
Switch Leakage Current	I_{SWLKG}	V_{SW} = 16 V, EN/PWM = V_{IL}	•	–	0.1	1	µA
Switch Current Limit	$I_{SW(LIM)}$		•	3.0	3.5	4.2	A
Secondary Switch Current Limit [4]	$I_{SW(LIM2)}$	Higher than $I_{SW(LIM)}$(max) for all conditions, device latches when detected		–	7.0	–	A
Soft Start Boost Current Limit	$I_{SWSS(LIM)}$	Initial soft start current for boost switch		–	700	–	mA
Minimum Switch On-Time	$t_{SWONTIME}$			–	85	–	ns
Minimum Switch Off-Time	$t_{SWOFFTIME}$			–	47	–	ns

Continued on the next page…

ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over the full operating temperature range with $T_A = T_J$ = –40°C to 105°C, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 10 kΩ	•	1.8	2	2.2	MHz
		R_{FSET} = 20 kΩ		–	1	–	MHz
		R_{FSET} = 35.6 kΩ		–	580	–	kHz
FSET/SYNC Pin Voltage	V_{FSET}	R_{FSET} = 10 kΩ		–	1.00	–	V
FSET Frequency Range	f_{FSET}			580	–	2500	kHz
SYNCHRONIZATION							
Synchronized PWM Frequency	f_{SWSYNC}		•	580	–	2300	kHz
Synchronization Input Minimum Off-Time	$t_{PWSYNCOFF}$		•	150	–	–	ns
Synchronization Input Minimum On-Time	$t_{PWSYNCON}$		•	150	–	–	ns
SYNC Input Logic Voltage	$V_{SYNC(H)}$	FSET/SYNC pin, high level	•	2.0	–	–	V
	$V_{SYNC(L)}$	FSET/SYNC pin, low level	•	–	–	0.4	V
LED CURRENT SINKS							
LEDx Accuracy	Err_{LED}	I_{SET} = 120 µA	•	–	–	3	%
LEDx Matching	ΔLEDx	I_{SET} = 120 µA	•	–	–	3	%
LEDx Regulation Voltage	V_{LED}	V_{LED1} through V_{LED8} all equal, I_{SET} = 120 µA		–	680	–	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 120 µA	•	317	327	337	A/A
ISET Pin Voltage	V_{ISET}			–	1.003	–	V
Allowable ISET Current	I_{SET}		•	40	–	120	µA
V_{LED} Short Detect	V_{LEDSC}	While LED sinks are in regulation, sensed from LEDx pin to GND		4.6	–	–	V
Soft Start LEDx Current	I_{LEDSS}	Current through each enabled LEDx pin during soft start, I_{SET} = 120 µA		–	1.06	–	mA
Maximum PWM Dimming Until Off-Time [3]	t_{PWML}	Measured while EN/PWM = low, during dimming control and internal references are powered-on (exceeding t_{PWML} results in shutdown)		–	32750	–	f_{SW} cycles
Minimum EN/PWM On-Time	t_{PWMH}	First cycle when powering-up device	•	–	0.75	2	µs
EN/PWM High to LED-On Delay	$t_{dPWM(on)}$	Time between EN/PWM enable and LEDx current reaching 90% of maximum	•	–	0.5	1	µs
EN/PWM Low to LED-Off Delay	$t_{dPWM(off)}$	Time between EN/PWM enable going low and LEDx current reaching 10% of maximum	•	–	–	500	ns
VGATE PIN							
VGATE Pin Sink Current	I_{GSINK}	$V_{GS} = V_{IN}$		–	–104	–	µA
VGATE Pin Fault Shutdown	t_{GFAULT}			–	–	3	µs
VGATE Pin Voltage	V_{GS}	Gate to source voltage measured when gate is on		–	–6.7	–	V

Continued on the next page…

ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over the full operating temperature range with $T_A = T_J$ = –40°C to 105°C; unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ. [2]	Max.	Unit
VSENSE PIN							
VSENSE Pin Sink Current	I_{ADJ}		•	18.8	20.3	21.8	µA
VSENSE Trip Point	$V_{SENSEtrip}$	Measured between VIN and VSENSE, R_{ADJ} = 0 Ω		–	180	–	mV
$\overline{\text{FAULT}}$ PIN							
$\overline{\text{FAULT}}$ Pin Pull-Down Voltage	V_{FAULT}	I_{FAULT} = 1 mA (400 Ω)		–	–	0.5	V
$\overline{\text{FAULT}}$ Pin Leakage Current	$I_{FAULTLKG}$	V_{FAULT} = 5 V		–	–	1	µA
THERMAL PROTECTION (TSD)							
Thermal Shutdown Threshold [4]	T_{SD}	Temperature rising		–	165	–	°C
Thermal Shutdown Hysteresis [4]	T_{SDHYS}			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Typical specifications are at T_A = 25°C.
[3] Minimum V_{IN} = 5 V is only required at startup. After startup is completed, the IC is able to function down to V_{IN} = 4 V.
[4] Ensured by design and characterization, not production tested.

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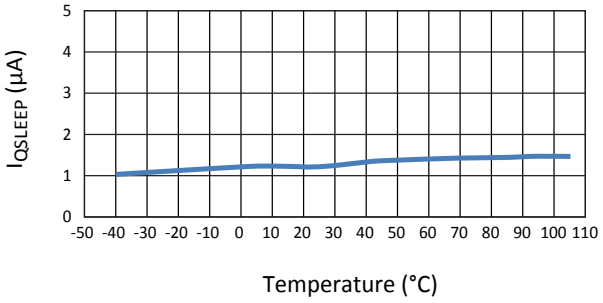
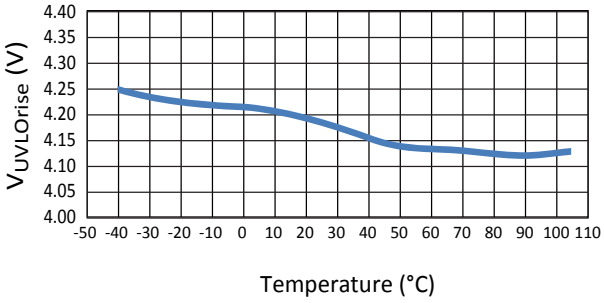
TYPICAL CHARACTERISTIC PERFORMANCE

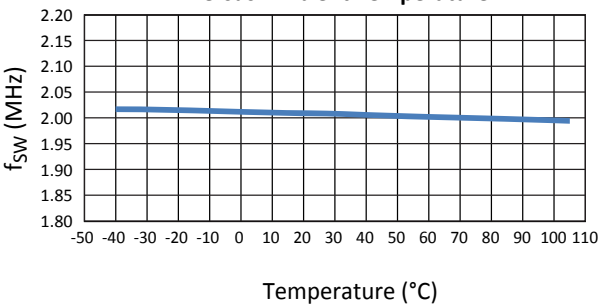
VIN Input Sleep Mode Current versus Ambient Temperature



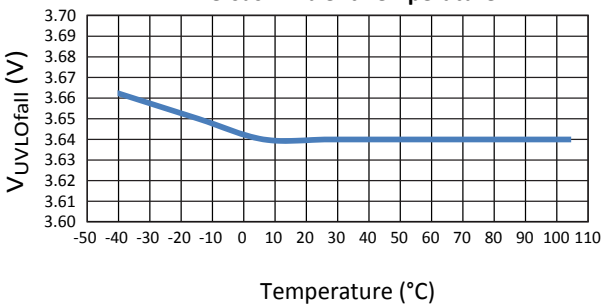
VIN UVLO Rising Threshold Voltage versus Ambient Temperature



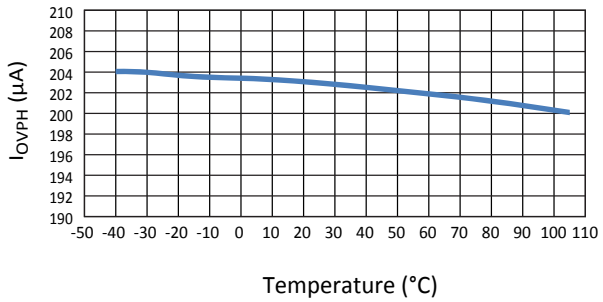
Switching Frequency versus Ambient Temperature



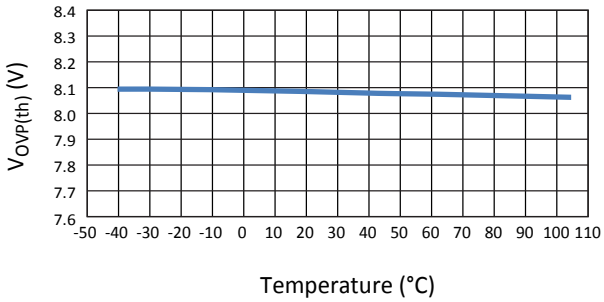
VIN UVLO Falling Threshold Voltage versus Ambient Temperature



OVP Pin Sense Current versus Ambient Temperature



OVP Pin Overvoltage Threshold versus Ambient Temperature



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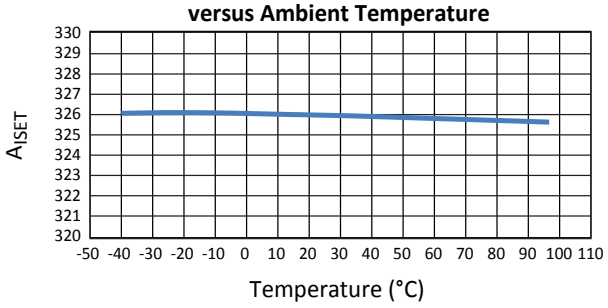
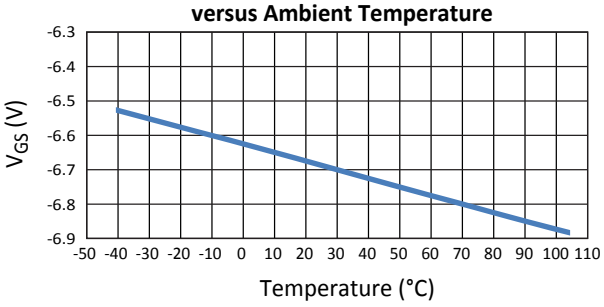
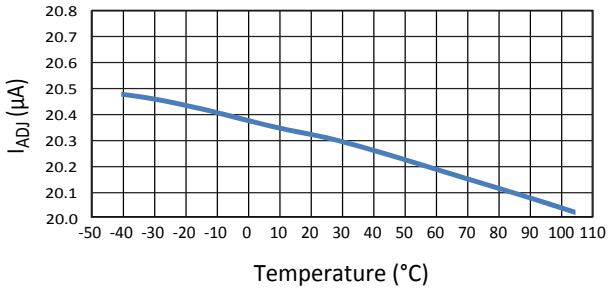
ISET to LED Current Gain versus Ambient Temperature



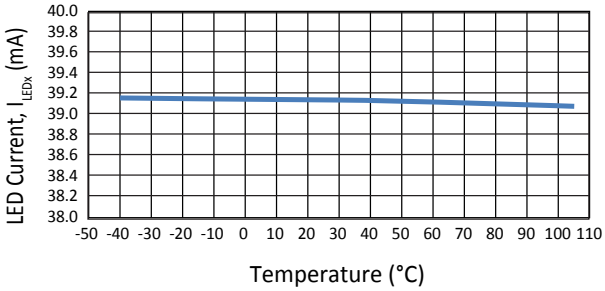
Input Disconnect Switch Gate to Source Voltage versus Ambient Temperature



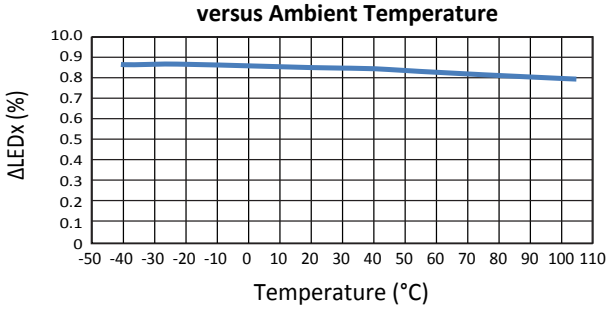
VSENSE Pin Sink Current versus Ambient Temperature



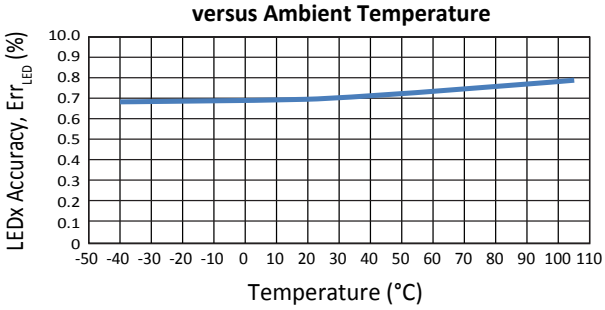
LEDx Current versus Ambient Temperature I_{SET} = 120 µA



LED to LED Matching Accuracy versus Ambient Temperature

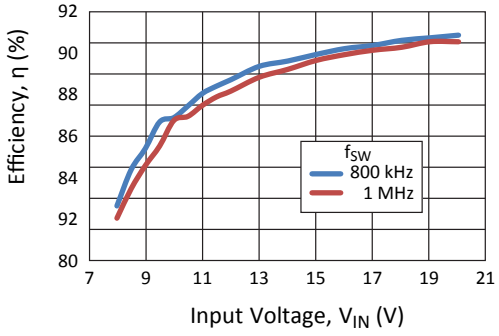


LED Set Point Accuracy versus Ambient Temperature



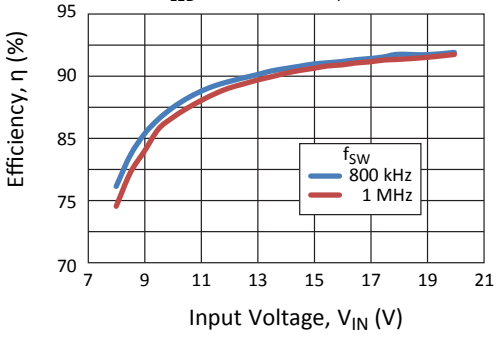
Efficiency for 10 Series LEDs per Channel

I_{LED} = 40 mA, LED V_f ≈ 3.2 V



Efficiency for 12 Series LEDs per Channel

I_{LED} = 40 mA, LED V_f ≈ 3.2 V



FUNCTIONAL DESCRIPTION

The A8510 incorporates a current-mode boost controller with internal DMOS switch, and eight LED current sinks. It can be used to drive eight LED strings of up to 12 white LEDs in series, with current up to 40 mA per string. For optimal efficiency, the output of the boost stage is adaptively adjusted to the minimum voltage required to power all of the LED strings. This is expressed by the following equation:

$$V_{OUT} = \max (V_{LED1} ,..., V_{LED8}) + V_{REG} \quad (1)$$

where

V_{LEDx} is the voltage drop across LED strings 1 through 8, and

V_{REG} is the regulation voltage of the LED current sinks (typically 0.68 V at the maximum LED current).

ENABLING THE IC

The IC turns on when a logic high signal is applied on the EN/PWM pin with a minimum duration of t_{PWMH} for the first clock cycle, and the input voltage present on the VIN pin is greater than the 4.35 V necessary to clear the UVLO ($V_{UVLOrise}$) threshold. The power-up sequence is shown in figure 2. Before the LEDs are enabled, the A8510 driver goes through a system check to determine if there are any possible fault conditions that might prevent the system from functioning correctly. Also, if the FSET/SYNC pin is pulled low, the IC will not power-up. More information on the FSET/SYNC pin can be found below, in the Synchronization section of this document.

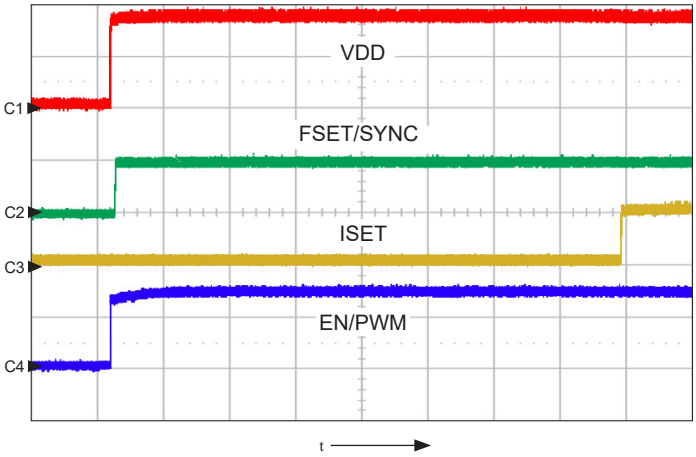


Figure 2. Power-up diagram at f_{SW} = 2 MHz; shows VDD (ch1, 2 V/div.), FSET/SYNC (ch2, 1 V/div.), ISET (ch3, 1 V/div.), and EN/PWM (ch4, 2 V/div.) pins, t = 200 µs/div.

POWERING UP: LED PIN SHORT-TO-GND CHECK

The VIN pin has a UVLO function that prevents the A8510 from powering-up until the UVLO threshold is reached. After the VIN pin goes above UVLO, and a high signal is present on the EN/PWM pin, the IC proceeds to power-up. As shown in figure 3, at this point the A8510 enables the disconnect switch and checks if any LED pins are shorted to GND and/or are not used. The LED detect phase starts when the VGATE voltage of the disconnect switch is equal to V_{IN} – 4.5 V.

After the voltage threshold on the LEDx pins exceeds 120 mV, a timer of 3000 to 4000 clock cycles is used to determine the status of the pins. Thus, the LED detection duration varies with the switching frequency, as shown in the following table:

Switching Frequency (kHz)	Detection Time (ms)
2000	1.5 to 2
1000	3 to 4
800	3.75 to 5
600	5 to 6.7

The LED pin detection voltage thresholds are as follows:

LED Pin Voltage	LED Pin Status	Action
<70 mV	Short-to-GND	Power-up is halted
150 mV	Not used	LED removed from operation
>325 mV	LED pin in use	None

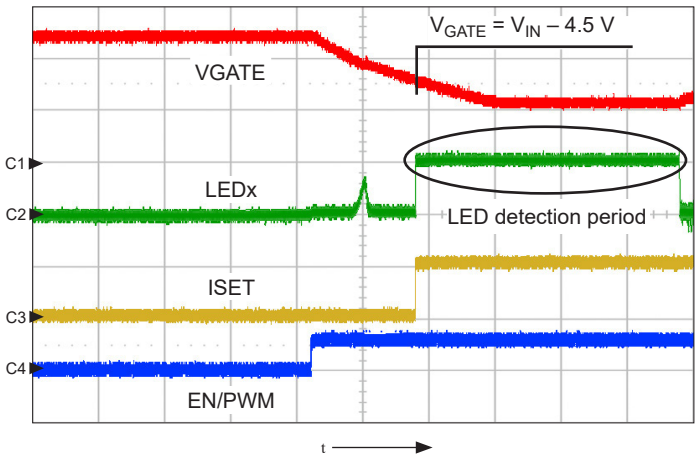


Figure 3. Power-up diagram; shows the relationship of an LEDx pin with respect to the gate voltage of the disconnect switch (if used) during the LED detect phase, as well as the duration of the LED detect phase for a switching frequency of 800 kHz; shows VGATE (ch1, 5 V/div.), LEDx (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and EN/PWM (ch4, 5 V/div.) pins, t = 1 ms/div.

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All unused pins should be connected with a 4.75 kΩ resistor to GND, as shown in figure 5. The unused pin, with the pull-down resistor, will be taken out of regulation at this point and will not contribute to the boost regulation loop.

If an LEDx pin is shorted to ground the A8510 will not proceed with soft start until the short is removed from the LEDx pin. This prevents the A8510 from powering-up and putting an uncontrolled amount of current through the LEDs. The various detect scenarios are presented in figures 4A and 4B.

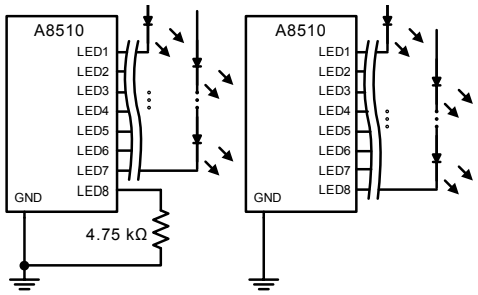
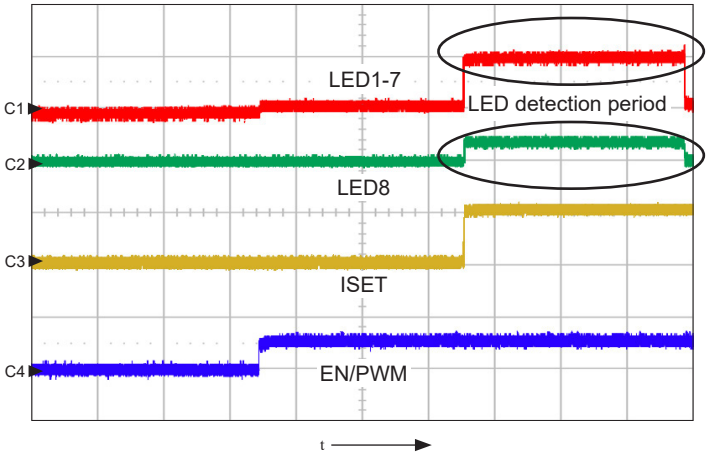
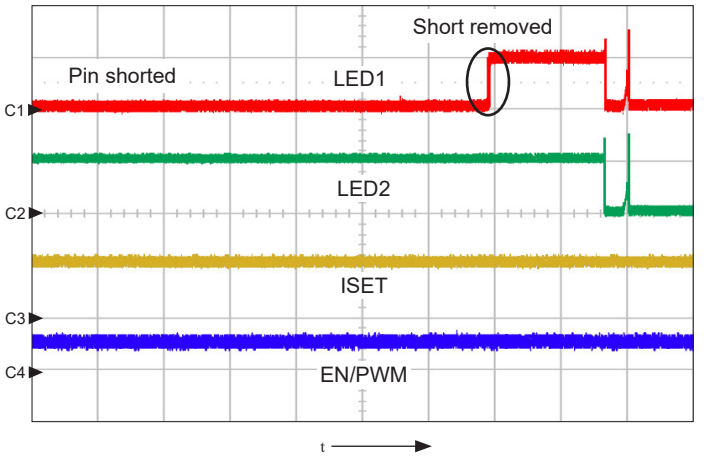


Figure 5. Channel select setup: (left) channel LED8 not used, (right) using all channels.



4A. Example with LED8 pin not being used; f_{SW} is 2 MHz, the detect voltage is about 150 mV; shows LED1-7 (ch1, 500 mV/div.), LED8 (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and EN/PWM (ch4, 5 V/div.) pins, t = 500 µs/div.



4B. Example with one LED shorted to GND. The IC will not proceed with power-up until the shorted LED pin is released, at which point the LED is checked to see if it is being used; shows LED1 (ch1, 500 mV/div.), LED2 (ch2, 500 mV/div.), ISET (ch3, 1 V/div.), and EN/PWM (ch4, 5 V/div.) pins, t = 1 ms/div.

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SOFT START FUNCTION

During soft start the LEDx pins are set to sink (I_{LEDSS}) and the boost switch current is reduced to the $I_{SWSS(LIM)}$ level to limit the inrush current generated by charging the output capacitors. When the converter senses that there is enough voltage on the LEDx pins, the converter proceeds to increase the LED current to the preset regulation current and the boost switch current limit is switched to the $I_{SW(LIM)}$ level to allow the A8510 to deliver the necessary output power to the LEDs. This is shown in figure 7.

FREQUENCY SELECTION

The switching frequency on the boost regulator is set by the resistor connected to the FSET/SYNC pin, and the switching frequency can be can be anywhere from 580 kHz to 2.3 MHz. Figure 6 shows the typical switching frequencies for given resistor values.

If during operation a fault occurs that will increase the switching frequency, the FSET/SYNC pin is clamped to a maximum switching frequency of no more than 3.5 MHz.

SYNCHRONIZATION

The A8510 can also be synchronized using an external clock on the FSET/SYNC pin. Figure 8 shows the correspondence of a SYNC signal and the SW pin, and figure 9 shows the result when a SYNC signal is detected: the LED current does not show any variation while the frequency synchronization occurs. At power-up if the FSET/SYNC pin is held low, the IC will not power-up. Only when the FSET/SYNC pin is tri-stated to allow for the pin to rise, to about 1 V, or when a sync clock is detected, will the A8510 try to power-up.

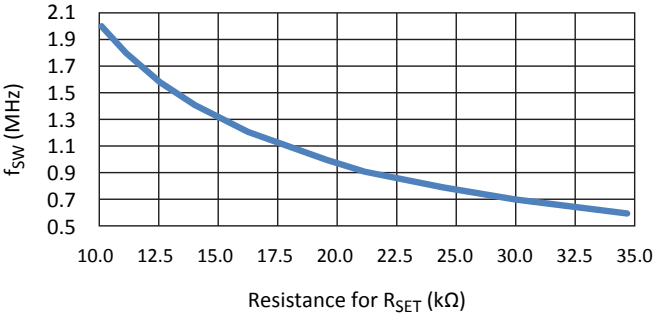

Figure 6. Typical Switching Frequency versus value of R_{FSET} resistor.

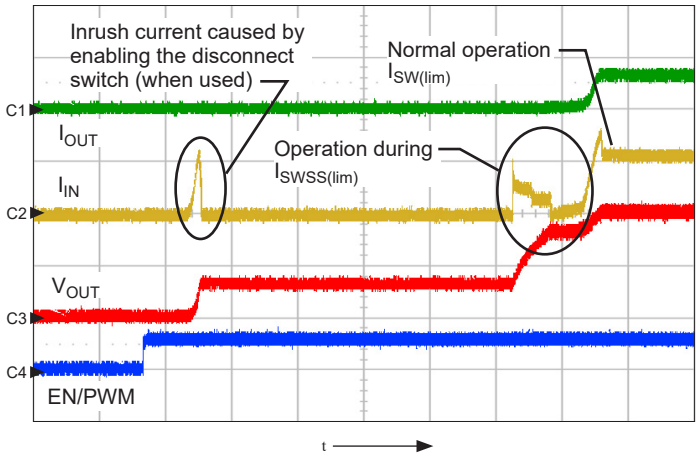

Figure 7. Startup diagram showing the input current, output voltage, and output current, f_{SW} = 800 kHz; shows I_{OUT} (ch1, 500 mA/div.), I_{IN} (ch2, 1 A/div.), V_{OUT} (ch3, 20 V/div.), and EN/PWM (ch4, 5 V/div.), t = 1 ms/div.

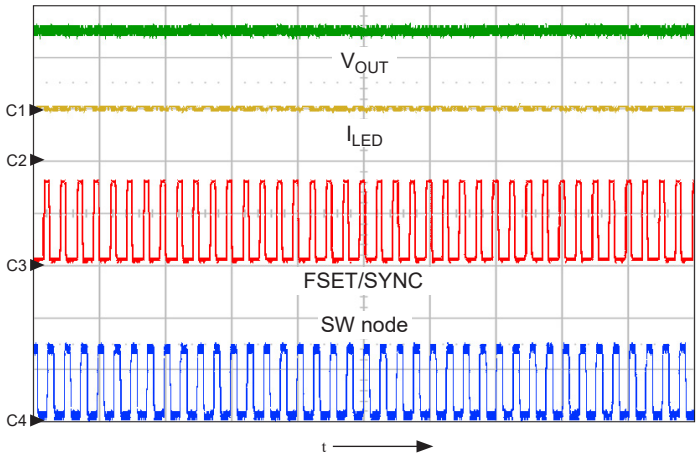

Figure 8. Diagram showing a synchronized FSET/SYNC pin and switch node; shows V_{OUT} (ch1, 20 V/div.), I_{LED} (ch2, 200 mA/div.), FSET/SYNC (ch3, 2 V/div.), and SW node (ch4, 20 V/div.), t = 2 µs/div.

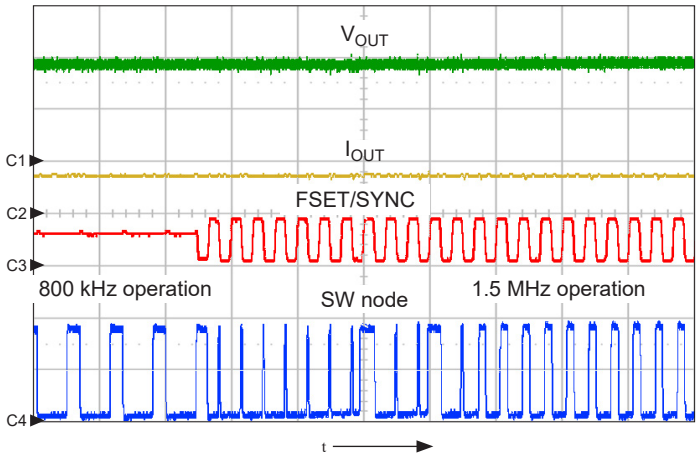

Figure 9. Transition of the SW waveform when the SYNC pulse is detected. The A8510 switching at 800 kHz, applied SYNC pulse at 1.5 MHz; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 500 mA/div.), FSET/SYNC (ch3, 2 V/div.), and SW node (ch4, 20 V/div.), t = 2 µs/div.

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The basic requirement of the SYNC signal is 150 ns minimum on-time and 150 ns minimum off time, as indicated by the specifications for $t_{PWSYNCON}$ and $t_{PWSYNCOFF}$. Figure 10 shows the timing for a synchronization clock into the A8510 at 800 kHz. Thus any pulse with a duty cycle of 12% to 88% at 800 kHz can be used to synchronize the IC.

The SYNC pulse duty cycle ranges for selected switching frequencies are:

SYNC Pulse Frequency (kHz)	Duty Cycle Range (%)
2200	33 to 66
2000	30 to 70
1000	15 to 85
800	12 to 88
600	9 to 91

If during operation a SYNC clock is lost, the IC will revert to the preset switching frequency that is set by the resistor R_{FSET}. During this period the IC will stop switching for a maximum period of about 7 µs to allow the sync detection circuitry to switch over to the externally preset switching frequency.

If the clock is held low for more than 7 µs, the A8510 will shut down. In this shutdown mode the IC will stop switching, the input disconnect switch is open, and the LEDs will stop sinking current. To shutdown the IC into low power mode, the IC must be disabled by keeping the EN/PWM pin low for a period of 32750 clock cycles. If the FSET/SYNC pin is released at any time after 7 µs, the A8510 will proceed to soft start.

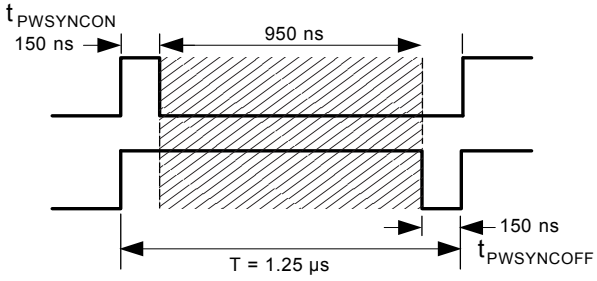

Figure 10. SYNC pulse on and off time requirements, for an 800-kHz clock.

LED CURRENT SETTING AND LED DIMMING

The maximum LED current can be up to 40 mA per channel, and is set through the ISET pin. To set the I_{LED} current, connect a resistor, R_{ISET}, between this pin and GND, according to the following formula:

$$R_{ISET} = (1.003 \times 327) / I_{LED} \quad (2)$$

where I_{LED} is in mA and R_{ISET} is in Ω. This sets the maximum current through the LEDs, referred to as the *100% current*. Standard R_{ISET} values, at gain equals 327, are as follows:

Standard Resistor Value Closest to R_{ISET} (kΩ)	LED current per LED, I_{LED} (mA)
8.25	40
10.5	30
13.0	25
16.2	20

PWM DIMMING

The LED current can be reduced from the 100% current level by PWM dimming using the EN/PWM pin. When the EN/PWM pin is pulled high, the A8510 turns on and all enabled LEDs sink 100% current. When EN/PWM is pulled low, the boost converter and LED sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active. The typical PWM dimming frequencies fall between 200 Hz and 1 kHz. Figures 12A to 12D provide examples of PWM switching behavior.

Another important feature of the A8510 is the PWM signal to LED current delay. This delay is typically less than 500 ns, which allows greater accuracy at low PWM dimming duty cycles, as shown in figure 11.

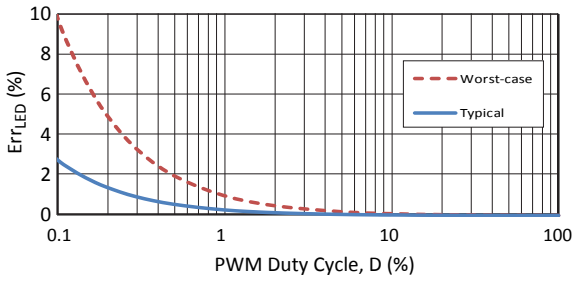

Figure 11. Percentage Error of the LED current versus PWM duty cycle (at 200 Hz PWM frequency), for 500 ns delay.

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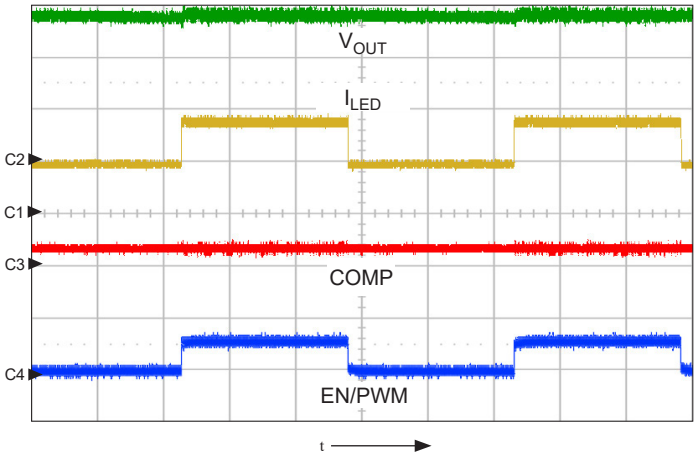

Figure 12A. Typical PWM diagram showing V_{OUT}, I_{LED}, and COMP pin as well as the PWM signal. PWM dimming frequency is 200 Hz at 50% duty cycle; shows V_{OUT} (ch1, 10 V/div.), I_{LED} (ch2, 50 mA/div.), COMP (ch3, 2 V/div.), EN/PWM (ch4, 5 V/div.), t = 1 ms/div.

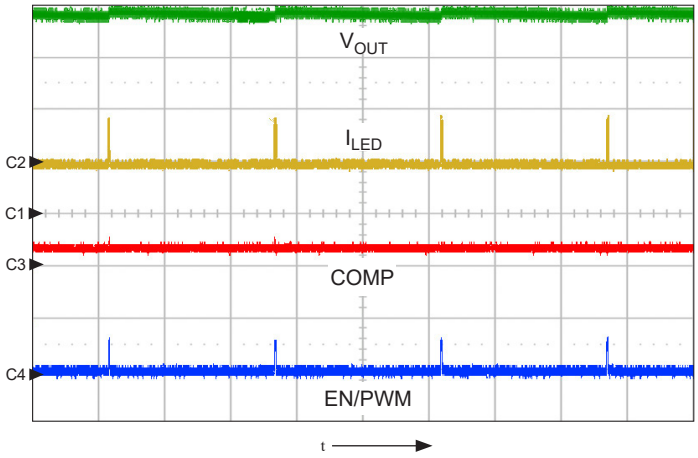

Figure 12B. Typical PWM diagram showing V_{OUT}, I_{LED}, and COMP pin as well as the PWM signal. PWM dimming frequency is 200 Hz at 1% duty cycle ; shows V_{OUT} (ch1, 10 V/div.), I_{LED} (ch2, 50 mA/div.), COMP (ch3, 2 V/div.), EN/PWM (ch4, 5 V/div.), t = 2 ms/div.

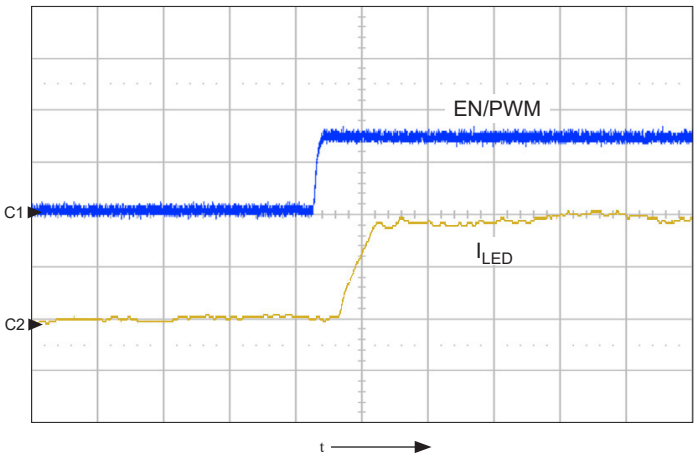

Figure 12C. Delay from rising edge of PWM signal to LED current; shows EN/PWM (ch1, 2 V/div.), and I_{LED} (ch2, 20 mA/div.), t = 200 ns/div.

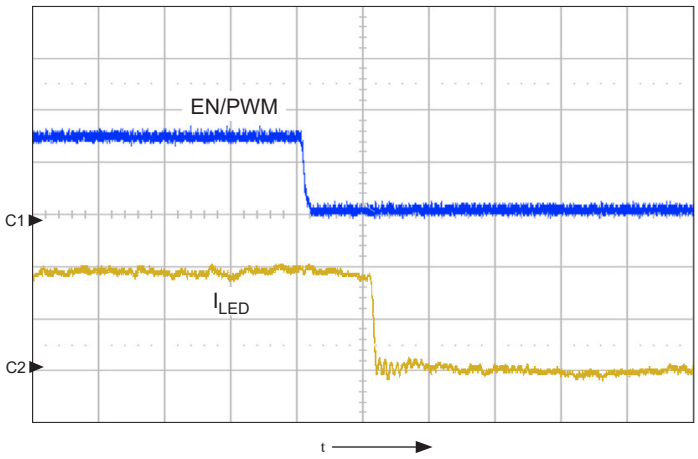

Figure 12D. Delay from falling edge of PWM signal to LED current turn off; shows EN/PWM (ch1, 2 V/div.), and I_{LED} (ch2, 50 mA/div.), t = 200 ns/div.

APWM PIN

The APWM pin is used in conjunction with the ISET pin. This is a digital signal pin that internally adjusts the ISET current. The typical input signal frequency is between 20 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current that is delivered to the LEDs (figure 14). As an example, a system that delivers a full LED current of 40 mA per LED would deliver 20 mA of current per LED when an APWM signal is applied with a duty cycle of 50%. When this pin is not used it should be tied to GND.

To use this pin for a trim function, the user should set the maximum output current to a value higher than the required current by at least 5%. The LED ISET current is then trimmed down to the

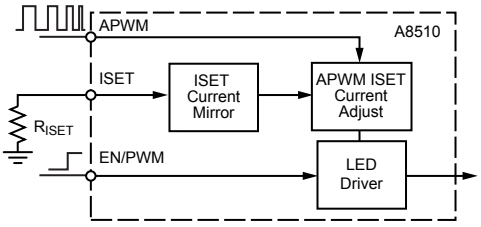

Figure 13. Simplified block diagram of the APWM ISET block.

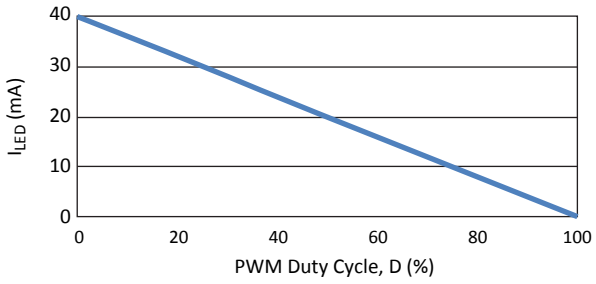

Figure 14. LED current versus PWM duty cycle; 200 kHz APWM frequency.

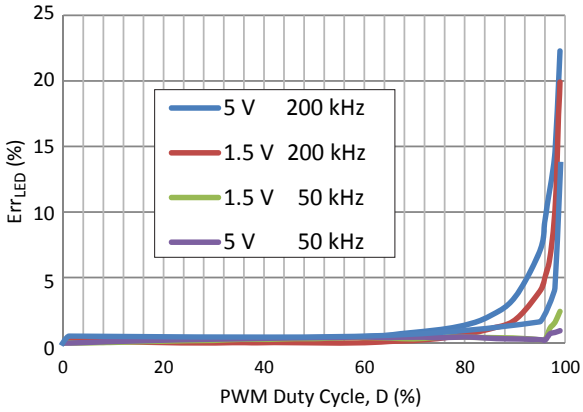

Figure 15. Percentage Error of the LED current versus APWM signals.

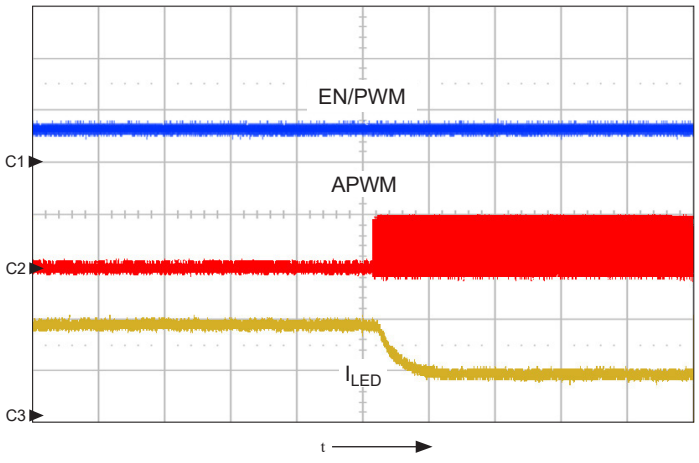

Figure 16. Diagram showing the transition of LED current from 40 mA to 20 mA, when a 50% duty cycle signal is applied to the APWM pin; EN/PWM = 1; shows EN/PWM (ch1, 5 V/div.), APWM (ch2, 5 V/div.), and I_{LED} (ch3, 20 mA/div.), t = 1 ms/div.

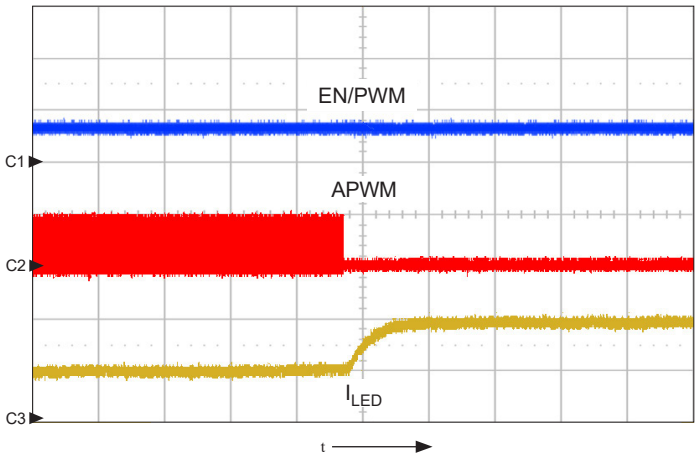

Figure 17. Diagram showing the transition of LED current from 20 mA to 40 mA, when a 50% duty cycle signal is removed from the APWM pin. EN/PWM = 1; shows EN/PWM (ch1, 5 V/div.), APWM (ch2, 5 V/div.), and I_{LED} (ch3, 20 mA/div.), t = 1 ms/div.

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appropriate value. In cases where the user-supplied APWM has significant duty cycle limitations, it might be preferable to set the maximum ISET current to be 25% to 50% higher, thus allowing the APWM signal to have duty cycles that are between 50% and 75%.

Although the APWM dimming function has a wide frequency range, if this function is used strictly as an analog dimming function it is recommended to use frequency ranges between 50 and 500 kHz for best accuracy. The frequency range must be considered only if the user is not using this function as a closed loop trim function. There is a few millisecond propagation delay between the APWM signal and I_{LED} current. This effect is shown in figures 16 through 18.

ANALOG DIMMING

The A8510 can also be dimmed by using an external DAC or another voltage source applied either directly to the ground side of the R_{ISET} resistor or through an external resistor to the ISET pin (see figure 19).

• For a single resistor (upper panel of figure 19), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET} - V_{DAC}} \quad (3)$$

Where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

When the DAC voltage is equal to V_{ISET}, the internal reference, there is no current through R_{ISET}. When the DAC voltage starts to decrease, the ISET current starts to increase, thus increasing the LED current. When the DAC voltage is 0 V, the LED current will be at its maximum.

• For a dual-resistor configuration (lower panel of figure 19), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET}}{R_{ISET}} - \frac{V_{DAC} - V_{ISET}}{R_1} \quad (4)$$

The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the R_{ISET} resistor:

- VDAC = 1.003 V; the output is strictly controlled by R_{ISET}
- VDAC > 1.003 V; the LED current is reduced
- VDAC < 1.003 V; the LED current is increased

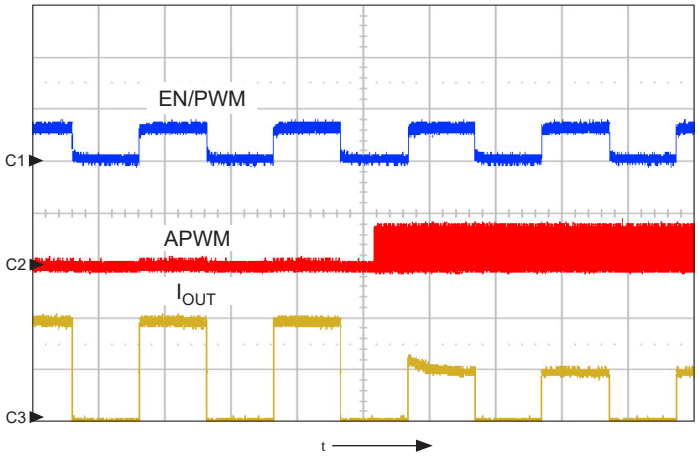

Figure 18. Transition of output current level when a 50% duty cycle signal is applied to the APWM pin, in conjunction with a 50% duty cycle PWM dimming being applied to the EN/PWM pin; shows EN/PWM (ch1, 5 V/div.), APWM (ch2, 5 V/div.), and I_{LED} (ch3, 20 mA/div.), t = 1 ms/div.

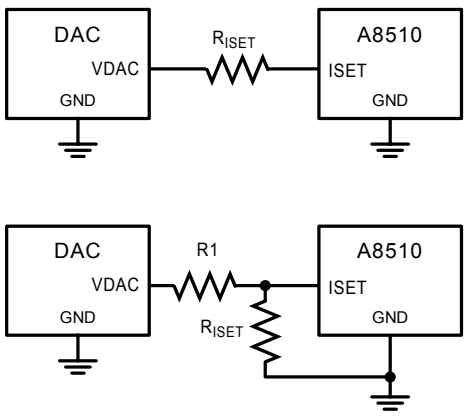

Figure 19. Simplified diagrams of voltage control of I_{LED}: typical applications using a DAC to control I_{LED} using a single resistor (upper), and dual resistors (lower).

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LED SHORT DETECT

All of the LEDx pins are capable of handling the maximum V_{OUT} that the converter can deliver, thus providing protection from the LED pin to V_{OUT} in the event of a connector short.

Any LEDx pin that has a voltage exceeding V_{LEDSC} will be removed from operation (see figure 20). This is to prevent the IC from dissipating too much power by having a large voltage present on the LEDx pin.

While the IC is being PWM-dimmed, the IC rechecks the disabled LEDx pin every time the PWM signal goes high, to prevent false tripping of an LEDx short event. This also allows some self-correction if an intermittent LEDx pin short-to-V_{OUT} is present.

OVERVOLTAGE PROTECTION

The A8510 has overvoltage protection (OVP) and open Schottky diode (D1) protection. The OVP protection has a default level of 8 V and can be increased up to 55 V by connecting R_{OVP} between the OVP pin and V_{OUT}. When the current into the OVP pin exceeds 199 µA typical, the OVP comparator goes low and the boost stops switching.

The following equation can be used to determine the resistance for setting the OVP level:

$$R_{OVP} = (V_{OUTovp} - V_{OVP(th)}) / I_{OVPH} \quad (4)$$

where:

V_{OUTovp} is the target overvoltage level,
R_{OVP} is the value of the external resistor, in Ω,
$V_{OVP(th)}$ is the pin OVP trip point found in the Electrical Characteristics table, and
I_{OVPH} is the current into the OVP pin.

There are several possibilities for why an OVP condition would be encountered during operation, the two most common being: an open LED string, and a disconnected output. Examples of these are provided in figures 21 and 22.

Figure 21 illustrates when the output of the A8510 is disconnected from load during normal operation. The output voltage instantly increases up to OVP voltage level and then the boost stops switching to prevent damage to the IC. If the output is drained off, eventually the boost might start switching for a short duration until the OVP threshold is hit again.

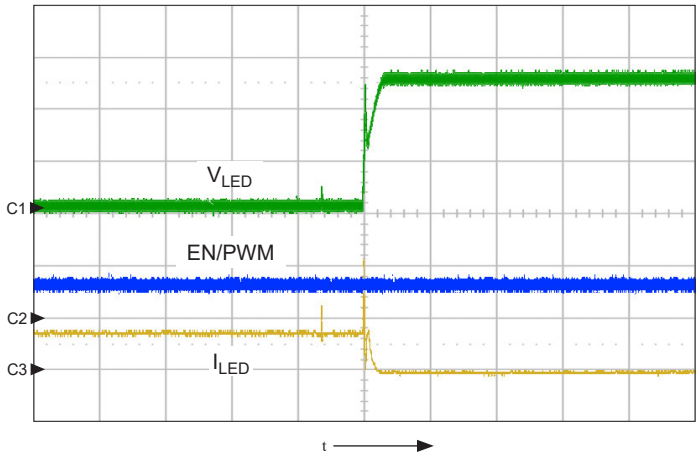

Figure 20. Example of the disabling of an LED string when the LED pin voltage is increased above 4.6 V; shows V_{LED} (ch1, 5 V/div.), EN/PWM (ch2, 5 V/div.), and I_{LED} (ch3, 50 mA/div.), t = 20 µs/div.

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Figure 22 displays a typical OVP event caused by an open LED string. After the OVP condition is detected, the boost stops switching, and the open LED string is removed from operation. Afterwards V_{OUT} is allowed to fall, and eventually the boost will resume switching and the A8510 will resume normal operation.

A8510 also has built-in secondary overvoltage protection to protect the internal switch in the event of an open diode condition. Open Schottky diode (D1) detection is implemented by detecting overvoltage on the SW pins of the device. If voltage on the SW pins exceeds the device safe operating voltage rating, the A8510 disables and remains latched. To clear this fault, the IC must be shut down either by using the PWM signal or by going below the UVLO threshold on the VIN pin. Figure 23 illustrates this. As soon as the switch node voltage (SW) exceeds $V_{OVP(sec)}$, the IC shuts down. Due to small delays in the detection circuit, as well as there being no load present, the switch node voltage will rise above the trip point voltage.

Figure 24 illustrates when the A8510 is being enabled during an open diode condition. The IC goes through all of its initial LED detection and then tries to enable the boost, at which point the open diode is detected.

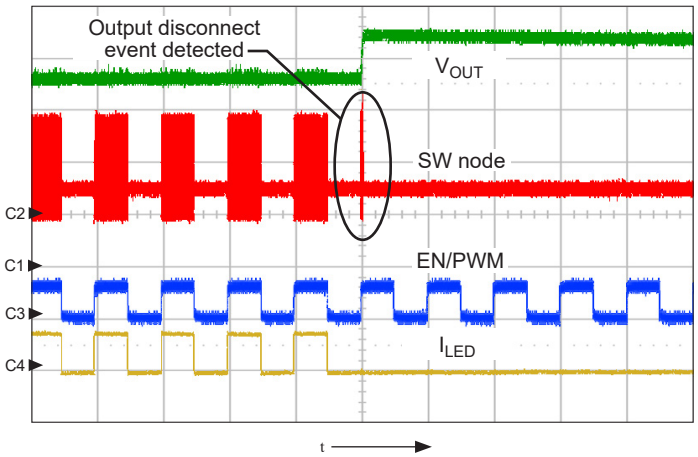

Figure 21. OVP protection in an output disconnect from load event; shows V_{OUT} (ch1, 10 V/div.), SW node (ch2, 20 V/div.), EN/PWM (ch3, 5 V/div.), and I_{LED} (ch4, 50 mA/div.), t = 2 ms/div.

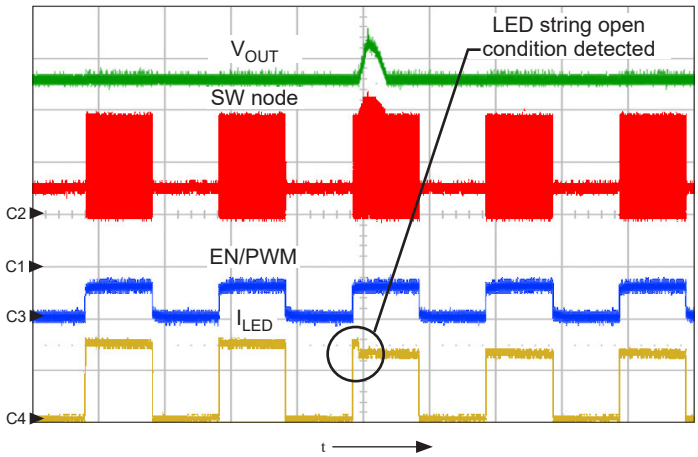

Figure 22. OVP protection in an open LED string event; shows V_{OUT} (ch1, 10 V/div.), SW node (ch2, 20 V/div.), EN/PWM (ch3, 5 V/div.), and I_{LED} (ch4, 200 mA/div.), t = 1 ms/div.

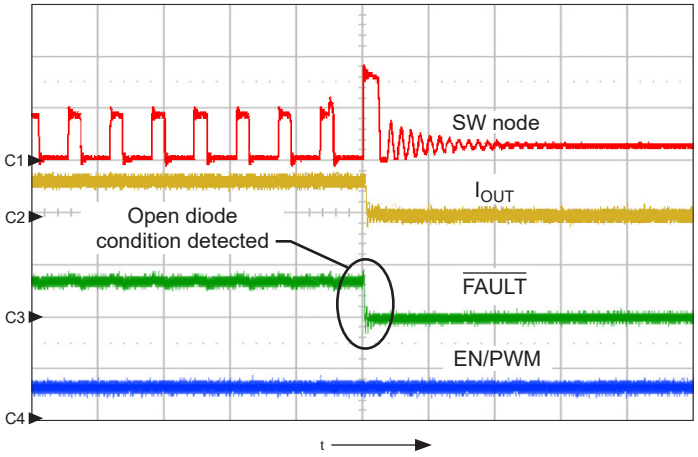

Figure 23. OVP protection in an open Schottky diode D1 event, while the IC is in normal operation; shows SW node (ch1, 50 V/div.), I_{OUT} (ch2, 500 mA/div.), $\overline{FAULT}$ (ch3, 5 V/div.), and EN/PWM (ch4, 5 V/div.), t = 2 µs/div.

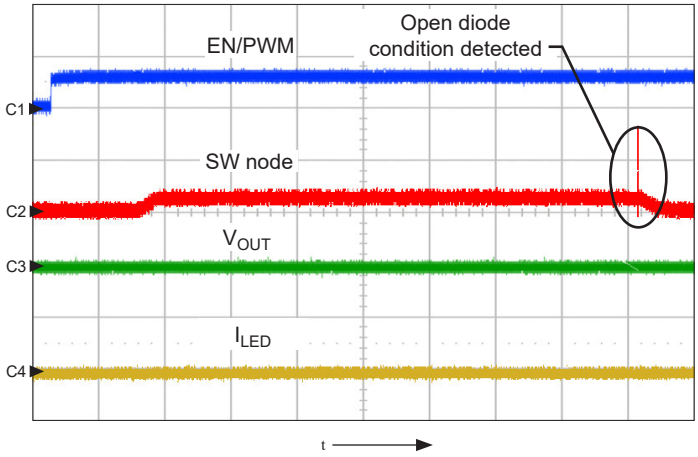

Figure 24. OVP protection when the IC is enabled during an open diode condition; shows EN/PWM (ch1, 5 V/div.), SW node (ch2, 50 V/div.), V_{OUT} (ch3, 10 V/div.), and I_{LED} (ch4, 200 mA/div.), t = 500 µs/div.

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BOOST SWITCH OVERCURRENT PROTECTION

The boost switch is protected with cycle-by-cycle current limiting set at a minimum of 3.0 A. There is also a secondary current limit that is sensed on the boost switch. When detected this current limit immediately shuts down the A8510. The level of this current limit is set above the cycle-by-cycle current limit to protect the switch from destructive currents when the boost inductor is shorted. Various boost switch overcurrent conditions are shown in figures 25 through 27.

INPUT OVERCURRENT PROTECTION AND DISCONNECT SWITCH

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition. The external circuit implementing the disconnect is shown in figure 28. If the input disconnect switch is not used, the VSENSE pin must be tied to VIN and the VGATE pin must be left open.

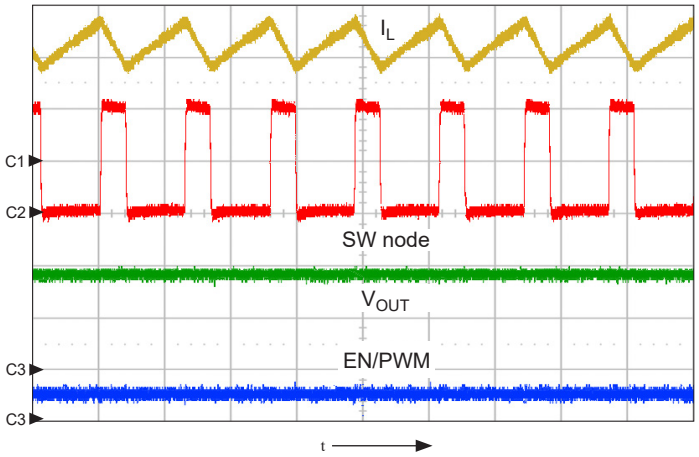

Figure 25. Normal operation of the switch node (SW); inductor current (I_L) and output voltage (V_{OUT}) for 12 series LEDs in each of 8 strings configuration; shows I_L (ch1, 500 mA/div.), SW node (ch2, 20 V/div.), V_{OUT} (ch3, 20 V/div.), and EN/PWM (ch4, 5 V/div.), t = 1 µs/div.

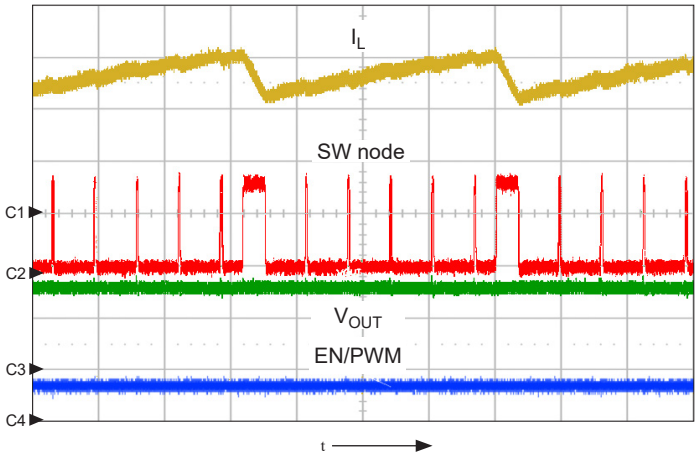

Figure 26. Cycle-by-cycle current limiting; inductor current (IL), note reduction in output voltage as compared to normal operation with the same configuration (figure 25); shows IL (ch1, 1 A/div.), SW node (ch2, 20 V/div.), VOUT (ch3, 10 V/div.), and EN/PWM (ch4, 5 V/div.), t = 2 µs/div.

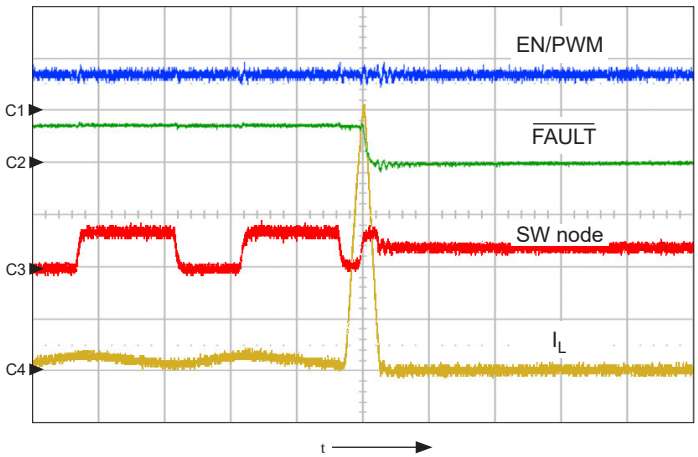

Figure 27. Secondary boost switch current limit; when this limit is hit, the A8510 immediately shuts down; shows EN/PWM (ch1, 5 V/div.), $\overline{FAULT}$ (ch2, 5 V/div.), SW node (ch3, 50 V/div.), and I_L (ch4, 2 A/div.), t = 200 ns/div.

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When selecting the external PMOS, check for the following parameters:

- Drain-source breakdown voltage $V_{(BR)DSS} > -40$ V
- Gate threshold voltage (make sure it is fully conducting at V_{GS} = -4 V, and cut-off at –1 V)
- $R_{DS(on)}$: Make sure the on-resistance is rated at V_{GS} = -4.5 V or similar, not at -10 V; derate it for higher temperature

If the input current level goes above the preset current limit threshold, the A8510 will shut down in less than 3 µs regardless of user input (figure 29). This is a latched condition. The Fault flag is also set to indicate a fault. This feature is meant to prevent catastrophic failure in the system due to a short of the inductor or output voltage to GND.

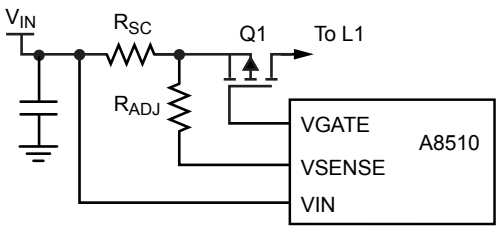

Figure 28. Typical circuit showing the implementation of the input disconnect feature.

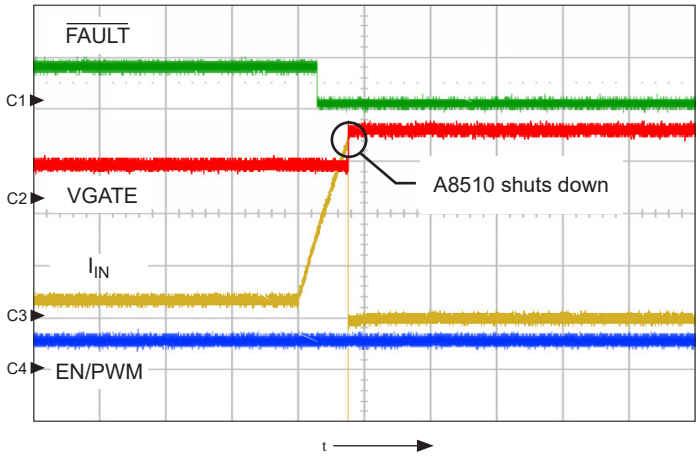

Figure 29. Diagram showing input disconnect current limit wave forms during fault condition; shows $\overline{\text{FAULT}}$ (ch1, 5 V/div.), VGATE (ch2, 10 V/div.), I_{IN} (ch3, 2 A/div.), and EN/PWM (ch4, 5 V/div.), t = 5 µs/div.

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SETTING THE CURRENT SENSE RESISTOR

The typical threshold for the current sense circuit is 180 mV, when R_{ADJ} is 0 Ω. This voltage can be trimmed by the R_{ADJ} resistor. The typical trip point should be set at about 3 A, which coincides with the cycle-by-cycle current limit minimum threshold. A sample calculation is done below:

Given: 2.85 A of input current, and the calculated maximum value of the sense resistor, R_{SC} = 0.063 Ω.

The R_{SC} chosen is 0.056 Ω, a standard value.

Also:

$$R_{ADJ} = (V_{SENSETRIP} - V_{ADJ}) / I_{ADJ} \quad (5)$$

The typical trip point voltage is calculated as:

$$V_{ADJ} = 2.85\ A \times 0.056\ \Omega = 0.160\ V$$

$$R_{ADJ} = (0.180 - 0.160\ V) / (20.3\ \mu A) = 1.0\ k\Omega$$

INPUT UVLO

When V_{IN} and V_{SENSE} rise above the UVLO enable hysteresis ($V_{UVLOrise}$ + $V_{UVLOhys}$), the A8510 is enabled. A8510 is disabled when V_{IN} falls below the $V_{UVLOfall}$ threshold for more than 50 µs. This lag is to avoid shutting down because of momentary glitches in the input power supply.

VDD

The VDD pin provides regulated bias supply for internal circuits. Connect the capacitor C_{VDD} with a value of 0.1 µF or greater to this pin.

Shutdown

If the EN/PWM pin is pulled low for more than t_{PWML}, the device enters shutdown mode and clears all internal fault registers. As an example, at a 2-MHz clock frequency, the maximum PWM low period, while avoiding shutdown, is 16 ms. In shut down, the IC disables all current sources and waits until the EN/PWM pin goes high to re-enable the IC and proceed with power-up.

FAULT PROTECTION DURING OPERATION

The A8510 constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the Fault Mode table, on the next page.

The possible fault conditions that the device can detect are: Open LED pin, LED pin shorted to GND, shorted inductor, V_{OUT} short to GND, SW pin shorted to GND, ISET pin shorted to GND, and input disconnect switch source shorted to GND.

Note the following:

- Some of the protection features might not be active during startup, to prevent false triggering of fault conditions.
- Some of these faults will not be protected if the input disconnect switch is not being used. An example of this is VOUT short to ground.

Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect switch	Sink driver
Primary switch overcurrent protection (cycle-by-cycle current limit)	Auto-restart	Always	No	This fault condition is triggered by the cycle-by-cycle current limit, ISW(LIM).	Off for a single cycle	On	On
Secondary switch current limit	Latched	Always	Yes	When the current through the boost switch exceeds secondary current SW limit ($I_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers, and boost. The Fault flag is set. To re-enable the device, the EN/PWM pin must be pulled low for 32750 clock cycles.	Off	Off	Off
Input disconnect current limit	Latched	Always	Yes	The device is immediately shut off if the voltage across the input sense resistor is above the $V_{SENSEtrip}$ threshold. The Fault flag is set. To re-enable the part the EN/PWM pin must be pulled low for 32750 clock cycles.	Off	Off	Off
Secondary OVP	Latched	Always	Yes	Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(SEC)}$ is reached. This fault latches the IC. The input disconnect switch is disabled as well as the LED drivers, and the Fault flag is set. To re-enable the part the EN/PWM pin must be pulled low for 32750 clock cycles.	Off	Off	Off
LEDx pin short protection	Auto-restart	Startup	No	This fault prevents the device from starting-up if any of the LEDx pins are shorted. The device stops soft-start from starting while any of the LED pins are determined to be shorted. Once the short is removed, soft-start is allowed to start.	Off	On	Off
LEDx pin open	Auto-restart	Normal Operation	No	When an LEDx pin is open the device will determine which LEDx pin is open by increasing the output voltage until OVP is reached. Any LED string not in regulation will be turned off. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	On	On	Off for open pins. On for all others.
ISET short protection	Auto-restart	Always	No	This fault occurs when the ISET current goes above 150% of the maximum current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed the IC will try to regulate to the preset LED current.	Off	On	Off

Continued on the next page…

Fault Mode Table (continued)

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	Sink driver
FSET/SYNC short protection	Auto-restart	Always	Yes	Fault occurs when the FSET/SYNC current goes above 150% of maximum current. The boost will stop switching, the disconnect switch will turn off and the IC will disable the LEDx sinks until the fault is removed. When the fault is removed the IC will try to restart with soft-start.	Off	Off	Off
Overvoltage protection	Auto-restart	Always	No	Fault occurs when OVP pin exceeds $V_{OVP(th)}$ threshold. The A8510 will immediately stop switching to try to reduce the output voltage. If the output voltage decreases then the A8510 will restart switching to regulate the output voltage.	Stop during OVP event.	On	On
LED short protection	Auto-restart	Always	No	Fault occurs when the LEDx pin voltage exceeds 5.1 V. When the LED short protection is detected the LED string above the threshold will be removed from operation.	On	On	Off for shorted pins. On for all others.
Overtemperature protection	Auto-restart	Always	No	Fault occurs when the die temperature exceeds the overtemperature threshold, typically 165°C.	Off	Off	Off
VIN UVLO	Auto-restart	Always	No	Fault occurs when V_{IN} drops below V_{UVLO}, typically 3.90 V. This fault resets all latched faults.	Off	Off	Off

APPLICATIONS INFORMATION

Design Example for Boost Configuration

This section provides a method for selecting component values when designing an application using the A8510. An example schematic is provided in figure 30.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 10 to 14 V
- Quantity of LED channels, $\#_{CHANNELS}$: 8
- Quantity of series LEDs per channel, $\#_{SERIESLEDS}$: 12
- LED current per channel, I_{LED}: 40 mA
- V_f at 40 mA: 3.2 V
- f_{SW}: 800 kHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% Duty cycle

Procedure: The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence. It should be noted that in many calculations the minimum and/or maximum specification values are used to guarantee proper system operation.

Step 1: Connect LEDs to pins LED1 through LED8.

Step 2: Determining the LED current setting resistor R_{ISET}:

$$R_{ISET} = 1.003 \times 327 / I_{LED} \quad (6)$$
$$= 327.981 / 40\ mA = 8.20\ k\Omega$$

Choose a 8.25 kΩ resistor.

Step 3: Determining the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter.

Step 3a: The first step is determining the maximum voltage based on the LED requirements. Then this value and the regulation voltage (V_{LED}) should be added together, as well as another 750 mV to take noise and output ripple into consideration. The regulation voltage, V_{LED}, of the A8510 is 680 mV.

$$V_{OUT(OVP)} = \#_{SERIESLEDS} \times V_f + V_{LED} + 2 \quad (7)$$
$$= 12 \times 3.2\ V + 0.680\ V + 2\ V$$
$$= 41.08\ V$$

Then the OVP resistor is:

$$R_{OVP} = (V_{OUT(OVP)} - V_{OVP(th)}) / I_{OVPH} \quad (8)$$
$$= (41.08\ V - 8.1\ V) / 199\ \mu A = 165.73\ k\Omega$$

where both I_{OVPH} and $V_{OVP(th)}$ are taken from the Electrical Characteristics table.

Chose a value of resistor that is higher value than the calculated R_{OVP}. In this case a value of 169 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor:

$$V_{OUT(OVP)} = 169\ k\Omega \times 199\ \mu A + 8.1\ V = 41.7\ V$$

Step 3b: At this point a quick check must be done to see if the conversion ratio is acceptable for the selected frequency.

$$D_{maxofboost} = 1 - t_{SWOFFTIME} \times f_{SW} \quad (9)$$
$$= 1 - 1.5 \times 47\ ns \times 800\ kHz = 94.36\%$$

where minimum off time ($t_{SWOFFTIME}$) is found in the Electrical Characteristics table.

The Theoretical Maximum V_{OUT} is then calculated as:

$$V_{OUTthe}(max) = \frac{V_{IN}(min)}{1 - D_{maxofboost}} - V_d \quad (10)$$

$$= \frac{10\ V}{1 - 0.9436} - 0.4 = 177\ V$$

where V_d is the diode forward voltage.

The Theoretical Maximum V_{OUT} value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, the switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirements.

Step 4: Selecting the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system must operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determining the duty cycle, calculated as follows:

$$D(\text{max}) = 1 - \frac{V_{IN}(\text{min})}{V_{OUT(OVP)} + V_d} \quad (11)$$

$$= 1 - \frac{10\ \text{V}}{41.7\ \text{V} + 0.4\ \text{V}} = 76.3\%$$

The voltage drop of the diode can be approximated to be about 0.4 V.

Step 4b: Determining the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor. First, the maximum input current, given:

$$I_{OUT} = \#_{CHANNELS} \times I_{LED} \quad (12)$$

$$= 8 \times 0.040\ \text{A} = 0.320\ \text{A}$$

then:

$$I_{IN}(\text{max}) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\text{min}) \times \eta} \quad (13)$$

$$= \frac{41.7\ \text{V} \times 0.320\ \text{A}}{10\ \text{V} \times 0.9} = 1.483\ \text{A}$$

where η is efficiency.

Next, calculate minimum input current, as follows:

$$I_{IN}(\text{min}) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\text{max}) \times \eta} \quad (14)$$

$$= \frac{41.7\ \text{V} \times 0.320\ \text{A}}{14\ \text{V} \times 0.9} = 1.059\ \text{A}$$

A good approximation of efficiency, η, can be taken from the efficiency curves located in the diode datasheet. A value of 90% is a good starting approximation.

Step 4c: Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor must be set such that the ½ inductor ripple current is not greater than the average minimum input current. A first past assumes I_{ripple} to be 30% of the maximum inductor current:

$$\Delta I_L = I_{IN}(\text{max}) \times 0.3 \quad (15)$$

$$= 1.48\ \text{A} \times 0.3 = 0.444\ \text{A}$$

Then:

$$L = \frac{V_{IN}(\text{min})}{\Delta I_L \times f_{SW}} \times D(\text{max}) \quad (16)$$

$$= \frac{10\ \text{V}}{0.444\ \text{A} \times 800\ \text{kHz}} \times 0.76 = 21.4\ \mu\text{H}$$

Step 4d: Double-check to make sure the ½ current ripple is less than $I_{IN}(\text{min})$:

$$I_{IN}(\text{min}) > {}^1/_2\ \Delta I_L \quad (17)$$

$$1.059\ \text{A} > 0.222\ \text{A}$$

A good inductor value to use would be 22 µH, L_{used}.

Step 4e: This step is used to verify that there is sufficient slope compensation for the inductor chosen. The slope compensation value is determined by the following formula:

$$\text{Slope Compensation} = \frac{4.5 \times f_{SW}}{2 \times 10^6} = 1.8\ \text{A}/\mu\text{s} \quad (18)$$

Next insert the inductor value used in the design:

$$\Delta I_{Lused} = \frac{V_{IN}(\text{min}) \times D(\text{max})}{L_{used} \times f_{SW}} \quad (19)$$

$$= \frac{10\ \text{V} \times 0.763}{22\ \mu\text{H} \times 800\ \text{kHz}} = 0.434\ \text{A}$$

Calculate the minimum required slope:

$$\text{Required Slope (min)} = \frac{\Delta I_{Lused} \times 1 \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D(\text{max}))} \quad (20)$$

$$= \frac{0.434\ \text{A} \times 1 \times 10^{-6}}{\frac{1}{800\ \text{kHz}} \times (1 - 0.763)} = 1.46\ \text{A}/\mu\text{s}$$

If the minimum required slope is larger than the calculated slope compensation, the inductor value must be increased.

Note: that the slope compensation value is in A/µs, and 1×10^{-6} is a constant multiplier.

Step 4f: Determining the inductor current rating. The inductor current rating must be greater than the $I_{IN}(\text{max})$ value plus the ripple current ΔI_L, or about 1.7 A, calculated as follows:

$$I_L(\text{min}) = I_{IN}(\text{max}) + {}^1/_2\ \Delta I_{Lused} \quad (21)$$

$$= 1.483\ \text{A} + 0.217\ \text{A} = 1.70\ \text{A}$$

Step 5: Determining the resistor value for a particular switching frequency. Use the R_{FSET} values shown in figure 6. For example, a 25.5 kΩ resistor will result in an 800 kHz switching frequency.

Step 6: Choosing the proper switching diode. The switching diode must be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are: current rating of the diode and reverse voltage rating.

The reverse voltage rating should be such that during operation condition, the voltage rating of the device is larger than the maximum output voltage. In this case it is $V_{OUT(OVP)}$.

The peak current through the diode is calculated as:

$$I_{dp} = I_{IN}(\max) + {}^{1}/_{2}\,\Delta I_{Lused} \quad (22)$$
$$= 1.483\text{ A} + 0.217\text{ A} = 1.70\text{ A}$$

The third major component in deciding the switching diode is the reverse current, I_R, characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding off of the output voltage, due to leakage currents. I_R can be a large contributor, especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA.

Step 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor are PWM dimming frequency and PWM duty cycle. Another major contributor is leakage current (I_{LK}). This current is the combination of the OVP leakage current as well as the reverse current of the switching diode. In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically the voltage variation on the output (V_{COUT}) during PWM dimming must be less than 250 mV, so that no audible hum can be heard. The capacitance can be calculated as follows:

$$C_{OUT} = I_{LK} \times \frac{1 - D(\min)}{f_{PWM(dimming)} \times V_{COUT}} \quad (23)$$
$$= 200\ \mu\text{A} \times \frac{1 - 0.01}{200\text{ Hz} \times 0.250\text{ V}} = 3.96\ \mu\text{F}$$

A capacitor larger than 3.96 µF should be selected due to degradation of capacitance at high voltages on the capacitor. A ceramic 4.7 µF 50 V capacitor is a good choice to fulfill this requirement.

Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

The rms current through the capacitor is given by:

$$I_{COUT}\text{rms} = I_{OUT} \sqrt{\frac{D(\max) + \frac{\Delta I_{Lused}}{I_{IN}(\max) \times 12}}{1 - D(\max)}} \quad (24)$$
$$= 0.320\text{ A} \sqrt{\frac{0.763 + \frac{0.434\text{ A}}{1.48\text{ A} \times 12}}{1 - 0.763}} = 0.583\text{ A}$$

The output capacitor must have a current rating of at least 583 mA. The capacitors selected in this design have a combined rms current rating of 3 A.

Step 8: Selecting input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple ΔV_{IN} to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (25)$$
$$= \frac{0.434\text{ A}}{8 \times 800\text{ kHz} \times 0.1\text{ V}} = 0.68\ \mu\text{F}$$

The rms current through the capacitor is given by:

$$I_{IN}\text{rms} = \frac{I_{OUT} \times \frac{\Delta I_{Lused}}{I_{IN}(\max)}}{(1 - D(\max))\sqrt{12}} \quad (26)$$
$$= \frac{0.320\text{ A} \times \frac{0.434\text{ A}}{1.48\text{ A}}}{(1 - 0.763)\sqrt{12}} = 0.11\text{ A}$$

A good ceramic input capacitor with ratings of 2.2 µF 50V or 4.7 µF 50 V will suffice for this application.

Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

Step 9: Choosing the input disconnect switch components. Set the input disconnect current limit to 3 A by choosing a corresponding sense resistor. The calculated maximum value of the sense resistor is:

$$R_{SC}(\max) = V_{SENSEtrip} / 3.0\ A \quad (27)$$
$$= 0.180\ V / 3.0\ A = 0.060\ \Omega$$

The R_{SC} chosen is 0.056 Ω, a standard value.

The trip point voltage must be:

$$V_{ADJ} = 3.0\ A \times 0.056\ \Omega = 0.168\ V$$

$$R_{ADJ} = (V_{SENSEtrip} - V_{ADJ}) / I_{ADJ} \quad (28)$$
$$= (0.180\ V - 0.168\ V) / 20.3\ \mu A = 591\ \Omega$$

A value of 590 Ω was chosen for this design.

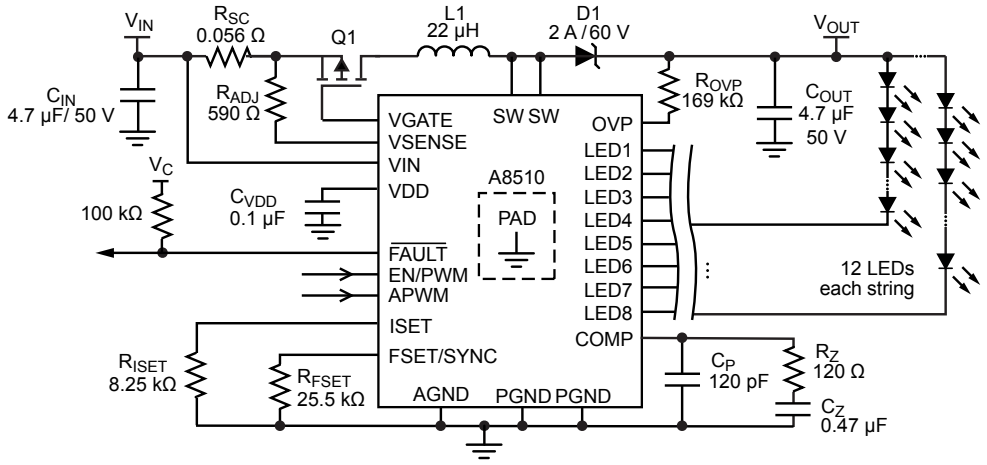

Figure 30. The schematic diagram showing calculated values from the design example above

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Design Example for SEPIC Configuration

This section provides a method for selecting component values when designing an application using the A8510 in SEPIC (Single-Ended Primary-Inductor Converter) circuit. SEPIC topology has the advantage that it can generate a positive output voltage either higher or lower than the input voltage. The resulting design is diagrammed in figure 31.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 6 to 14 V (V_{IN}(min): 5 V and V_{IN}(max): 16 V)
- Quantity of LED channels, $\#_{CHANNELS}$: 8
- Quantity of series LEDs per channel, $\#_{SERIESLEDS}$: 4
- LED current per channel, I_{LED}: 40 mA
- LED V_f at 60 mA: ≈ 3.3 V
- f_{SW}: 800 kHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% duty cycle

Procedure: The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence.

Step 1: Connecting LEDs to LEDx pins. If only some of the LED channels are needed, the unused LEDx pins should be pulled to ground using a 1.5 kΩ resistor.

Step 2: Determining the LED current setting resistor R_{ISET}:

$$R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED} \quad (29)$$
$$= (1.003\ (V) \times 327) / 0.40\ (A) = 8.20\ k\Omega$$

Choose an 8.25 kΩ 1% resistor.

Step 3: Determining the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter.

Step 3a: The first step is determining the maximum voltage based on the LED requirements. The regulation voltage, V_{LED}, of the A8510 is 720 mV. A constant term, 2 V, is added to give margin to the design due to noise and output voltage ripple.

$$V_{OUT(OVP)} = \#_{SERIESLEDS} \times V_f + V_{LED} + 2\ (V) \quad (30)$$
$$= 4 \times 3.3\ (V) + 0.680\ (V) + 2\ (V) = 15.9\ V$$

Then the OVP resistor is:

$$R_{OVP} = (V_{OUT(OVP)} - V_{OVP(th)}) / I_{OVPH} \quad (31)$$
$$= (15.9\ (V) - 8.1\ (V)) / 0.199\ (mA) = 39.196\ k\Omega$$

where both I_{OVPH} and $V_{OVP(th)}$ are taken from the Electrical Characteristics table.

In this case a value of 39.2 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor:

$$V_{OUT(OVP)} = 39.2\ (k\Omega) \times 0.199\ (mA) + 8.1\ (V) = 15.9\ V$$

Step 3b: At this point a quick check must be done to determine if the conversion ratio is acceptable for the selected frequency.

$$D_{max} = 1 - t_{SWOFFTIME} \times f_{SW} \quad (32)$$
$$= 1 - 1.5 \times 47\ (ns) \times 800\ (kHz) = 94.4\%$$

where the minimum off-time ($t_{SWOFFTIME}$) is found in the Electrical Characteristics table.

The Theoretical Maximum V_{OUT} is then calculated as:

$$V_{OUT}(max) = V_{IN}(min) \times \frac{D_{max}}{1 - D_{max}} - V_d \quad (33)$$
$$= 5\ (V) \times \frac{0.94}{1 - 0.94} - 0.4\ (V) = 77.9\ V$$

where V_d is the diode forward voltage.

The Theoretical Maximum V_{OUT} value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, it may be necessary to reduce the frequency to allow the boost to convert the voltage ratios.

Step 4: Selecting the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applica-

tions, due to stringent EMI requirements, the system must operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determining the duty cycle, calculated as follows:

$$D(\max) = \frac{V_{OUT(OVP)} + V_d}{V_{IN}(\min) + V_{OUT(OVP)} + V_d} \quad (34)$$

$$= \frac{15.9\ (V) + 0.4\ (V)}{5\ (V) + 15.9\ (V) + 0.4\ (V)} = 76.5\%$$

Step 4b: Determining the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor. First, the maximum input current, given:

$$I_{OUT} = \#_{CHANNELS} \times I_{LED} \quad (35)$$

$$= 8 \times 40\ (mA) = 0.320\ A$$

then:

$$I_{IN}(\max) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\min) \times \eta} \quad (36)$$

$$= \frac{15.9\ (V) \times 0.32\ (A)}{5\ (V) \times 0.90} = 1.131\ A$$

where η is efficiency.

Next, calculate minimum input current, as follows:

$$I_{IN}(\min) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\max) \times \eta} \quad (37)$$

$$= \frac{15.9\ (V) \times 0.32\ (A)}{16\ (V) \times 0.90} = 0.353\ A$$

Step 4c: Determining the inductor value. To ensure that the inductor operates in continuous conduction mode, the value of the inductor must be set such that the ½ inductor ripple current is not greater than the average minimum input current. As a first pass assume I_{ripple} to be 30% of the maximum inductor current:

$$\Delta I_L = I_{IN}(\max) \times I_{ripple} \quad (38)$$

$$= 1.131 \times 0.30 = 0.339\ A$$

then:

$$L = \frac{V_{IN}(\min)}{\Delta I_L \times f_{SW}} \times D(\max) \quad (39)$$

$$= \frac{5\ (V)}{0.339\ (A) \times 800\ (kHz)} \times 0.765 = 14.1\ \mu H$$

Step 4d: Double-check to make sure the ½ current ripple is less than $I_{IN}(\min)$:

$$I_{IN}(\min) > {}^1/_2\ \Delta I_L \quad (40)$$

$$0.353\ A > 0.170\ A$$

A good inductor value to use would be 15 µH.

Step 4e: Next insert the inductor value used in the design to determine the actual inductor ripple current:

$$\Delta I_{Lused} = \frac{V_{IN}(\min) \times D(\max)}{L_{used} \times f_{SW}} \quad (41)$$

$$= \frac{5\ (V) \times 0.765}{15\ (\mu H) \times 800\ (kHz)} = 0.319\ A$$

Step 4f: Determining the inductor current rating. The inductor current rating must be greater than the $I_{IN}(\max)$ value plus half of the ripple current ΔI_L, calculated as follows:

$$L(\min) = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} \quad (42)$$

$$= 1.131\ (A) + 0.160\ (A) = 1.291\ A$$

Step 5: Determining the resistor value for a particular switching frequency. Use the R_{FSET} values shown in figure 6. For example, a 25.5 kΩ resistor will result in an 800 kHz switching frequency.

Step 6: Choosing the proper switching diode. The switching diode must be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are: current rating of the diode and reverse voltage rating.

The reverse breakdown voltage rating for the output diode in a SEPIC circuit should be:

$$V_{BD} > V_{OUT(OVP)}(\max) + V_{IN}(\max) \quad (43)$$
$$> 15.9\ (V) + 16\ (V) = 31.9\ V$$

because the maximum output voltage in this case is $V_{OUT(OVP)}$.

The peak current through the diode is calculated as:

$$I_{dp} = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} \quad (44)$$
$$= 1.131\ (A) + 0.160\ (A) = 1.291\ A$$

The third major component in deciding the switching diode is the reverse current, I_R , characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding off of the output voltage, due to leakage currents. I_R can be a large contributor, especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA. It is often advantageous to pick a diode with a much higher breakdown voltage, just to reduce the reverse current. Therefore for this example, pick a diode rated for a V_{BD} of 60 V, instead of just 40 V.

Step 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor are: PWM dimming frequency and PWM duty cycle. Another major contributor is leakage current, I_{LK}. This current is the combination of the OVP leakage current as well as the reverse current of the switching diode. In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically, the voltage variation on the output, V_{COUT}, during PWM dimming must be less than 250 mV, so that no audible hum can be heard. The capacitance can be calculated as follows:

$$C_{OUT} = I_{LK} \times \frac{1 - D(\min)}{f_{PWM(dimming)} \times V_{COUT}} \quad (45)$$
$$= 200\ (\mu A) \times \frac{1 - 0.01}{200\ (Hz) \times 0.250\ (V)} = 3.96\ \mu F$$

A capacitor larger than 3.96 µF should be selected due to degradation of capacitance at high voltages on the capacitor. Select a 4.7 µF capacitor for this application.

The rms current through the capacitor is given by:

$$I_{COUT}\text{rms} = I_{OUT} \sqrt{\frac{D(\max)}{1 - D(\max)}} \quad (46)$$
$$= 0.320\ (A) \sqrt{\frac{0.765}{1 - 0.765}} = 0.577\ A$$

The output capacitor must have a ripple current rating of at least 600 mA. The capacitor selected for this design is a 4.7 µF 50 V capacitor with a 1.5 A current rating.

Step 8: Selecting input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A estimation rule is to set the input voltage ripple, ΔV_{IN}, to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (47)$$
$$= \frac{0.319\ (A)}{8 \times 800\ (kHz) \times 0.05\ (V)} = 1.00\ \mu F$$

The rms current through the capacitor is given by:

$$C_{IN}\text{rms} = \frac{\Delta I_{Lused}}{\sqrt{12}} \quad (48)$$
$$= \frac{0.319\ (A)}{\sqrt{12}} = 0.092\ A$$

A good ceramic input capacitor with a rating of 2.2 µF 25 V will suffice for this application.

Step 9: Selecting coupling capacitor C_{SW}. The minimum capacitance of C_{SW} is related to the maximum voltage ripple allowed across it:

$$C_{SW} = \frac{I_{OUT} \times D_{MAX}}{\Delta V_{SW} \times f_{SW}} \quad (49)$$

$$= \frac{0.32\ (A) \times 0.765}{0.1\ (V) \times 800\ (kHz)} = 0.627\ \mu F$$

The rms current requirement of the coupling capacitor is given by:

$$I_{CSW}rms = I_{IN}(max)\sqrt{\frac{1 - D(max)}{D(max)}} \quad (50)$$

$$= 1.131\ (A)\sqrt{\frac{1 - 0.765}{0.765}} = 0.627\ A$$

The voltage rating of the coupling capacitor must be greater than V_{IN}(max), or 16 V in this case. A ceramic capacitor rated for 2.2 µF 25 V will suffice for this application.

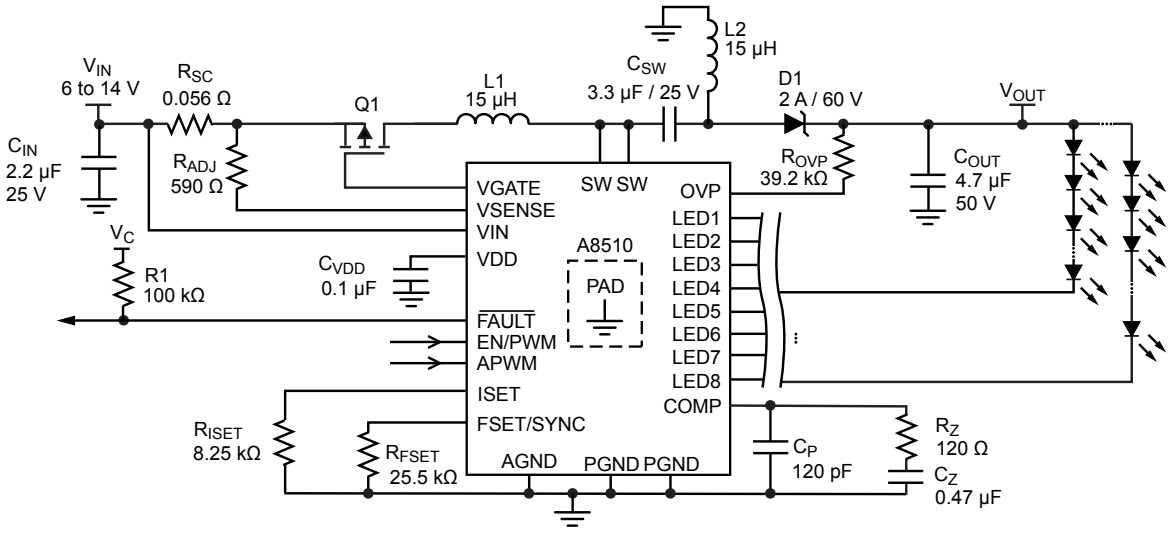
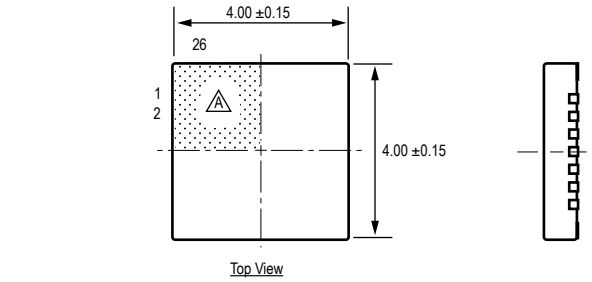
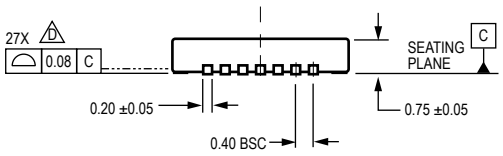


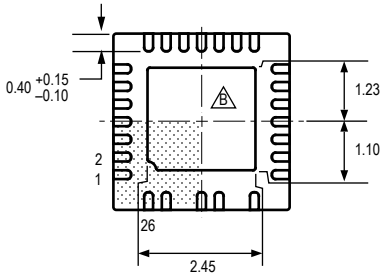
Figure 31. Typical application showing SEPIC configuration, with accurate input current sense, and VSENSE to GND protection.

Package EC, 26-Pin QFN with Exposed Thermal Pad

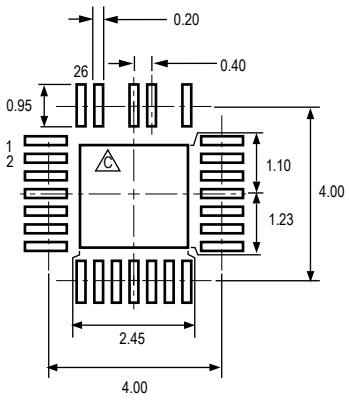


Top View





Bottom View



PCB Layout Reference View

For Reference Only
(reference JEDEC MO-220WGGE)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN40P400X400X80-29M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Number	Date	Description
2	December 15, 2011	Update to application examples, add V_{SYNC}
3	March 1, 2017	Corrected SYNC Input Logic Voltage values on page 6
4	February 11, 2019	Minor editorial updates

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