SAM G51G / SAM G51N

Atmel | SMART ARM-based Flash MCU

SUMMARY DATASHEET

Description

The Atmel® | SMART™ SAM G51 series is a member of a family of Flash microcontrollers based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor with Floating Point Unit. It operates at a maximum speed of 48 MHz and features up to 256 Kbytes of Flash and up to 64 Kbytes of SRAM. The peripheral set includes one USART, two UARTs, two I^2C-bus interfaces (TWI), one high-speed TWI, up to two SPIs, one three-channel general-purpose 16-bit timer (TC), one RTT and one 8-channel 12-bit ADC.

The Atmel | SMART SAM G51 devices have two software-selectable low-power modes: Sleep and Wait. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped.

The Event System allows peripherals to receive, react to and send events in Active and Sleep modes without processor intervention.

A general-purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set, the SAM G51 series sustains a wide range of applications including consumer, industrial control, and PC peripherals.

The device operates from 1.7V to 2.0V and is available in a 49-ball WLCSP package and a 100-lead LQFP package.

Features

- Core
  - ARM Cortex-M4 up to 48 MHz
  - Memory Protection Unit (MPU)
  - DSP Instructions
  - Floating Point Unit (FPU)
  - Thumb®-2 instruction set
- Memories
  - 256 Kbytes embedded Flash
  - 64 Kbytes embedded SRAM
- System
  - Embedded voltage regulator for single-supply operation
  - Power-on reset (POR) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz power with failure detection and 32.768 kHz for RTT or device clock
  - High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment
  - Slow clock internal RC oscillator as permanent low-power mode device clock
  - PLL range from 24 MHz to 48 MHz for device clock
  - Up to 18 Peripheral DMA Controller (PDC) channels
  - Eight 32-bit General-Purpose Backup Registers (GPBR)
  - 16 external interrupt lines
- Power consumption in active mode
  - 103 µA/MHz running Fibonacci on SRAM
- Low-power modes (typical value)
  - Wait mode 6.8 µA
  - Wake-up time from wait mode to active mode: 3.2 µs
- Peripherals
  - One USART with SPI Mode
  - Two 2-wire UARTs
  - Three Two-Wire Interface (TWI) modules featuring two fast mode TWI masters and one high-speed TWI slave
  - One fast SPI at up to 24 Mbit/s
  - One three-channel 16-bit Timer/Counter (TC) with capture, waveform, compare and PWM modes
  - One 32-bit Real-time Timer (RTT)
  - One Real-time Clock (RTC)
- I/Os
  - Up to 38 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination. Individually Programmable Open-drain, Pull-up and pull-down resistor and Synchronous Output
  - Two up to 25-bit PIO Controllers
- Analog
  - One 8-channel 12-bit ADC, up to 600 ksps

- Package
  - 49-ball WLCSP
  - 100-lead LQFP
- Industrial operating temperature range (-40 °C to +85 °C)

1. Configuration Summary

Table 1-1 summarizes the SAM G51 device configurations.

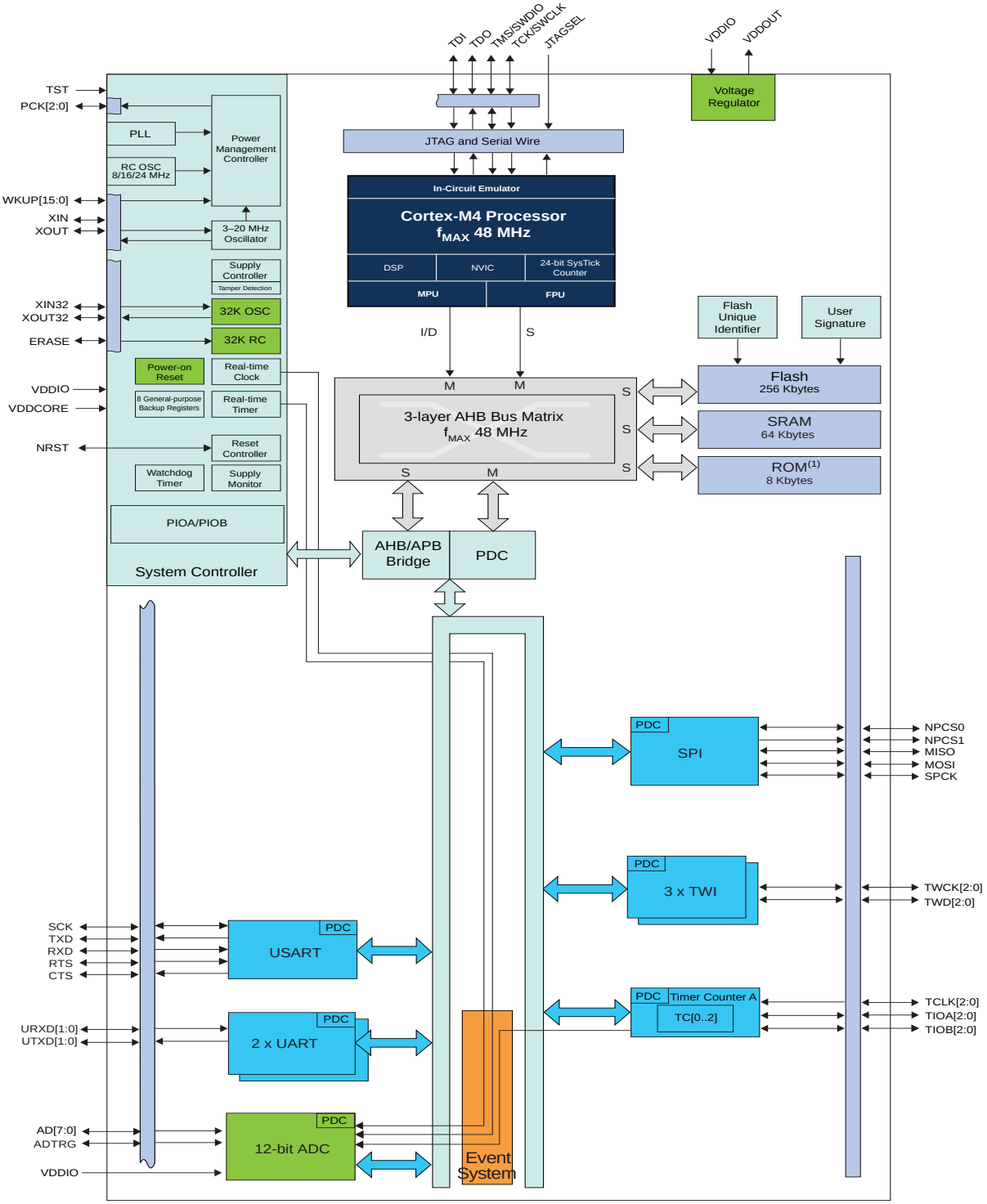
Table 1-1. Configuration Summary

Feature	SAM G51G18	SAM G51N18
Flash	256 Kbytes	256 Kbytes
SRAM	64 Kbytes	64 Kbytes
Package	WLCSP49	LQFP100
Number of PIOs	38	38
Event System	Yes	Yes
12-bit ADC	8 channels Performance: 600 ksps at 10-bit resolution 150 ksps at 11-bit resolution 37 ksps at 12-bit resolution	8 channels Performance: 600 ksps at 10-bit resolution 150 ksps at 11-bit resolution 37 ksps at 12-bit resolution
16-bit Timer	3 channels	3 channels
PDC Channels	18	18
USART/UART	1/2	1/2
SPI	2(1)	2(1)
TWI	2 masters 400 Kbit/s and 1 slave 3.4 Mbit/s	2 masters 400 Kbit/s and 1 slave 3.4 Mbit/s

Note: 1. One with SPI module + one USART configured in SPI mode.

2. SAM G51 Block Diagram

Figure 2-1. SAM G51 Block Diagram



Note: 1. The ROM is reserved for future use.

3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines, Voltage Regulator, ADC Power Supply	Power	–	–	1.7V to 2.0V
VDDOUT	Voltage Regulator Output	Power	–	–	
VDDCORE	Core Chip Power Supply	Power	–	–	Connected externally to VDDOUT
GND	Ground	Ground	–	–	
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	Reset state: - PIO input - Internal pull-up disabled - Schmitt Trigger enabled
XOUT	Main Oscillator Output	Output	–	–	
XIN32	Slow Clock Oscillator Input	Input	–	VDDIO	
XOUT32	Slow Clock Oscillator Output	Output	–		
PCK0–PCK2	Programmable Clock Output	Output	–	–	Reset state: - PIO input - Internal pull-up enabled - Schmitt Trigger enabled
ICE and JTAG					
TCK	Test Clock	Input	–	VDDIO	No pull-up resistor
TDI	Test Data In	Input	–	VDDIO	No pull-up resistor
TDO	Test Data Out	Output	–	VDDIO	
TRACESWO	Trace Asynchronous Data Out	Output	–	VDDIO	
SWDIO	Serial Wire Input/Output	I/O	–	VDDIO	
SWCLK	Serial Wire Clock	Input	–	VDDIO	
TMS	Test Mode Select	Input	–	VDDIO	No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDIO	Pull-down resistor
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down (15 kΩ) resistor
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
TST	Test Mode Select	Input	–	VDDIO	Pull-down resistor
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input	–	–	
UTXDx	UART Transmit Data	Output	–	–	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PIO Controller - PIOA - PIOB					
PA0–PA24	Parallel I/O Controller A	I/O	–	VDDIO	Pulled-up input at reset
PB0–PB12	Parallel I/O Controller B	I/O	–	VDDIO	Pulled-up input at reset
Wake-up Pins					
WKUP0–15	Wake-up Pin / External Interrupt	I/O	–	VDDIO	Wake-up pins are used also as External Interrupt
Universal Synchronous Asynchronous Receiver Transmitter - USART					
SCK	USART Serial Clock	I/O	–	–	
TXD	USART Transmit Data	I/O	–	–	
RXD	USART Receive Data	Input	–	–	
RTS	USART Request To Send	Output	–	–	
CTS	USART Clear To Send	Input	–	–	
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input	–	–	
TIOAx	TC Channel x I/O Line A	I/O	–	–	
TIOBx	TC Channel x I/O Line B	I/O	–	–	
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O	–	–	
MOSI	Master Out Slave In	I/O	–	–	
SPCK	SPI Serial Clock	I/O	–	–	High Speed Pad
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	
NPCS1	SPI Peripheral Chip Select 1	Output	Low	–	
Two-Wire Interface - TWIx					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	High Speed Pad for TWD0
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	High Speed Pad for TWDCK0
12-bit Analog-to-Digital Converter - ADC					
AD0–AD7	Analog Inputs	Analog	–	–	
ADTRG	ADC Trigger	Input	–	–	

4. Package and Pinout

Table 4-1. SAM G51 Packages

Device	Package
SAM G51G18	WLCSP49
SAM G51N18	LQFP100

4.1 49-ball WLCSP Pinout

Table 4-2. SAM G51G18 49-ball WLCSP Pinout

A1	PA9	B6	NRST	D4	PB10	F2	PA19/AD2
A2	GND	B7	PB12	D5	PA1	F3	PA17/AD0
A3	PA24	C1	VDDCORE	D6	PA5	F4	PA21
A4	PB8/XOUT	C2	PA11	D7	VDDCORE	F5	PA23
A5	PB9/XIN	C3	PA12	E1	PB2/AD6	F6	PA16
A6	PB4	C4	PB6	E2	PB0/AD4	F7	PA8/XOUT32
A7	VDDIO	C5	PA4	E3	PA18/AD1	G1	VDDIO
B1	PB11	C6	PA3	E4	PA14	G2	VDDOUT
B2	PB5	C7	PA0	E5	PA10	G3	GND
B3	PB7	D1	PA13	E6	TST	G4	VDDIO
B4	PA2	D2	PB3/AD7	E7	PA7/XIN32	G5	PA22
B5	JTAGSEL	D3	PB1/AD5	F1	PA20/AD3	G6	PA15
–	–	–	–	–	–	G7	PA6

4.2 100-lead LQFP Pinout

Table 4-3. SAM G51N18 100-lead Pinout

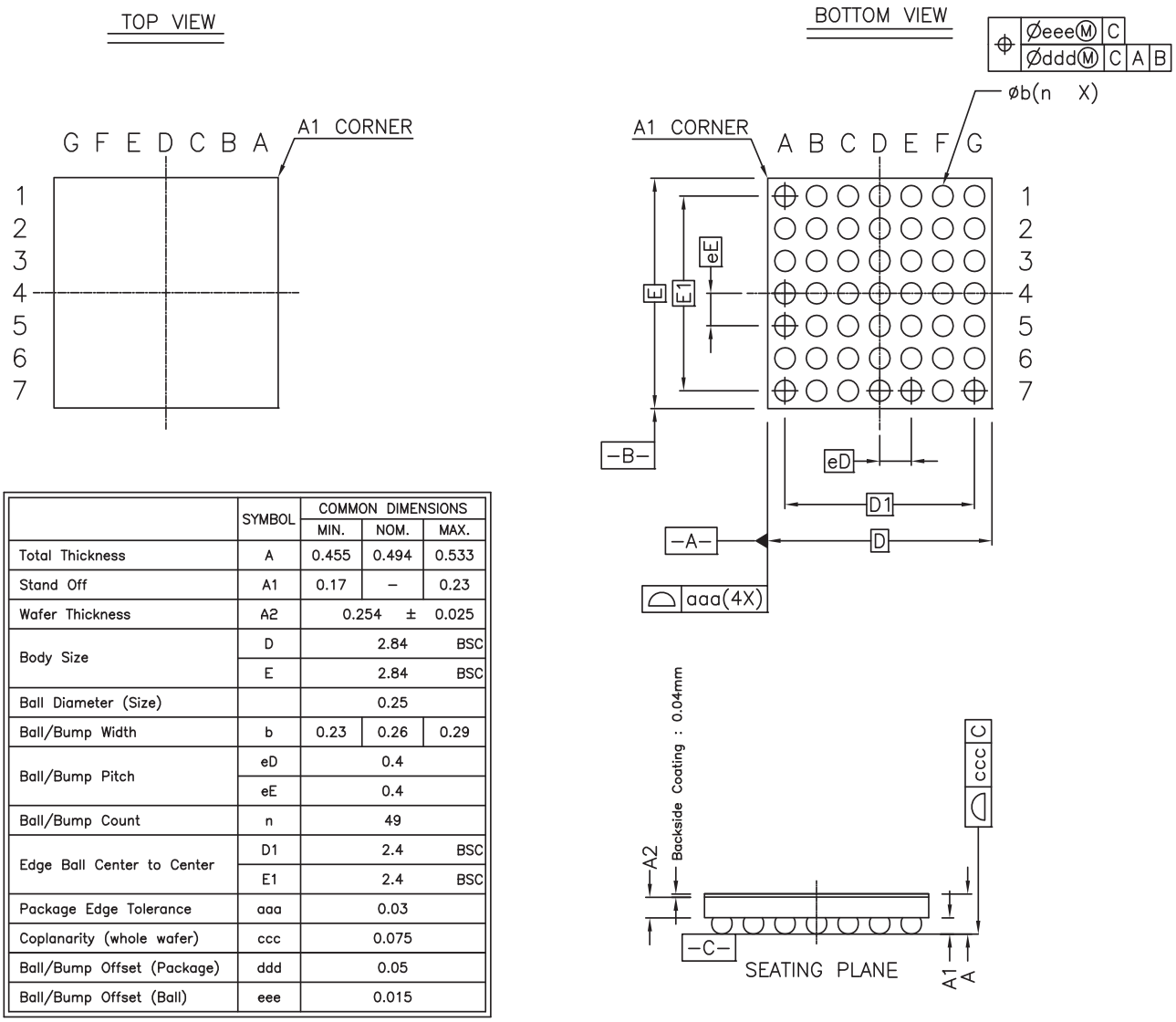
1	NC	26	NC	51	NC	76	NC
2	NC	27	NC	52	NC	77	NC
3	NC	28	PA6	53	PA17	78	NC
4	NC	29	VDDIO	54	PA18	79	PA9
5	VDDIO	30	PA16	55	PA19	80	PB5
6	VDDIO	31	PA15	56	PA20	81	GND
7	NRST	32	PA23	57	PB0	82	GND
8	PB12	33	NC	58	PB1	83	GND
9	PA4	34	NC	59	PB2	84	PB6
10	PA3	35	PA22	60	PB3	85	PB7
11	PA0	36	PA21	61	VDDIO	86	PA24
12	PA1	37	VDDIO	62	PA14	87	PB8
13	PA5	38	VDDIO	63	PA13	88	PB9
14	VDDIO	39	GND	64	PA12	89	VDDIO
15	VDDCORE	40	GND	65	PA11	90	PA2
16	VDDCORE	41	GND	66	VDDCORE	91	PB4
17	TEST	42	GND	67	VDDCORE	92	PB4
18	PA7	43	GND	68	PB10	93	JTAGSEL
19	PA8	44	VDDOUT	69	PB11	94	VDDIO
20	GND	45	VDDOUT	70	GND	95	VDDIO
21	NC	46	VDDIO	71	GND	96	NC
22	NC	47	VDDIO	72	PA10	97	NC
23	NC	48	VDDIO	73	NC	98	NC
24	NC	49	NC	74	NC	99	NC
25	NC	50	NC	75	NC	100	NC

Note: NC = Not connected

5. SAM G51 Mechanical Characteristics

5.1 49-lead WLCSP Package

Figure 5-1. 49-lead WLCSP Package Mechanical Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.455	0.494	0.533
Stand Off	A1	0.17	–	0.23
Wafer Thickness	A2	0.254 ± 0.025		
Body Size	D	2.84 BSC		
	E	2.84 BSC		
Ball Diameter (Size)		0.25		
Ball/Bump Width	b	0.23	0.26	0.29
Ball/Bump Pitch	eD	0.4		
	eE	0.4		
Ball/Bump Count	n	49		
Edge Ball Center to Center	D1	2.4 BSC		
	E1	2.4 BSC		
Package Edge Tolerance	aaa	0.03		
Coplanarity (whole wafer)	ccc	0.075		
Ball/Bump Offset (Package)	ddd	0.05		
Ball/Bump Offset (Ball)	eee	0.015		

Table 5-1. Device and WLCSP Package Maximum Weight

SAM G51G18	10	mg

Table 5-2. Package Reference

JEDEC Drawing Reference	na
JESD97 Classification	e1

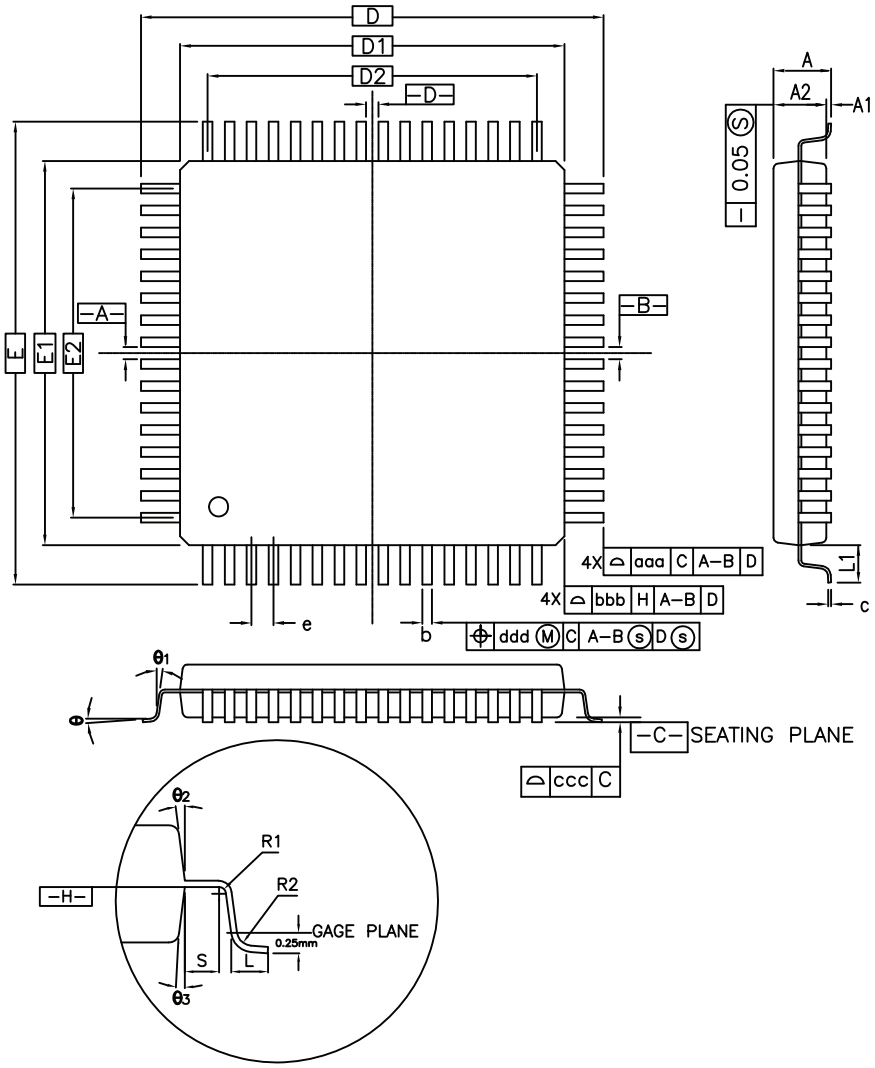
Table 5-3. WLCSP Package Characteristics

Moisture Sensitivity Level	1

This package respects the recommendations of the NEMI User Group.

5.2 100-lead LQFP Package

Figure 5-2. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 5-4. Device and LQFP Package Maximum Weight

SAM G51N18	675	mg

Table 5-5. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	e3

Table 5-6. LQFP Package Characteristics

Moisture Sensitivity Level	3

This package respects the recommendations of the NEMI User Group.

6. Ordering Information

Table 6-1. Ordering Codes for SAM G51 Devices

Ordering Code	MRL	Flash (Kbytes)	Package	Carrier Type	Package Type	Temperature Operating Range
SAMG51G18A-UUT	A	256	WLCSP49	Tape and Reel	Green	Industrial -40°C to 85°C
SAMG51N18A-AU	A	256	LQFP100	Tray	Green	Industrial -40°C to 85°C

7. Revision History

In the tables that follow, the most recent version of the document appears first.

Table 7-1. SAM G51 Datasheet Rev. 11209DS Revision History

Doc. Date	Change
19-Nov-14	"Description" Editorial changes; added paragraph about low-power modes; added sentence about "Event System"; in last paragraph, replaced "The device operates from 1.62V to 2V" with "The device operates from 1.7V to 2.0V"
	"Features" Minor editorial changes In "Analog" bullet, replaced "up to 800 KSps" with "up to 600 ksps" In "Low-power modes" bullet, renamed "Wake-up time" to "Wake-up time from wait mode to active mode"
	Section 1. "Configuration Summary" Minor editorial changes Table 1-1 "Configuration Summary": - in SAM G51G18 ADC configuration, replaced "800 KSps at 10-bit resolution / 200 KSps at 11-bit resolution / 50 KSps at 12-bit resolution" with "600 ksps at 10-bit resolution / 150 ksps at 11-bit resolution / 37 ksps at 12-bit resolution" - in SPI configuration, added cross-reference link to footnote No. 1
	Section 2. "SAM G51 Block Diagram" Updated Section 2-1 "SAM G51 Block Diagram"
	Section 3. "Signal Description" Minor formatting changes Table 3-1 "Signal Description List": - in VDDIO comments, replaced "1.62V to 2V" with "1.7V to 2.0V" - deleted "1V output" from VDDOUT comments - removed "PIOC" from "PIO Controller" heading - renamed heading "10-bit Analog-to-Digital Converter - ADCC" to "12-bit Analog-to-Digital Converter - ADC"
	Section 4. "Package and Pinout" Table 4-3 "SAM G51N18 100-lead Pinout": replaced two instances of "UNCONNECTED" with "NC"; added note to read "NC = Not connected"
	Section 5. "SAM G51 Mechanical Characteristics": no changes
	Section 6. "Ordering Information" Table 6-1 "Ordering Codes for SAM G51 Devices": deleted "Kbytes" from "Package" colunm header; added "Carrier Type" column

Table 7-2. SAM G51 Datasheet Rev. 11209CS 20-Dec-13 Revision History

Doc. Date	Change
20-Dec-13	First public issue.

Table 7-3. SAM G51 Datasheet Rev. 11209BS 23-Jul-13 Revision History

Doc. Date	Changes
23-Jul-13	Atmel internal document.

Table 7-4. SAM G51 Datasheet Rev. 11209AS 05-Dec-12 Revision History

Doc. Date	Changes
08-Mar-13	Atmel internal document.

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