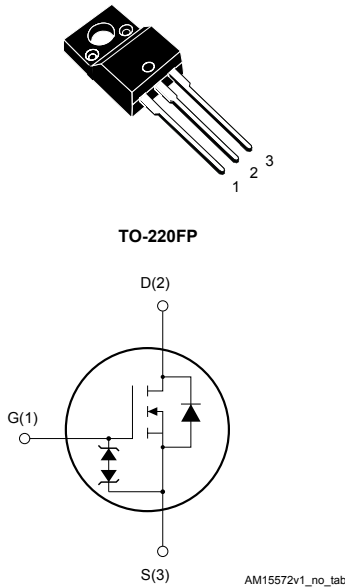


N-channel 600 V, 0.230 Ω typ., 13 A, MDmesh™ M2 EP Power MOSFET in a TO-220FP package



Features

| Order code | V_{DS} | $R_{DS(on)}$ max | I_D |
|---------------|----------|------------------|-------|
| STF20N60M2-EP | 600 V | 0.278 Ω | 13 A |

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters ($f > 150$ kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status

STF20N60M2-EP

Product summary

| | |
|-------------------|---------------|
| Order code | STF20N60M2-EP |
| Marking | 20N60M2EP |
| Package | TO-220FP |
| Packing | Tube |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------|
| V_{GS} | Gate-source voltage | ±25 | V |
| V_{GS} | Transient gate-source voltage ($t_p \leq 10$ ns) | ±35 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25$ °C | 13 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100$ °C | 8 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 52 | A |
| P_{TOT} | Total dissipation at $T_C = 25$ °C | 25 | W |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1$ s, $T_C = 25$ °C) | 2.5 | kV |
| T_{stg} | Storage temperature range | -55 to 150 | °C |
| T_j | Operating junction temperature range | | |

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 13$ A, $di/dt \leq 400$ A/ μ s, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400$ V
4. $V_{DS} \leq 480$ V

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case | 5 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | °C/W |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 2.7 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V) | 138 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$ | | | 1 | μA |
| | Drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3.25 | 4 | 4.75 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 6.5\text{ A}$ | | 0.230 | 0.278 | Ω |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|-------------------------------|--|------|------|------|---------------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 787 | - | μF |
| C_{oss} | Output capacitance | | - | 50 | - | |
| C_{riss} | Reverse transfer capacitance | | - | 1.2 | - | |
| $C_{oss\ eq.}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 89 | - | μF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 5.9 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior) | - | 22 | - | nC |
| Q_{gs} | Gate-source charge | | - | 3.5 | - | |
| Q_{gd} | Gate-drain charge | | - | 10.5 | - | |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching energy

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|--|--|------|------|------|---------------|
| E_{off} | Turn-off energy (from 90% V_{GS} to 0% I_D) | $V_{DD} = 400\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 7.2 | - | μJ |
| | | $V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 20.4 | - | μJ |

Table 7. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}$, $I_D = 6.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | - | 10.5 | - | ns |
| t_r | Rise time | | - | 5.2 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 41 | - | ns |
| t_f | Fall time | | - | 8 | - | ns |

Table 8. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 13 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 52 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 13\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 230 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.3 | | μC |
| I_{RRM} | Reverse recovery current | | - | 20 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 287 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.9 | | μC |
| I_{RRM} | Reverse recovery current | | - | 20.2 | | A |

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

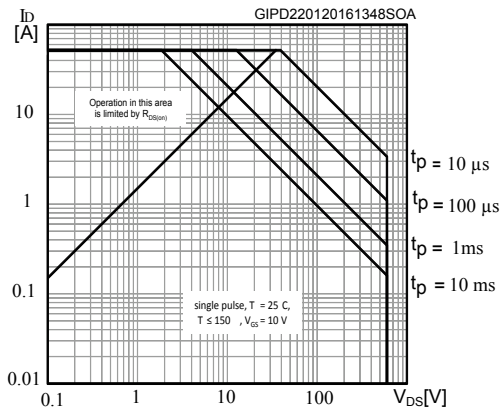


Figure 2. Thermal impedance

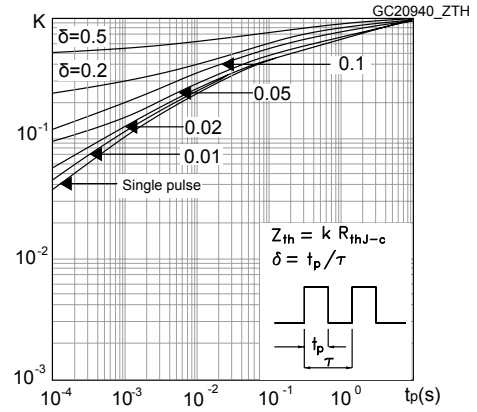


Figure 3. Output characteristics

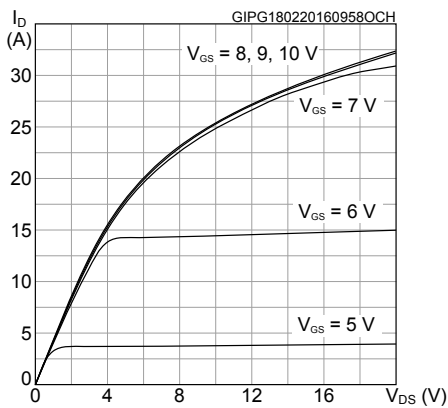


Figure 4. Transfer characteristics

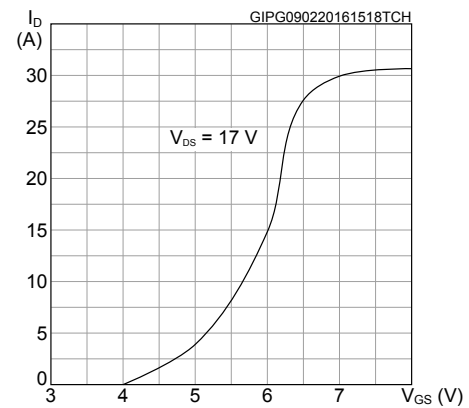


Figure 5. Gate charge vs gate-source voltage

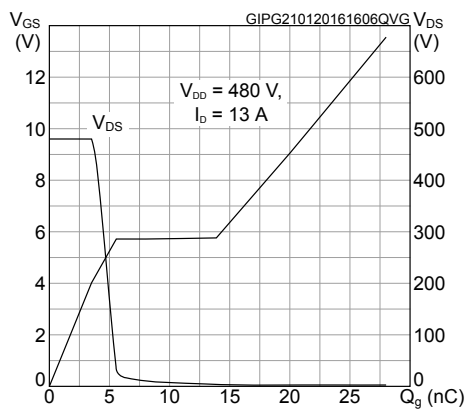


Figure 6. Static drain-source on-resistance

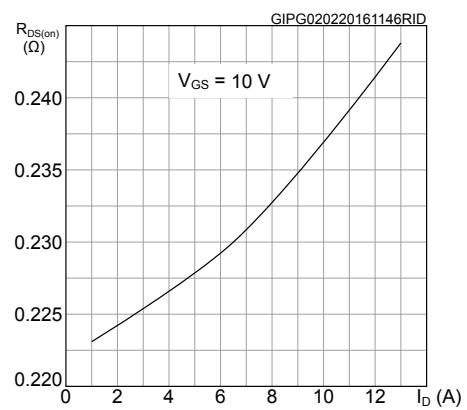


Figure 7. Capacitance variations

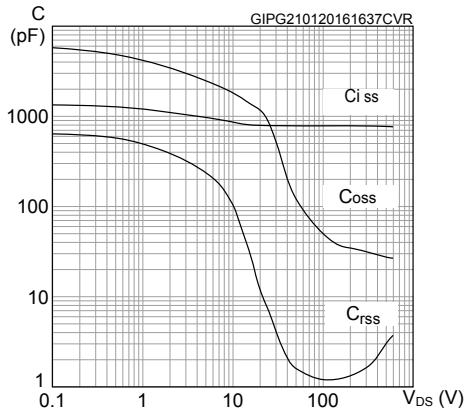


Figure 8. Output capacitance stored energy

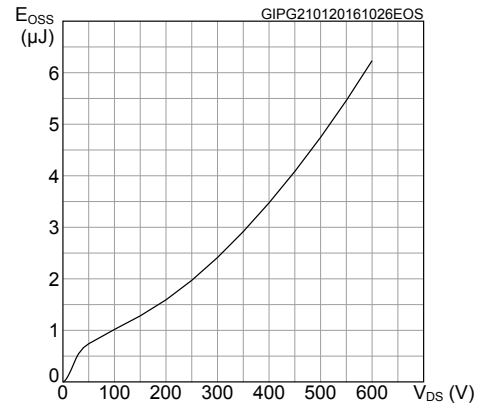


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

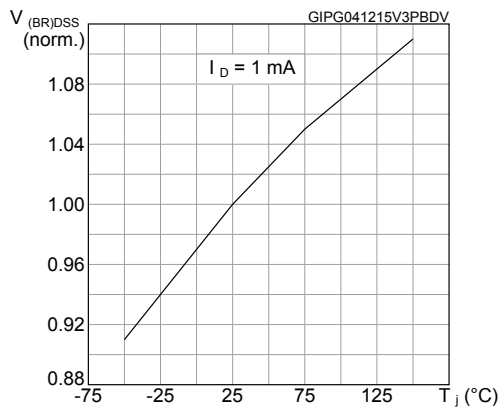


Figure 10. Normalized gate threshold voltage vs temperature

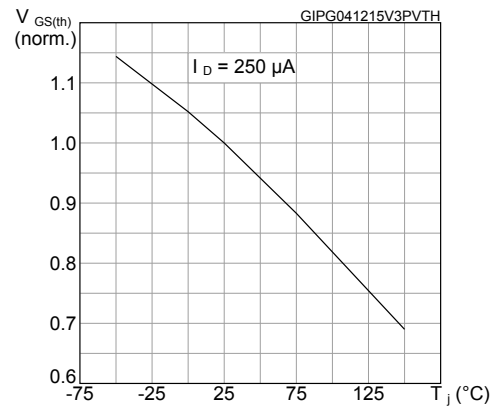


Figure 11. Normalized on-resistance vs temperature

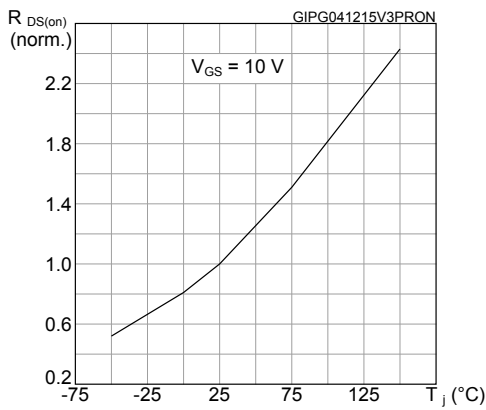


Figure 12. Source-drain diode forward characteristics

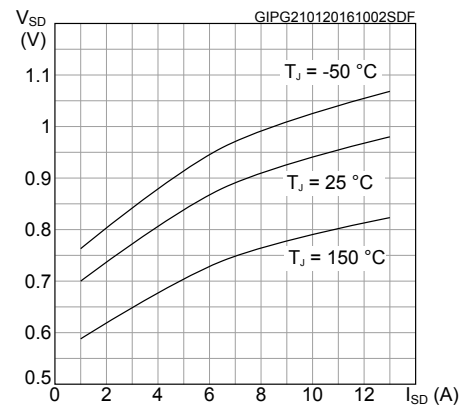
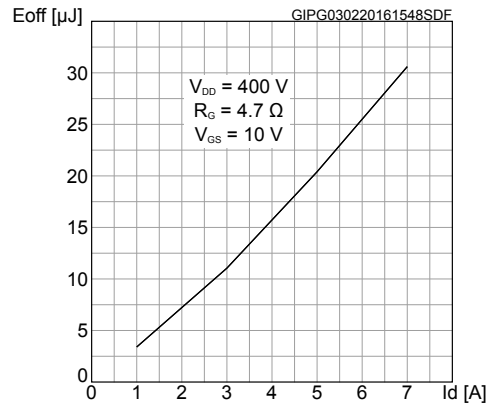
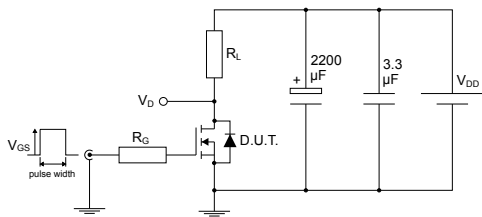


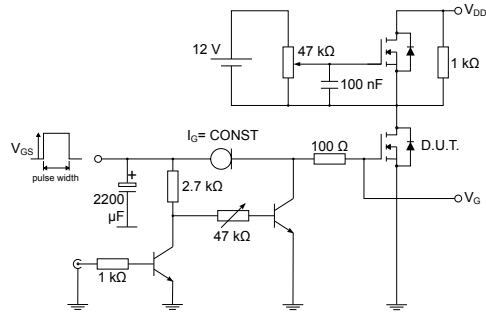
Figure 13. Turn-off switching energy vs drain current



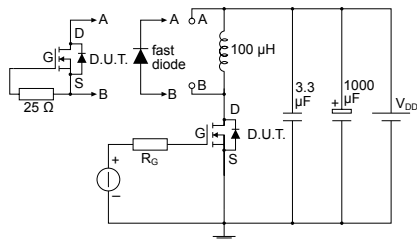
3 Test circuits

Figure 14. Test circuit for resistive load switching times


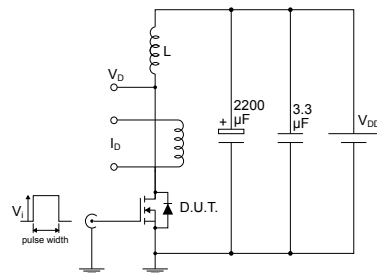
AM01468v1

Figure 15. Test circuit for gate charge behavior


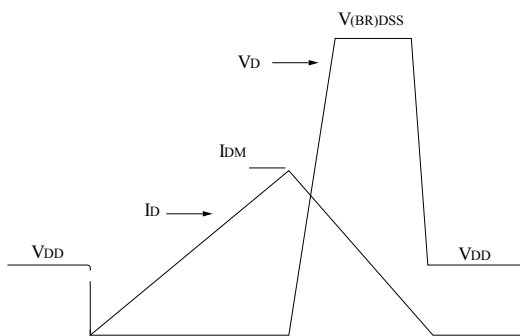
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


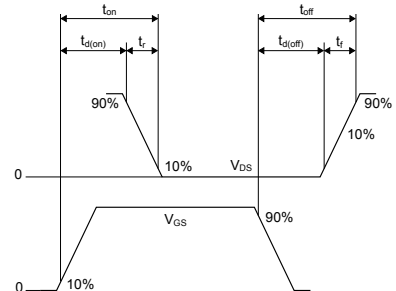
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


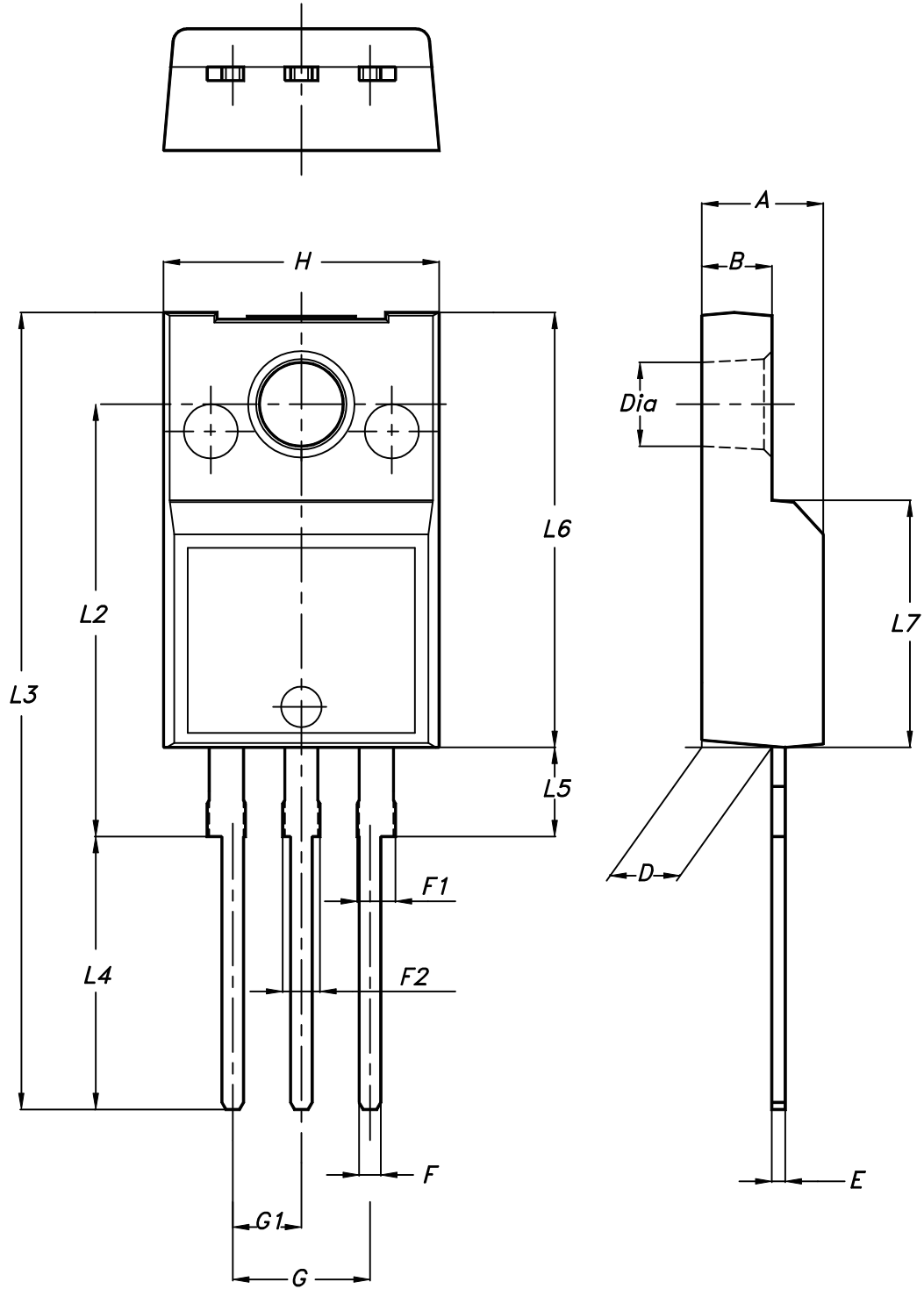
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline



7012510_Rev_12_B

Table 9. TO-220FP package mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 29-Feb-2016 | 1 | First release. |
| 18-Aug-2016 | 2 | Modified: <i>Table 2: "Absolute maximum ratings"</i> Minor text changes |
| 02-Mar-2018 | 3 | Removed maturity status indication from cover page. The document status is production data. Updated <i>Table 1. Absolute maximum ratings</i> , <i>Table 4. On/off states</i> and <i>Table 5. Dynamic</i> . Updated <i>Figure 1. Safe operating area</i> , <i>Figure 3. Output characteristics</i> , <i>Figure 4. Transfer characteristics</i> and <i>Figure 5. Gate charge vs gate-source voltage</i> . Minor text changes. |
| 04-Jun-2018 | 4 | Modified Table 1. Absolute maximum ratings . Modified Figure 1. Safe operating area . Modified Table 8. Source-drain diode . Minor text changes. |

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