Async/Page CellularRAM™ 1.0 Memory

MT45W4MW16P*

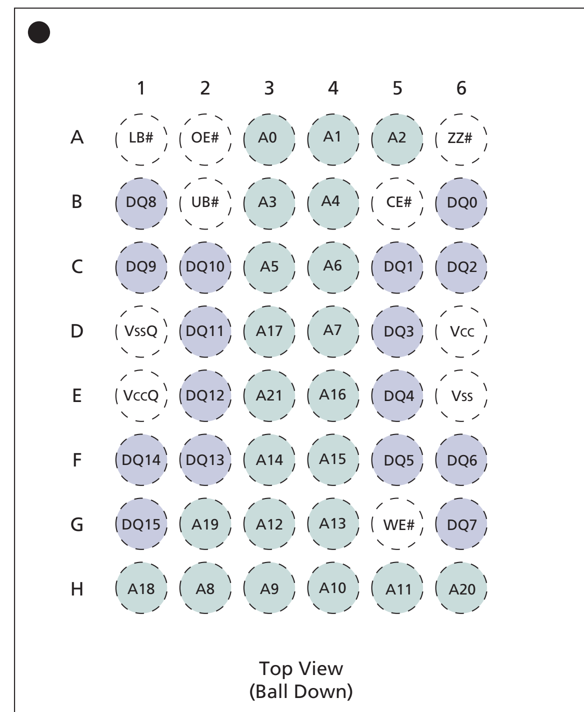
*Note: Not recommended for new designs.

For the latest data sheet, refer to Micron's Web site: http://www.micron.com/products/psram/

Features

- Asynchronous and page mode interface
- Random access time: 70ns, 85ns
- VCC, VCCQ voltages
  1.70V–1.95V VCC
  1.70V–3.30V VCCQ
- Page mode read access
  Sixteen-word page size
  Interpage read access: 70ns, 85ns
  Intrapage read access: 20ns, 25ns
- Low power consumption
  Asynchronous READ: <25mA
  Intrapage READ: <15mA
  Standby: 120µA – standard
  100µA – low-power option
  Deep power-down: <10µA (TYP @ 25°)
- Low-power features
  Temperature-compensated refresh (TCR)
  Partial-array refresh (PAR)
  Deep power-down (DPD) mode

Figure 1: Ball Assignment – 48-Ball VFBGA



Options	Designator
• Configuration	
4 Meg x 16	MT45W4MW16P[1]
• Package	
48-ball VFBGA (standard)	FA
48-ball VFBGA (lead-free)	BA[2]
• Access time	
70ns	-70
85ns	-85
• Standby power	
Standard	None
Low power	L

Options (continued)	Designator
• Operating temperature range	
Wireless (-30°C to +85°C)	WT[3]
Industrial (-40°C to +85°C)	IT[2]

Notes: 1. Not recommended for new designs.
2. Contact factory.
3. -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.

Part Number Example:

MT45W4MW16PFA-70LWT

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General Description

Micron® CellularRAM™ products are high-speed, CMOS PSRAM memories developed for low-power, portable applications. The MT45W4MW16PFA is a 64Mb DRAM core device organized as 4 Meg x 16 bits. This device includes the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings.

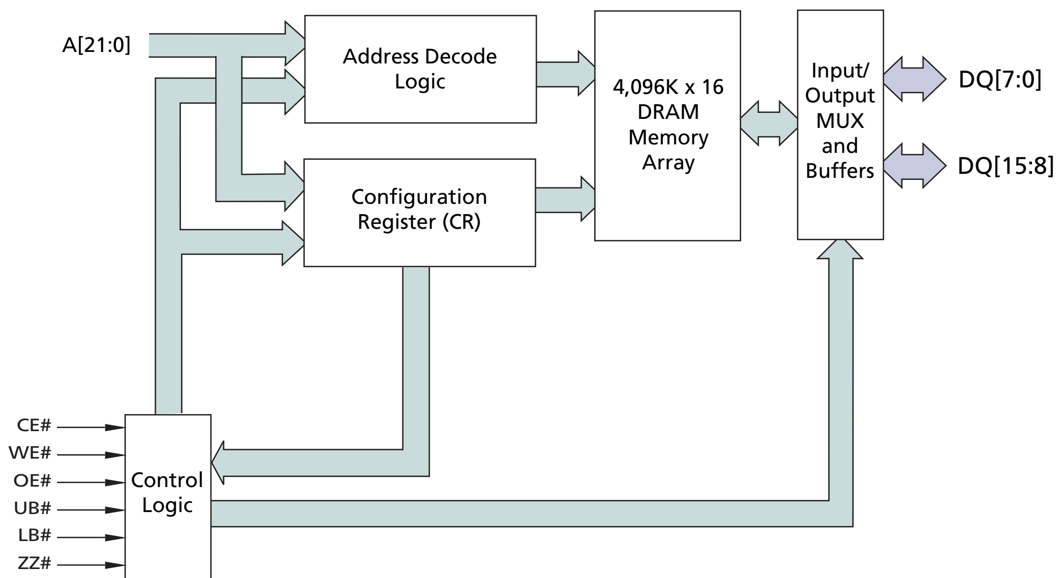
Operating voltages have been reduced in an effort to minimize power consumption. The core voltage has been reduced to a 1.80V operating level. To maintain compatibility with different memory bus interfaces, CellularRAM devices are available with I/O voltages of 3.0V, 2.5V, or 1.8V.

A user-accessible configuration register (CR) defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

To operate seamlessly on an asynchronous memory bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. CellularRAM products include three system-accessible mechanisms used to minimize refresh current. Temperature-compensated refresh (TCR) is used to adjust the refresh rate according to the case temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Setting sleep enable (ZZ#) to LOW enables one of two low-power modes: partial-array refresh (PAR) or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

Figure 2: Functional Block Diagram: 4 Meg x 16



Note: Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

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Table 1: VFBGA Ball Descriptions

VFBGA Ball Assignment	Symbol	Type	Description
E3, H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[21:0]	Input	Address Inputs: Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the CR.
A6	ZZ#	Input	Sleep Enable: When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR).
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Enables WRITE operations when LOW.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
D6	V_{CC}	Supply	Device Power Supply: (1.70V–1.95V) Power supply for device core operation.
E1	$V_{CC}Q$	Supply	I/O Power Supply: (1.70V–3.30V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	$V_{SS}Q$	Supply	$V_{SS}Q$ must be connected to ground.

Table 2: Bus Operations

Mode	Power	CE#	WE#	OE#	LB#/UB#	ZZ#	DQ[15:0][1]	Notes
Standby	Standby	H	X	X	X	H	High-Z	2, 5
Read	Active	L	H	L	L	H	Data-Out	1, 4
Write	Active	L	L	X	L	H	Data-In	1, 3, 4
No Operation	Idle	L	X	X	X	H	X	4, 5
PAR	Partial-Array Refresh	H	X	X	X	L	High-Z	6
DPD	Deep Power-Down	H	X	X	X	L	High-Z	6
Load Configuration Register	Active	L	L	X	X	L	High-Z	

Notes:
1. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# only is in select mode, only DQ[7:0] are affected. When UB# only is in the select mode, DQ[15:8] are affected.
2. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When WE# is invoked, the OE# input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
6. DPD is enabled when configuration register bit CR[4] is “0”; otherwise, PAR is enabled.

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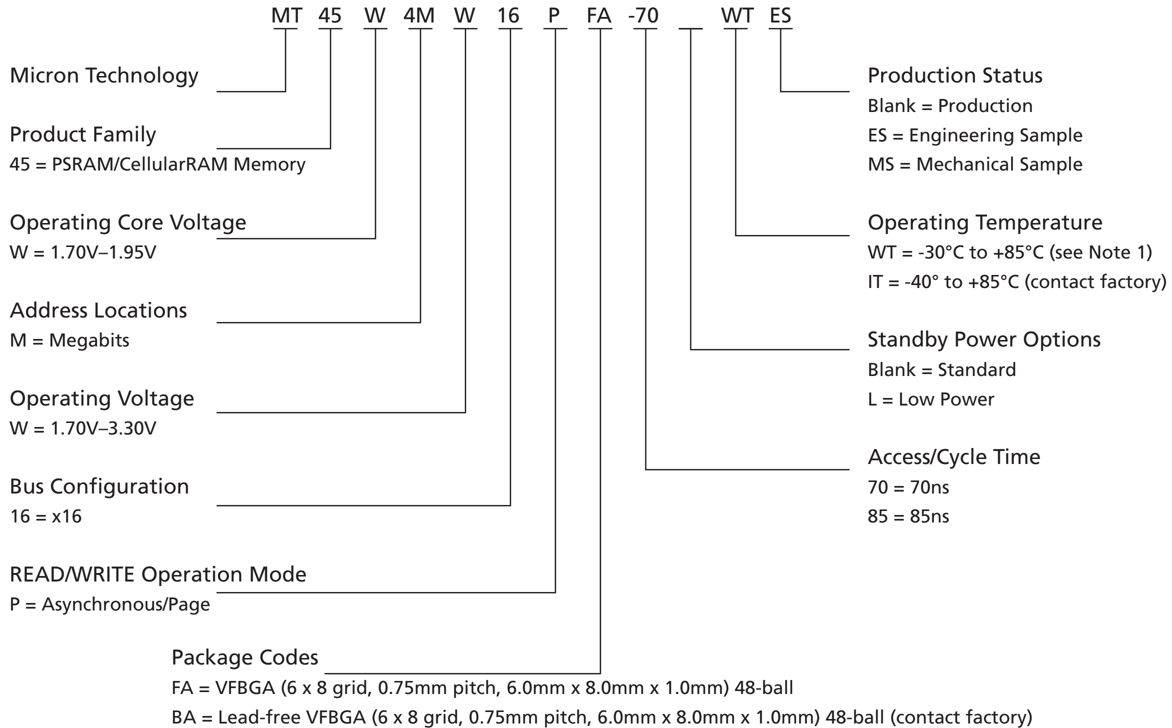
Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

Figure 3: Part Number Chart



Note: -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.

Valid Part Number Combinations

After building the part number from the part numbering chart, please go to the Micron Part Marking Decoder Web site at http://www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at http://www.micron.com/partsearch. To view the location of the abbreviated mark on the device, please refer to customer service note, CSN-11, “Product Mark/Label,” at http://www.micron.com/csn.

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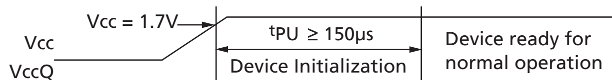
Functional Description

In general, the MT45W4MW16PFA device is a high-density alternative to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The MT45W4MW16PFA contains a 67,108,864-bit DRAM core organized as 4,194,304 addresses by 16 bits. This device implements the industry-standard, asynchronous memory interface found on other low-power SRAM or Pseudo SRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default settings. VCC and VCCQ must be applied simultaneously, and when they reach a stable level above 1.70V, the device will require 150µs to complete its self-initialization process (see Figure 4). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation. At power-up, the CR is set to 0070h.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

The MT45W4MW16PFA CellularRAM product incorporates the industry-standard, asynchronous interface found on other low-power SRAM or Pseudo SRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a “Don't Care”; WE# will override OE#. The data to be written will be latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). WE# LOW time must be limited to ^tCEM.

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Figure 5: READ Operation

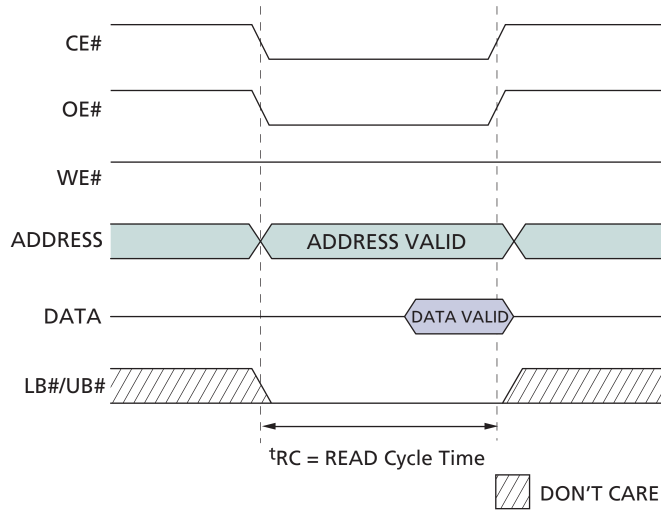
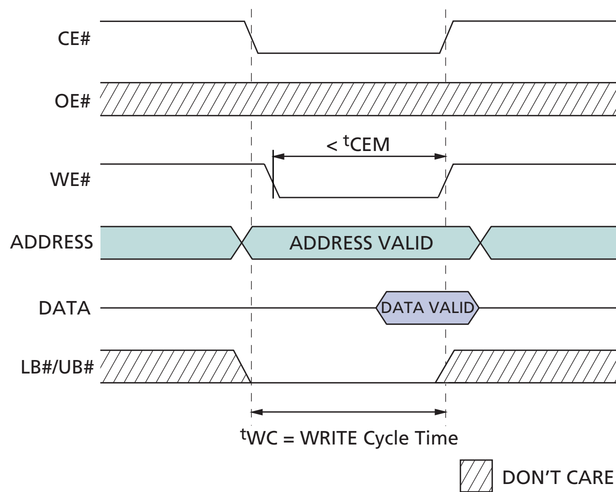


Figure 6: WRITE Operation



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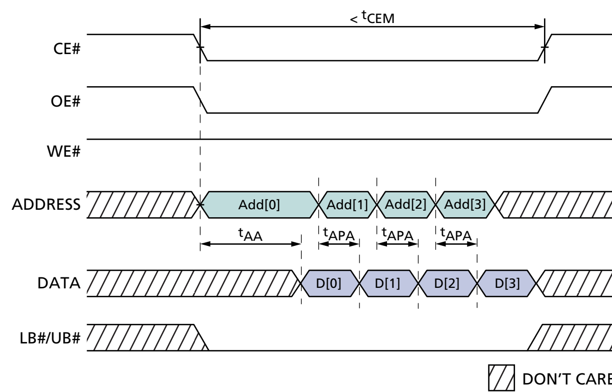
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any changes in addresses A[4] or higher will initiate a new ^{t}AA access. Figure 7 shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM.

Figure 7: Page READ Operation



LB#/UB# Operation

The lower byte (LB#) enable and upper byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQ. The DQ associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, the device remains in an active mode as long as CE# remains LOW.

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Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. STANDBY operation occurs when CE# and ZZ# are HIGH.

The device will enter a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature-Compensated Refresh

Temperature-compensated refresh is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires more frequent REFRESH operations to maintain data integrity as temperatures increase. More frequent refresh is required due to the increased leakage of the DRAM's capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. For example, if the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Partial-Array Refresh

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 3 on page 15). READ and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bringing ZZ# to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see Software Access to the Configuration Register on page 13). PAR is enabled immediately upon setting CR[4] to "1" using this method. However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up. (See Figure 8.)

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing ZZ# to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

Driving ZZ# LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

The device should not be put into DPD using CR software access.

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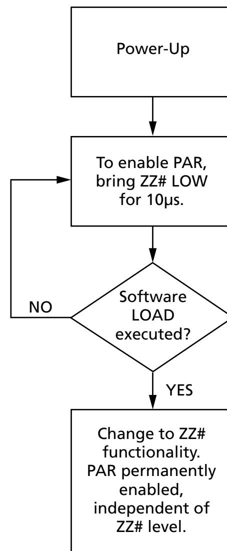
Figure 8: Software Access PAR Functionality



Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

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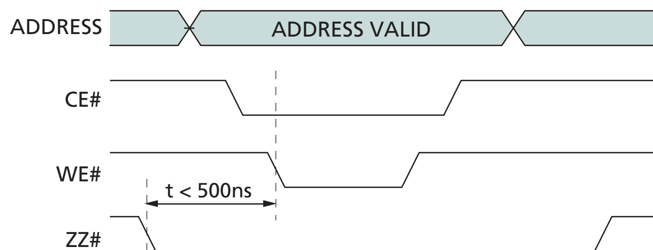
Configuration Register Operation

The configuration register (CR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated anytime while the device is operating in a standby state.
Figure 12 on page 15 describes the control bits used in the CR. At power up, the CR is set to 0070h.

Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 9). The values placed on addresses A[21:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are “Don’t Care.” Access using ZZ# is WRITE only.

Figure 9: Load Configuration Register Operation



Software Access to the Configuration Register

The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for ZZ# ball.

If the software mechanism is used, ZZ# can simply be tied to VCCQ. The port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to VCCQ if the system will use DPD; DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 10). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 11). Note that a third READ cycle of the highest address cancels the sequence until a different address is read.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the content at this address is changed by using this sequence (note that this is a deviation from the CellularRAM specification). The data bus is used to transfer data into or out of bits 15–0 of the CR.

Writing to the CR using the software sequence modifies the function of ZZ#. Once the software sequence loads the CR, the ZZ# level no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This ZZ# functionality will continue until the next time the device is powered up. The operation of ZZ# is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ#-controlled) method of loading the CR.

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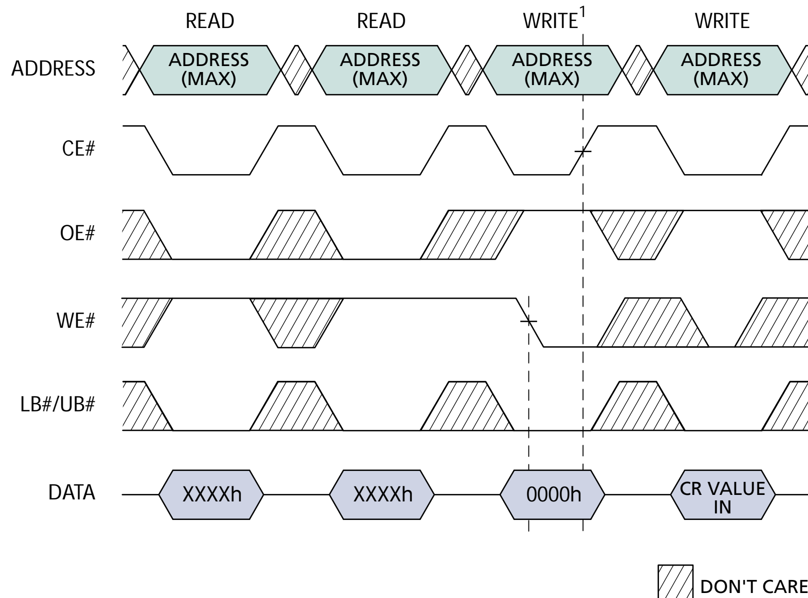
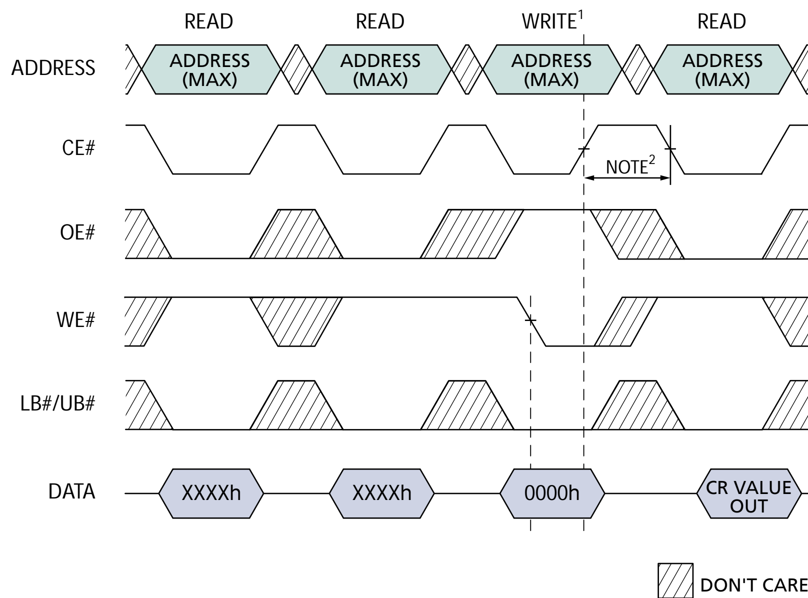
Figure 10: Software Access Load Configuration Register



Note: The WRITE on the third cycle must be CE#-controlled.

Figure 11: Software Access Read Configuration Register



Notes:
1. The WRITE on the third cycle must be CE#-controlled.
2. CE# must be HIGH for 150ns before performing the cycle that reads the configuration register.

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Figure 12: Configuration Register Bit Mapping

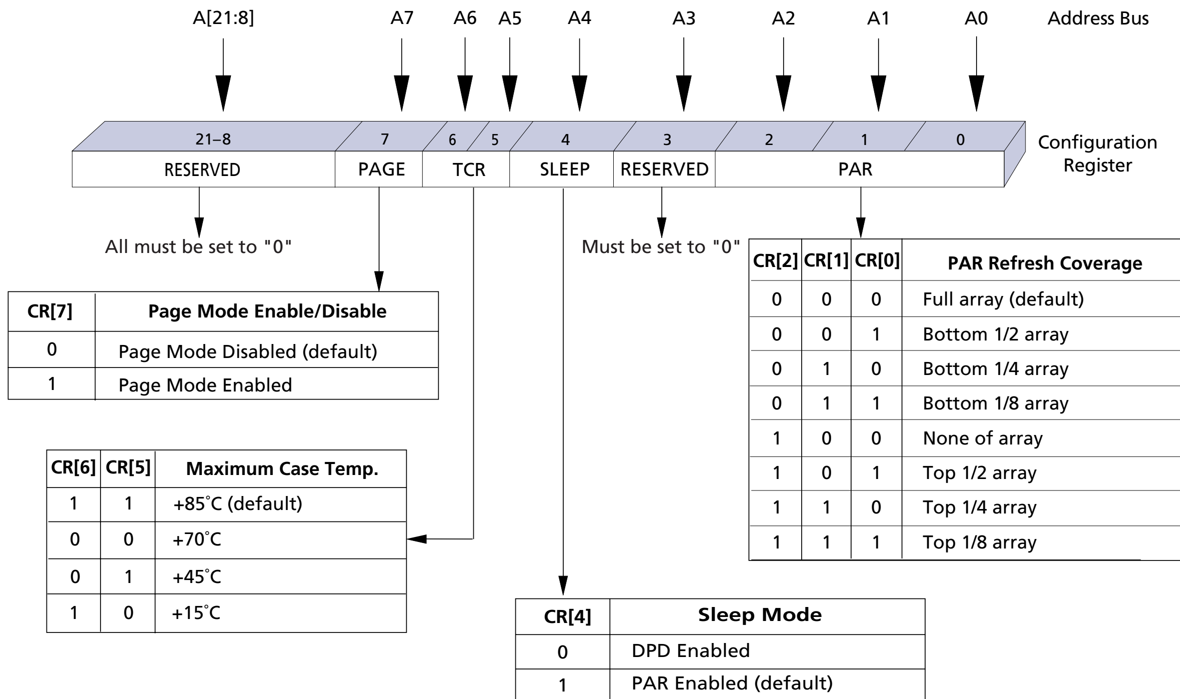

Table 3: 64Mb Address Patterns for PAR (CR[4] = 1)

CR[2]	CR[1]	CR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	200000h–3FFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	300000h–3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	380000h–3FFFFFh	512K x 16	8Mb

Partial-Array Refresh (CR[2:0]) Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 3).

Sleep Mode (CR[4]) Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using ZZ# to access the CR.

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DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

Temperature-Compensated Refresh (CR[6:5]) Default = +85°C Operation

The TCR bits allow for adequate refresh at four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Page Mode READ Operation (CR[7]) Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

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Electrical Characteristics

Table 4: Absolute Maximum Ratings

Parameter	Rating
Voltage to Any Ball Except Vcc, VccQ Relative to Vss	-0.50V to (4.0V or VccQ + 0.3V, whichever is less)
Voltage on Vcc Supply Relative to Vss	-0.20V to 2.45V
Voltage on VccQ Supply Relative to Vss	-0.20V to 4.0V
Storage Temperature	-55°C to +150°C
Operating Temperature (case) Wireless (see Note 1) Industrial	 -30°C to +85°C -40°C to +85°C
Soldering Temperature and Time 10s (solder ball only)	 +260°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes: 1. -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.

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Table 5: Electrical Characteristics and Operating Conditions

Wireless Temperature[1] (-30°C ≤ T_C ≤ +85 °C), Industrial Temperature (-40°C < T_C < +85°C).

Description	Conditions	Symbol		Min	Max	Units	Notes
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		$V_{CC}Q$		1.70	3.30	V	
Input High Voltage		V_{IH}		1.4	$V_{CC}Q$ + 0.2	V	2, 3
Input Low Voltage		V_{IL}		-0.2	+0.4	V	4
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 $V_{CC}Q$		V	
Output Low Voltage	I_{OL} = 0.2mA	V_{OL}			0.20 $V_{CC}Q$	V	
Input Leakage Current	V_{IN} = 0 to $V_{CC}Q$	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random READ/WRITE	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, I_{OUT} = 0	$I_{CC}1$	-70		25	mA	5
			-85		20		
Asynchronous Page READ		$I_{CC}1P$	-70		15	mA	5
			-85		12		
Standby Current	V_{IN} = $V_{CC}Q$ or 0V CE# = $V_{CC}Q$	I_{SB}	Standard		120	µA	6
			Low-Power (L)		100		

Notes:
1. -30°C exceeds the CellularRAM Working Group 1.0 specification of -25°C.
2. Input signals may overshoot to $V_{CC}Q$ + 1.0V for periods less than 2ns during transitions.
3. V_{IH} (MIN) value is not aligned with CellularRAM Working Group 1.0 specification of $V_{CC}Q$ - 0.4V.
4. Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions
5. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
6. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. In order to achieve low standby current, all inputs must be driven to $V_{CC}Q$ or V_{SS}. I_{SB} may be slightly higher for up to 500ms after power-up or when entering standby mode.

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Maximum and Typical Standby Currents

The following tables and figures refer to the maximum and typical standby currents for the MT45W4MW16PFA device. The typical values shown in Figure 13 are measured with the appropriate PAR and TCR settings. The maximum values shown in Table 6 and Table 7 are measured with the relevant TCR bits set in the configuration register.

Table 6: Maximum Standby Currents for Applying PAR and TCR Settings

PAR	TCR			
	+15°C (RCR[6:5] = 10b)	+45°C (RCR[6:5] = 01b)	+70°C (RCR[6:5] = 00b)	+85°C (RCR[6:5] = 11b)
Full Array	70	85	105	120
1/2 Array	65	80	100	115
1/4 Array	60	75	95	110
1/8 Array	57	70	90	105
0 Array	50	55	60	70

Notes:
1. For RCR[6:5] = 00b (default), refer to Figure 13, Typical Refresh Current vs. Temperature (I_{TCR}), on page 20 for typical values.
2. In order to achieve low standby current, all inputs must be driven to $V_{CC}Q$ or V_{SS}. I_{SB} may be slightly higher for up to 500ms after power-up or when entering standby mode.
3. TCR values for 85°C are 100 percent tested. TCR values for 15°C, 45°C, and 70°C are sampled only.

Table 7: Maximum Standby Currents for Applying PAR and TCR Settings – Low-Power (L)

PAR	TCR			
	+15°C (RCR[6:5] = 10b)	+45°C (RCR[6:5] = 01b)	+70°C (RCR[6:5] = 00b)	+85°C (RCR[6:5] = 11b)
Full Array	60	70	85	100
1/2 Array	57	65	80	95
1/4 Array	54	61	75	90
1/8 Array	52	58	70	85
0 Array	50	55	60	70

Notes:
1. For RCR[6:5] = 00b (default), refer to Figure 13, Typical Refresh Current vs. Temperature (I_{TCR}), on page 20 for typical values.
2. In order to achieve low standby current, all inputs must be driven to $V_{CC}Q$ or V_{SS}. I_{SB} may be slightly higher for up to 500ms after power-up or when entering standby mode.
3. TCR values for 85°C are 100 percent tested. TCR values for 15°C, 45°C, and 70°C are sampled only.

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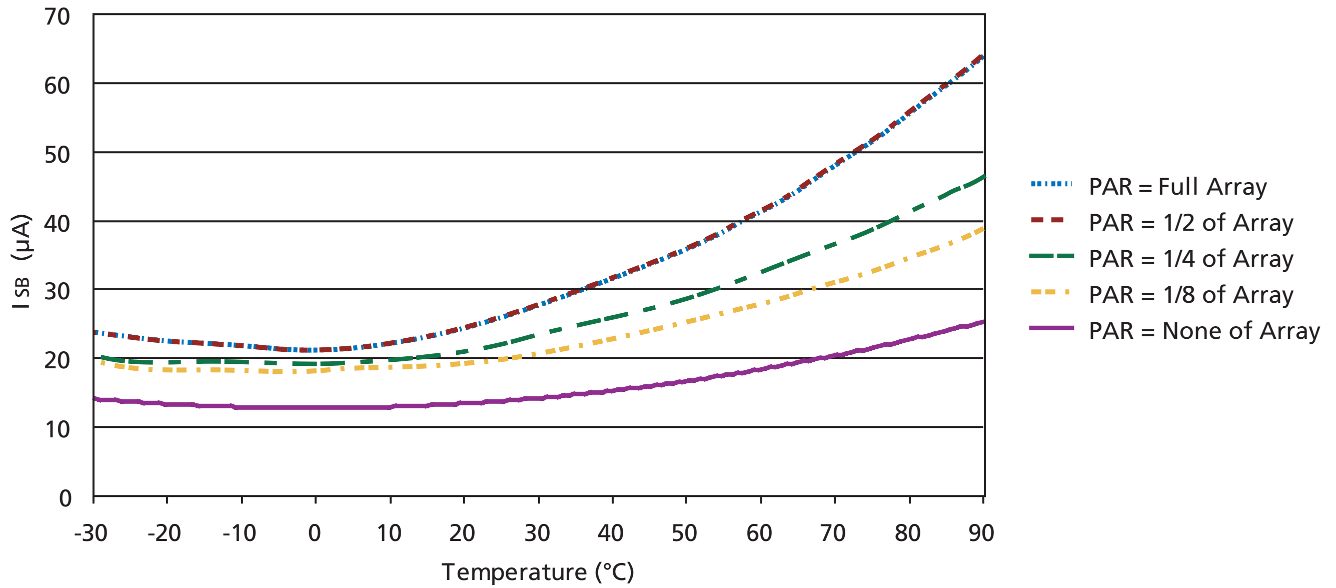
Figure 13: Typical Refresh Current vs. Temperature (ITCR)



Note: Typical ISB currents for each PAR setting with the appropriate TCR selected.

Table 8: Deep Power-Down Specifications and Conditions

Description	Conditions	Symbol	Typ	Units
Deep Power-Down	VIN = VCCQ or 0V; +25°C ZZ# = 0V CR[4] = 0	IZZ	10	µA

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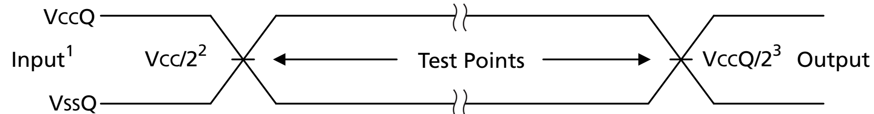
Table 9: Capacitance Specifications and Conditions

Description	Conditions	Symbol	Min	Max	Units	Notes
Input Capacitance	T_C = +25°C; f = 1 MHz; VIN = 0V	CIN	2.0	6	pF	1
Input/Output Capacitance (DQ)		CIO	2.5	6	pF	1

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.

Figure 14: AC Input/Output Reference Waveform



Notes: 1. AC test inputs are driven at VccQ for a logic 1 and VssQ for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at Vcc/2. Due to the possibility of a difference between Vcc and VccQ, the input test point may not be shown to scale.
3. Output timing ends at VccQ/2.

Figure 15: Output Load Circuit

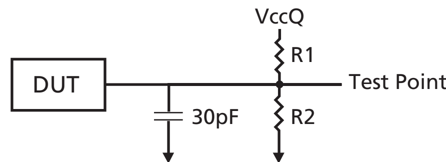


Table 10: Output Load Circuit

VccQ	R1/R2
1.8V	2.7KΩ
2.5V	3.7KΩ
3.0V	4.5KΩ

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Table 11: READ Cycle Timing Requirements

Parameter	Symbol	-70		-85		Units	Notes
		Min	Max	Min	Max		
Address Access Time	^tAA		70		85	ns	
Page Access Time	^tAPA		20		25	ns	
LB#/UB# Access Time	^tBA		70		85	ns	
LB#/UB# Disable to High-Z Output	^tBHZ		8		8	ns	2
LB#/UB# Enable to Low-Z Output	^tBLZ	10		10		ns	1
Maximum CE# Pulse Width	^tCEM		8		8	µs	3
Chip Select Access Time	^tCO		70		85	ns	
Chip Disable to High-Z Output	^tHZ		8		8	ns	2
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
Output Enable to Valid Output	^tOE		20		20	ns	
Output Hold from Address Change	^tOH	5		5		ns	
Output Disable to High-Z Output	^tOHZ		8		8	ns	2
Output Enable to Low-Z Output	^tOLZ	5		5		ns	1
Page Cycle Time	^tPC	20		25		ns	
Read Cycle Time	^tRC	70		85		ns	

Notes:
1. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 21. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 21. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. Page-mode enabled only.

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Table 12: WRITE Cycle Timing Requirements

Parameter	Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units	Notes
Address Setup Time	^tAS	0		0		ns	
Address Valid to End of Write	^tAW	70		85		ns	
Byte Select to End of Write	^tBW	70		85		ns	
CE# HIGH Time During Write	^tCPH	5		5		ns	
Chip Enable to End of Write	^tCW	70		85		ns	
Data Hold from Write Time	^tDH	0		0		ns	
Data Write Setup Time	^tDW	23		25		ns	
Chip Enable to Low-Z Output	^tLZ	10		10		ns	1
End Write to Low-Z Output	^tOW	5		5		ns	1
Write Cycle Time	^tWC	70		85		ns	
Write to High-Z Output	^tWHZ		8		8	ns	2
Write Pulse Width	^tWP	46		50		ns	3
Write Pulse Width HIGH	^tWPH	10		10		ns	
Write Recovery Time	^tWR	0		0		ns	

Notes:
1. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 21. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 21. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. WE# LOW time must be limited to ^tCEM (8µs).

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Table 13: Load Configuration Register Timing Requirements

Description	Symbol	-70		-85		Units
		Min	Max	Min	Max	
Address Setup Time	^tAS	0		0		ns
Address Valid to End of Write	^tAW	70		85		ns
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns
Chip Enable to End of Write	^tCW	70		85		ns
Write Cycle Time	^tWC	70		85		ns
Write Pulse Width	^tWP	40		40		ns
Write Recovery Time	^tWR	0		0		ns
ZZ# LOW to WE# LOW	^tZZWE	10	500	10	500	ns

Table 14: Deep Power-Down Timing Requirements

Description	Symbol	-70		-85		Units
		Min	Max	Min	Max	
Chip Deselect to ZZ# LOW	^tCDZZ	5		5		ns
Deep Power-Down Recovery	^tR	150		150		µs
Minimum ZZ# Pulse Width	^tZZMIN	10		10		µs

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Timing Diagrams

Figure 16: Power-Up Initialization Period

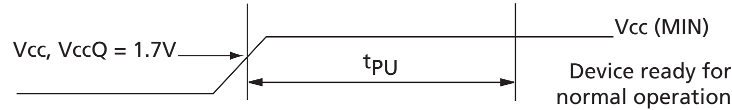

Table 15: Power-Up Initialization Timing Requirements

Parameter	Symbol	-70		-85		Units
		Min	Max	Min	Max	
Power-Up Initialization Period	^tPU	150		150		µs

Figure 17: Load Configuration Register

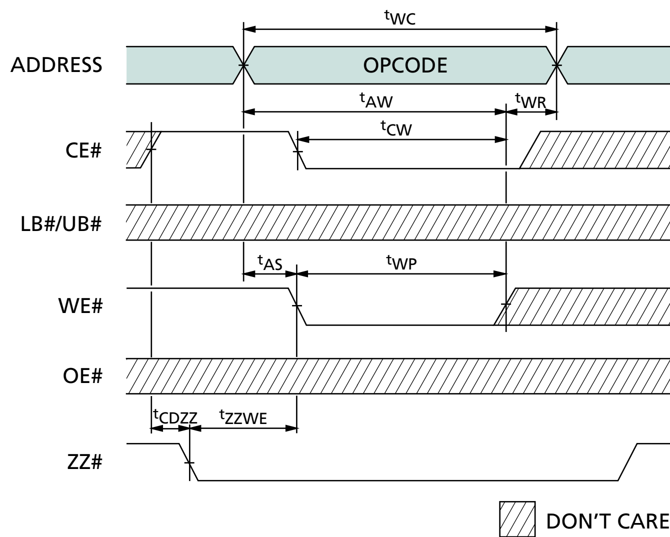

Table 16: Load Configuration Register Timing Requirements

Symbol	-70		-85		Units
	Min	Max	Min	Max	
^tAS	0		0		ns
^tAW	70		85		ns
^tCDZZ	5		5		ns
^tCW	70		85		ns

Symbol	-70		-85		Units
	Min	Max	Min	Max	
^tWC	70		85		ns
^tWP	40		40		ns
^tWR	0		0		ns
^tZZWE	10	500	10	500	ns

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Figure 18: Deep Power-Down – Entry/Exit

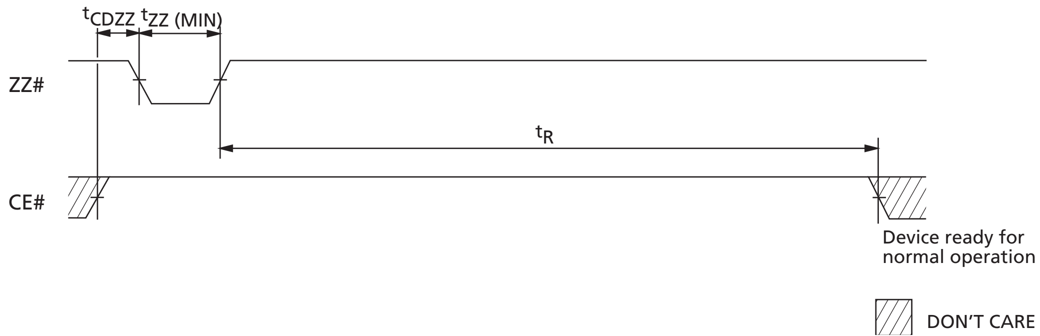

Table 17: Deep Power-Down Timing Parameters

Symbol	-70		-85		Units
	Min	Max	Min	Max	
^{t}CDZZ	5		5		ns
^{t}R	150		150		µs
^{t}ZZ (MIN)	10		10		µs

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Figure 19: Single READ Operation (WE# = VIH)

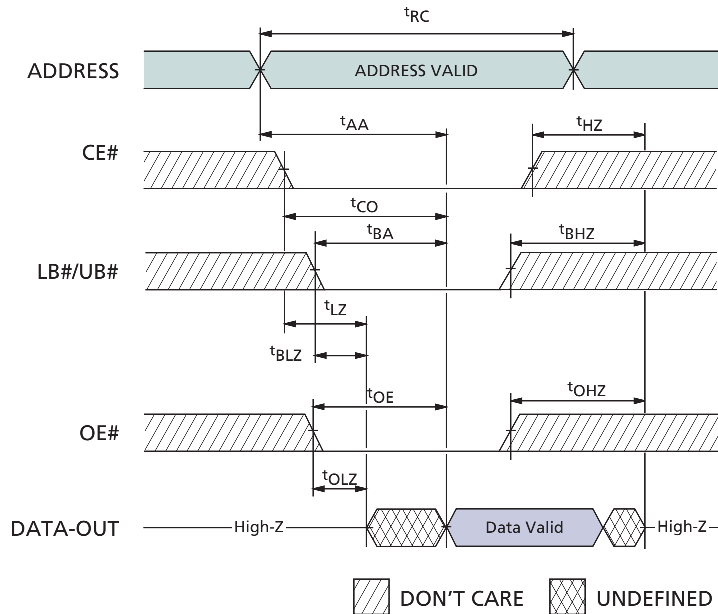

Table 18: READ Timing Parameters

Symbol	-70		-85		Units
	Min	Max	Min	Max	
tAA		70		85	ns
tBA		70		85	ns
tBHZ		8		8	ns
tBLZ	10		10		ns
tCO		70		85	ns
tHZ		8		8	ns
tLZ	10		10		ns
tOE		20		20	ns
tOHZ		8		8	ns
tOLZ	5		5		ns
tRC	70		85		ns

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Figure 20: Page Mode READ Operation (WE# = VIH)

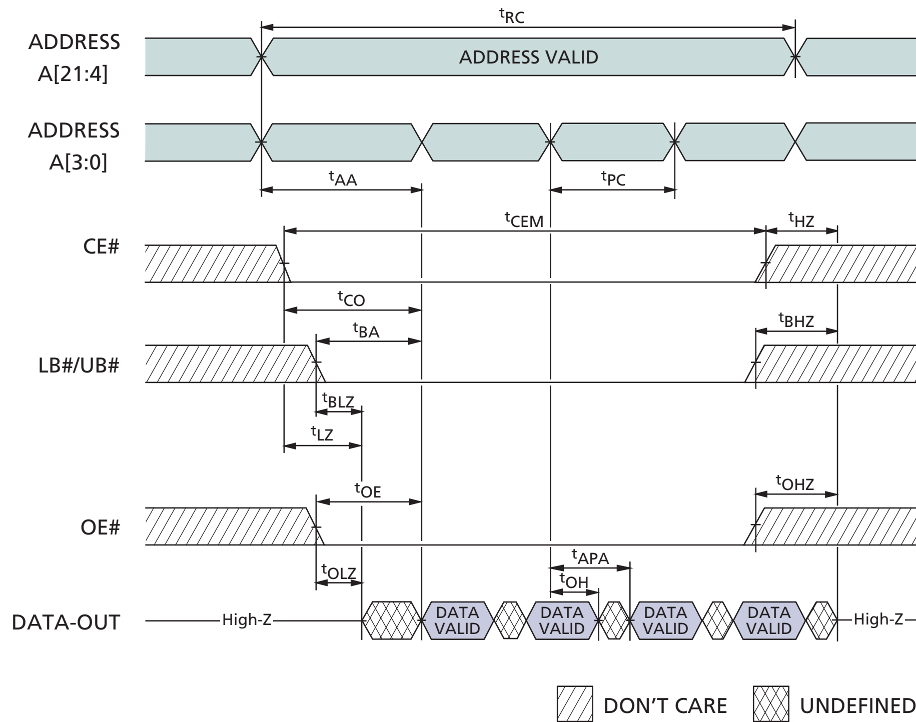

Table 19: Page Mode READ Timing Parameters

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^{t}AA		70		85	ns
^{t}APA		20		25	ns
^{t}BA		70		85	ns
^{t}BHZ		8		8	ns
^{t}BLZ	10		10		ns
^{t}CEM		8		8	µs
^{t}CO		70		85	ns
^{t}HZ		8		8	ns

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^{t}LZ	10		10		ns
^{t}OE		20		20	ns
^{t}OH	5		5		ns
^{t}OHZ		8		8	ns
^{t}OLZ	5		5		ns
^{t}PC	20		25		ns
^{t}RC	70		85		ns

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Figure 21: WRITE Cycle (WE#-Controlled)

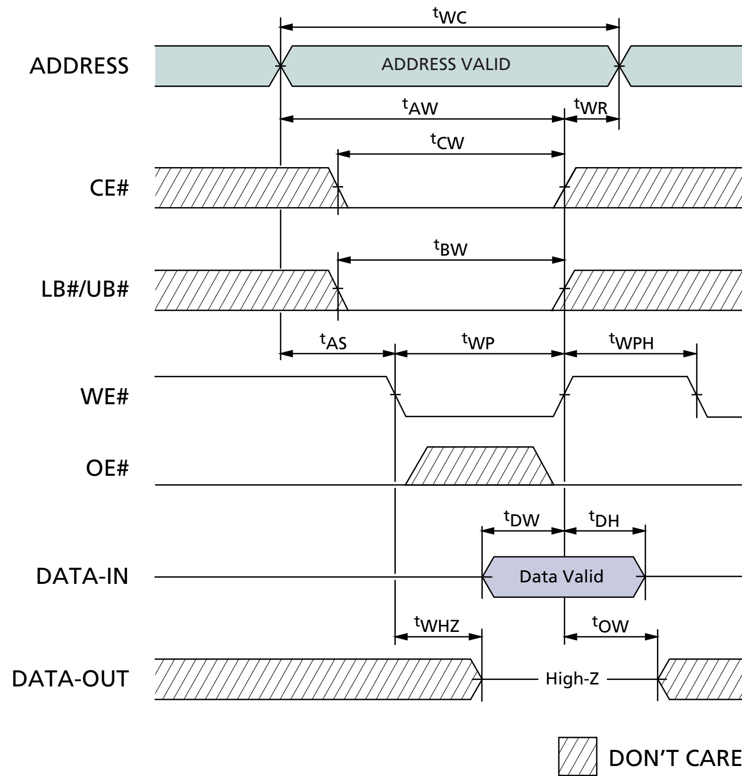

Table 20: WRITE Timing Parameters

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^tAS	0		0		ns
^tAW	70		85		ns
^tBW	70		85		ns
^tCW	70		85		ns
^tDH	0		0		ns
^tDW	23		25		ns

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^tOW	5		5		ns
^tWC	70		85		ns
^tWHZ		8		8	ns
^tWP	46		50		ns
^tWPH	10		10		ns
^tWR	0		0		ns

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Figure 22: WRITE Cycle (CE#-Controlled)

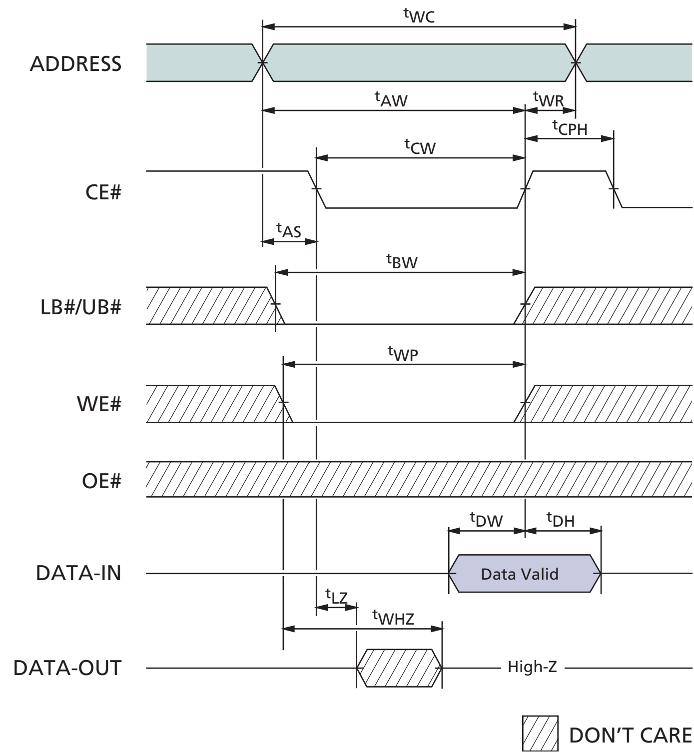

Table 21: WRITE Timing Parameters

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^{t}AS	0		0		ns
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CPH	5		5		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^{t}DW	23		25		ns
^{t}LZ	10		10		ns
^{t}WC	70		85		ns
^{t}WHZ		8		8	ns
^{t}WP	46		50		ns
^{t}WR	0		0		ns

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Figure 23: WRITE Cycle (LB#/UB#-Controlled)

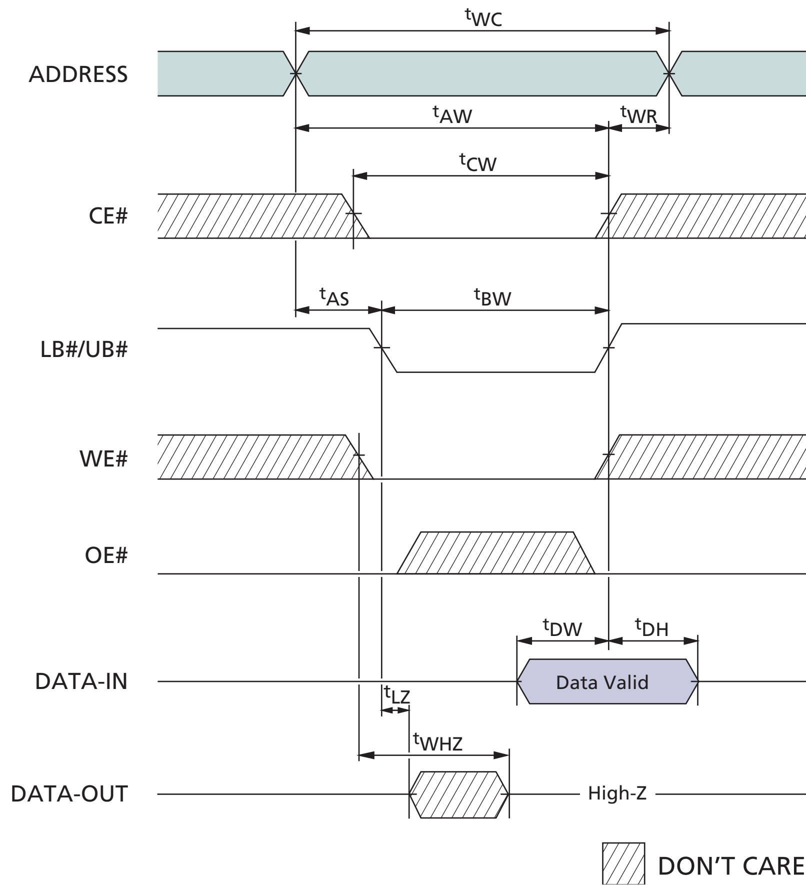

Table 22: WRITE Timing Parameters

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^tAS	0		0		ns
^tAW	70		85		ns
^tBW	70		85		ns
^tCW	70		85		ns
^tDH	0		0		ns

Symbol	-70 Min	-70 Max	-85 Min	-85 Max	Units
^tDW	23		25		ns
^tLZ	10		10		ns
^tWC	70		85		ns
^tWHZ		8		8	ns
^tWR	0		0		ns

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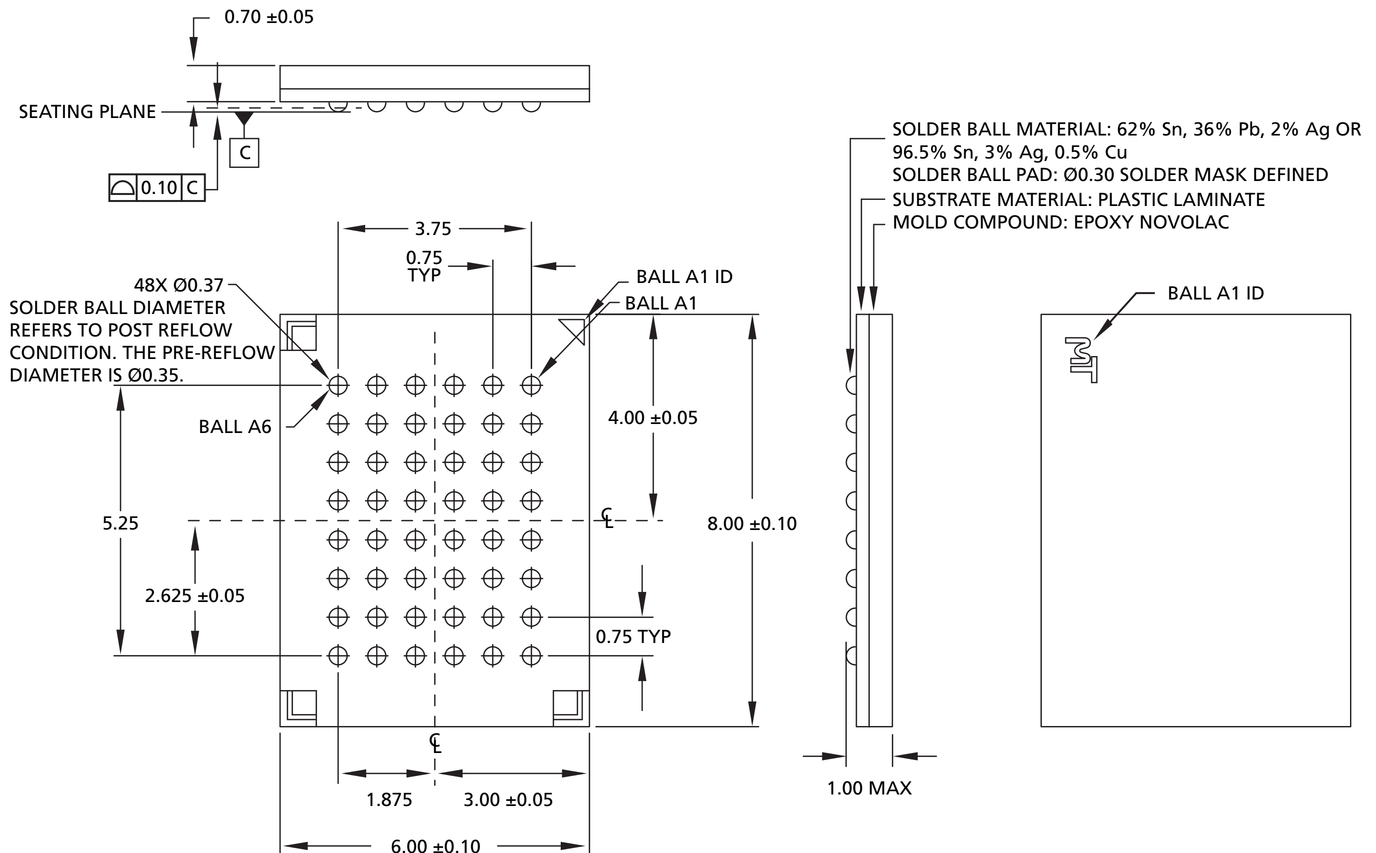
Figure 24: 48-Ball VFBGA



Notes: 1. All dimensions in millimeters, MAX/MIN, or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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Revision History

- Rev G 10/05
  - Added new P25A-specific note to the cover page.
- Rev F 04/05
  - Removed 60ns support.
  - Corrected typographic errors.
- Rev. E 12/04
  - Removed all references to 32Mb density.
  - Added Table 6, Maximum Standby Currents for Applying PAR and TCR Settings, on page 19
  - Added Table 7, Maximum Standby Currents for Applying PAR and TCR Settings – Low-Power (L), on page 19
  - Added Figure 13, Typical Refresh Current vs. Temperature (ITCR), on page 20
  - Added "Maximum and Typical Standby Currents" on page 19
- Rev. D 09/04
  - WE# LOW limited to ^{t}CEM for WRITEs.
  - Last address changed by software access sequence.
  - Noted software access third cycle must be CE#-controlled WRITE.
  - Change ^{t}CEH to ^{t}CPH.
  - Clarified TCR temperatures and setting in Table 6.
  - Changed VccQ Option W to 1.70V–3.30V.
  - Changed wireless temperature range to -30°C.
  - Noted input HIGH voltage not aligned with the Working Group specification of VccQ - 0.4.
  - Noted wireless temp (MIN) exceeds the Working Group spec.
- Rev. C, Preliminary 05/04
  - Clarified CE# LOW time limited by refresh—must not stay LOW longer than ^{t}CEM.
  - Changed ^{t}CEM MAX to 8.
  - Clarified address A[4] and higher in page mode.
  - Clarified ICC and updated symbols.
  - Changed PAR options to full, one-half, one-quarter, one-eighth, or none.
  - Deleted Appendix A (extended timings and all references).
  - Added CIN and CIO MIN values.
  - Replaced Abbreviated Component Marks table with Part Numbering chart.
  - Added measurement time clarification to ISB and IPAR notes
  - Corrected package nomenclature to VFBGA.
  - WE# LOW limited to ^{t}CEM for WRITES.
  - Last address changed by software access sequence.
  - Noted software access third cycle must be CE#-controlled WRITE.
  - Change ^{t}CEH to ^{t}CPH.
- Rev. B, Preliminary 12/03
  - Prohibited DPD via software access.
  - Updated Appendix regarding async page mode.
  - Added ^{t}WPH, ^{t}CEM, and ^{t}CW to tables and figures where not already appropriately represented.
  - Added "Access Using ZZ#" section.
  - Added software access section.

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- Added standard and low-power data in tables 8 & 9.
- V, IT, and -60 now “contact factory.
- Rev. A, Preliminary 07/03
  - Input/Output leakage to 1µA.
  - Added Industrial Temperature.
  - Changed standby power to 90µA and 100µA.
  - Changed Input High Voltage MAX to VccQ + 0.2.

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